171211191 Si53119-A01A and Si53119-A03A Datasheet Revisions

PCN Issue Date: 12/11/2017   **Effective Date:** 12/11/2017

PCN Type: Datasheet

Description of Change

Silicon Labs is pleased to announce the following Si53119-A01A and Si53119-A03A datasheet revisions:
Si53119-A01A: Update I2C register settings, remove Gen4 PLL mode jitter specification
Si53119-A03A: Update I2C register settings, remove Gen4 PLL mode jitter specification, update block diagram.

Reason for Change

The following changes are to correct typographical errors:
1) Update I2C register section to include a table for Byte18
2) PCI-SIG updated Gen4 refCLK jitter specification
3) Request to show internal resistors on the Si53119-A03A datasheet block diagram
4) Update and correct the Byte6 ID register values in Si53119-A03A datasheet.

Impact on Form, Fit, Function, Quality, Reliability

No impact on form, fit, function, quality and reliability.

Product Identification

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Si53119-A01AGM
Si53119-A01AGMR
Si53119-A03AGM
Si53119-A03AGMR
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Last Date of Unchanged Product: 12/11/2017

Qualification Samples

n/a

Specific conditions of acceptance of this change will be considered on a case by case basis if written notice is submitted within 30 days of this notice. To request further data or inquire about this notification, please contact your local Silicon Labs sales representative. A list of Silicon Labs sales representatives is available at http://www.silabs.com.

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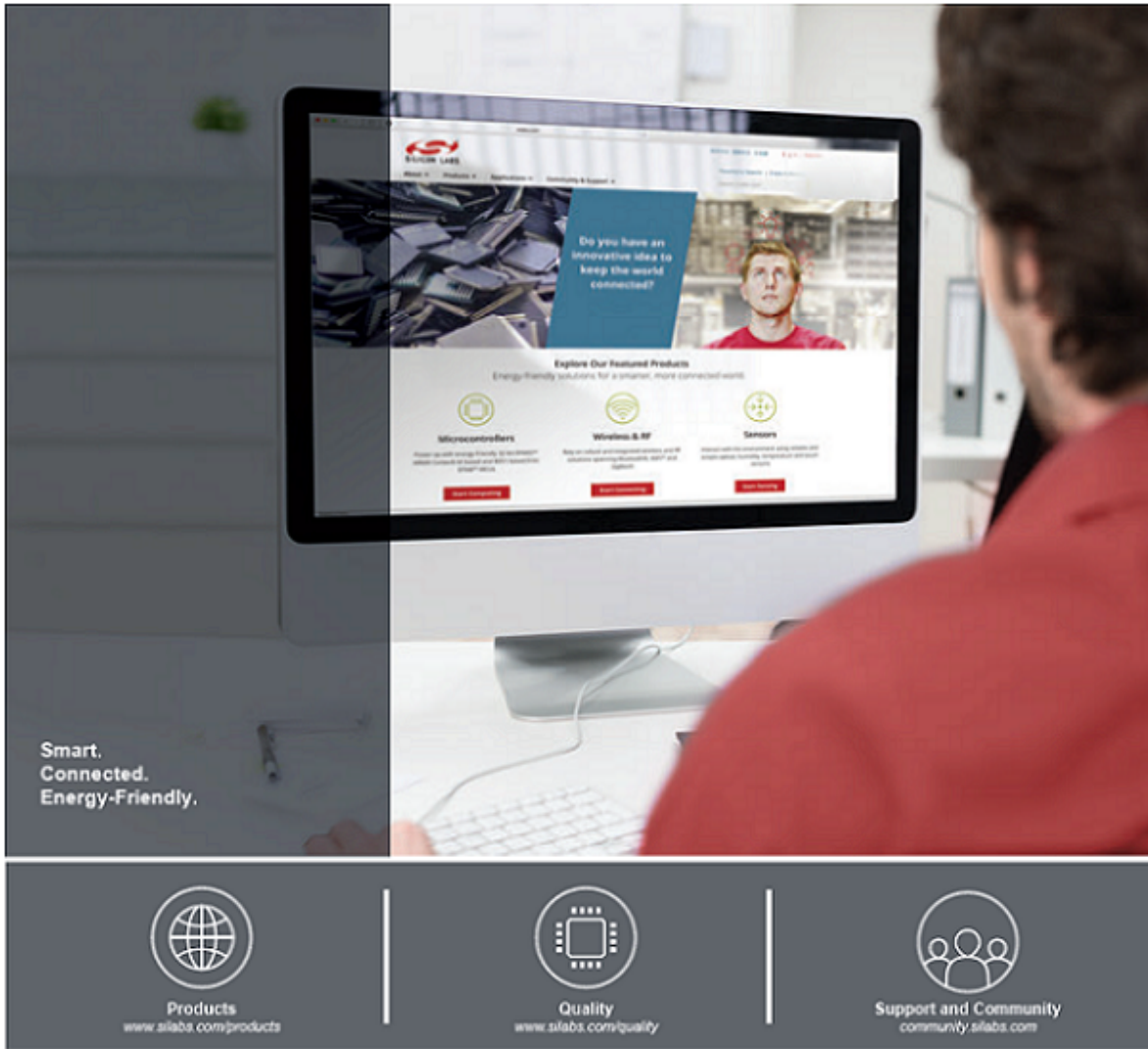
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Qualification Data

n/a

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Silicon Laboratories Inc.
400 West Cesar Chavez
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