PRODUCT/PROCESS CHANGE NOTIFICATION

PCN IPG-PWR/14/8603
Dated 21 Jul 2014

MDmesh II Technology, Power MOSFET Transistors, 8"

Wafer size Front-end Capacity Extension - Ang Mo Kio (Singapore)

Table 1. Change Implementation Schedule

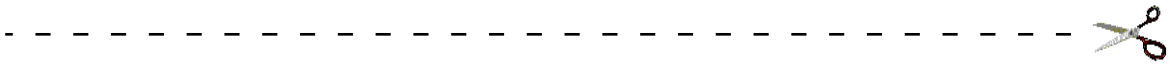
Forecasted implementation date for change	15-Jul-2014
Forecasted availability date of samples for customer	15-Jul-2014
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	15-Jul-2014
Estimated date of changed product first shipment	20-Oct-2014

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	see attached list
Type of change	Waferfab process change
Reason for change	Capacity extension
Description of the change	Following the continuous improvement of our service and in order to increase Power MOSFET productivity, this document is announcing the new 8" wafer line for MDmesh II Technology of Power MOSFET Transistors in the ST's Ang Mo Kio (Singapore) FAB. 8" wafer size production, guarantees the same quality and electrical characteristics as the current 6".
Change Product Identification	by traceability code
Manufacturing Location(s)	

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	



Customer Acknowledgement of Receipt	**PCN IPG-PWR/14/8603**
Please sign and return to STMicroelectronics Sales Office	**Dated 21 Jul 2014**
☐ Qualification Plan Denied	Name:
☐ Qualification Plan Approved	Title:
	Company:
☐ Change Denied	Date:
☐ Change Approved	Signature:

Remark

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DOCUMENT APPROVAL

Name	Function
Mottese, Anna	Marketing Manager
Aleo, Mario-Antonio	Product Manager
Falcone, Giuseppe	Q.A. Manager

Dear Customer,

Following the continuous improvement of our service and in order to increase Power MOSFET productivity, this document is announcing the new 8" wafer line for MDmesh™ II Technology of Power MOSFET Transistors in the ST's Ang Mo Kio (Singapore) FAB.
8" wafer size production, guarantees the same quality and electrical characteristics as the current 6".

The involved product series and affected packages are listed in the table below:

Product Family	Technology	Commercial Product / Series
Power MOSFET Transistors	MDmesh™ II	See attached list

Any other Product related to the above series, manufactured in the ST's Ang Mo Kio (Singapore) FAB, even if not expressly included or partially mentioned in the attached table, is affected by this change.

Qualification program and results availability:

The reliability test report is provided in attachment to this document.

Samples availability:

Samples of the test vehicle devices will be available on request starting from week 29-2014.
Any other sample request will be processed and scheduled by Power Transistor Division upon request.

Product Family	Package	Part Number - Test Vehicle
Power MOSFET Transistors	TO-220 IPAK IPAK	STP13NM60N STU13NM60N STU7NM60N

Change implementation schedule:

The production start and first shipments will be implemented according to our work in progress and materials availability:

Product Family	1st Shipments
Power MOSFET Transistors	From Week 42-2014

Lack of acknowledgement of the PCN within 30 days will constitute acceptance of the change. After acknowledgement, lack of additional response within the 90 days period will constitute acceptance of the change (Jedec Standard No. 46-C). In any case, first shipment may start earlier with customer written agreement.

Marking and traceability:

Unless otherwise stated by customer specific requirement, traceability of 8” wafer size, manufactured in ST’s Ang Mo Kio (Singapore) FAB, will be ensured by traceability code.

Sincerely Yours.

STP13NM60N -> 6" mass production Vs 8" pre-production

Static parameter distributions:

BVDSS @ 1mA; VTH @ 250uA; VSD @ 11A; RDSON@ 5.5A;

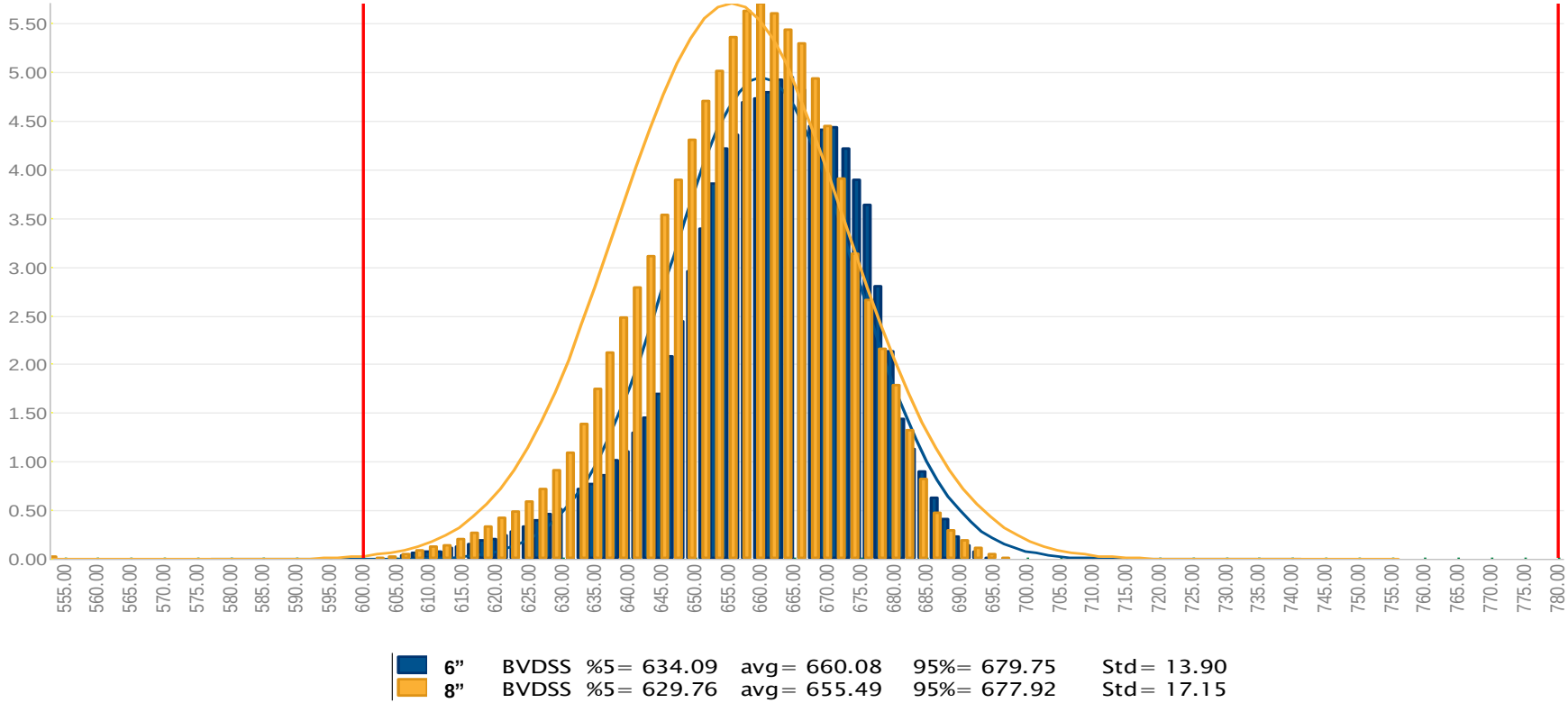
life.augmented

BVDSS@1mA

STP13NM60N

P-M263 BVDSS@ 1mA

6" mass production Vs 8" preproduction

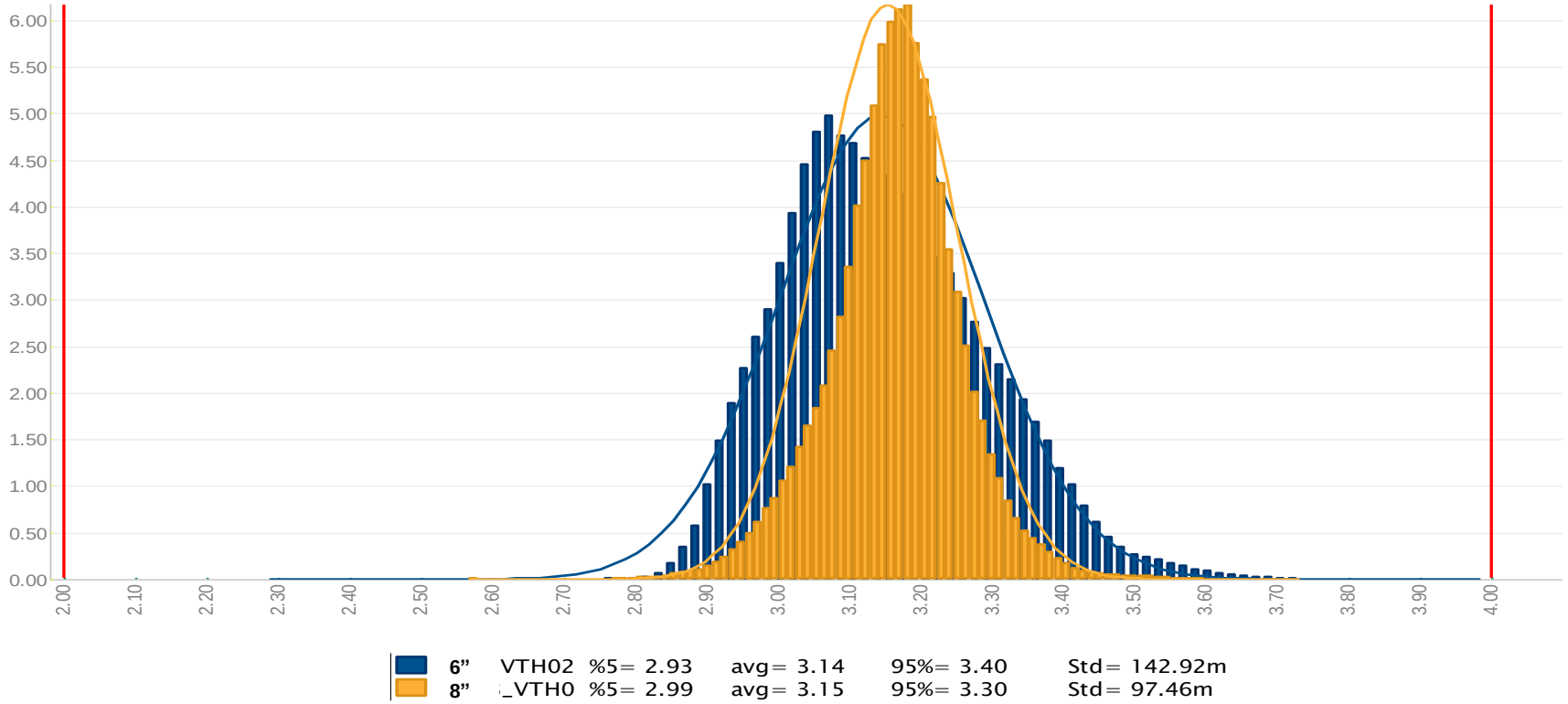


Vth@250uA

STP13NM60N

P-M263 VTH@ 250uA

6" mass production Vs 8" preproduction

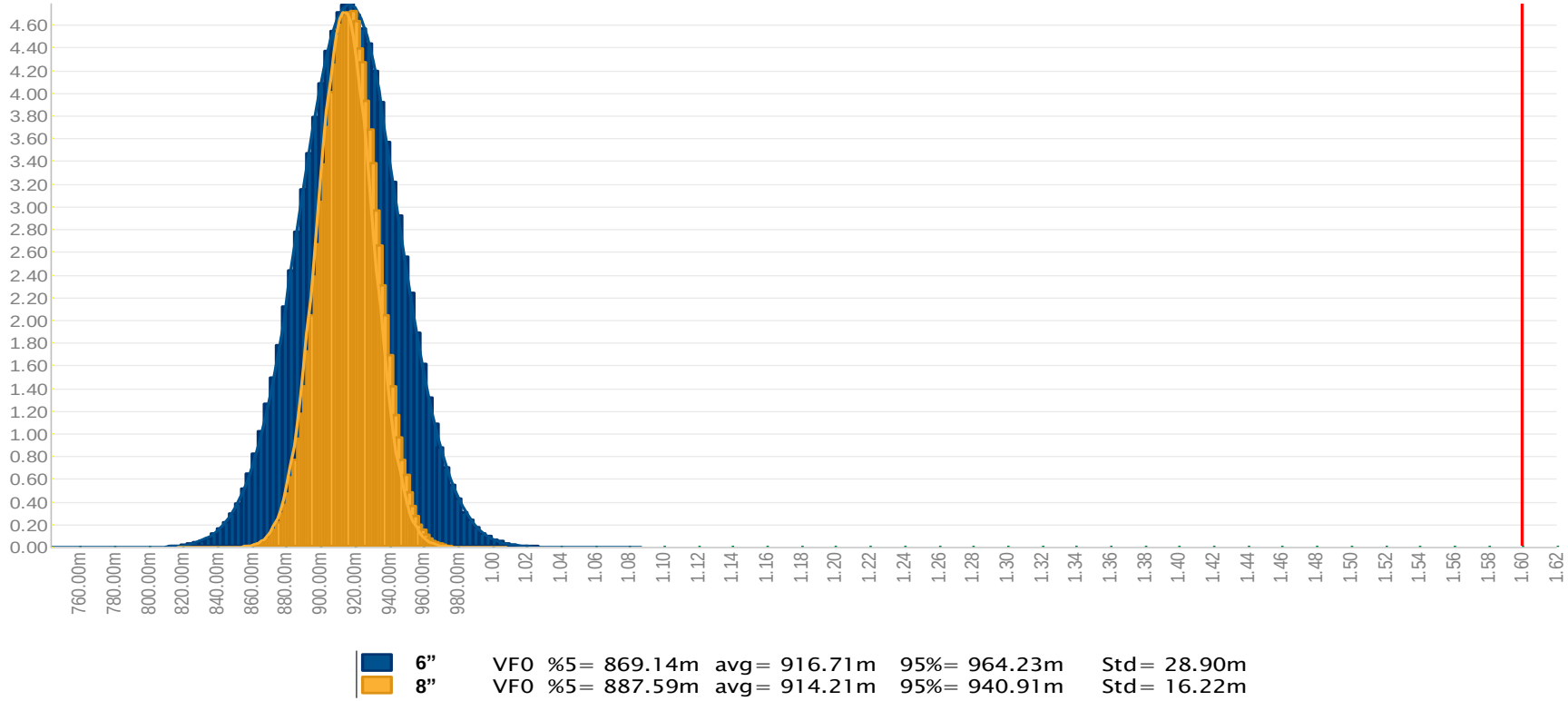


VSD@ 11A

STP13NM60N

P-M263 VSD@ 11A

6" mass production Vs 8" preproduction

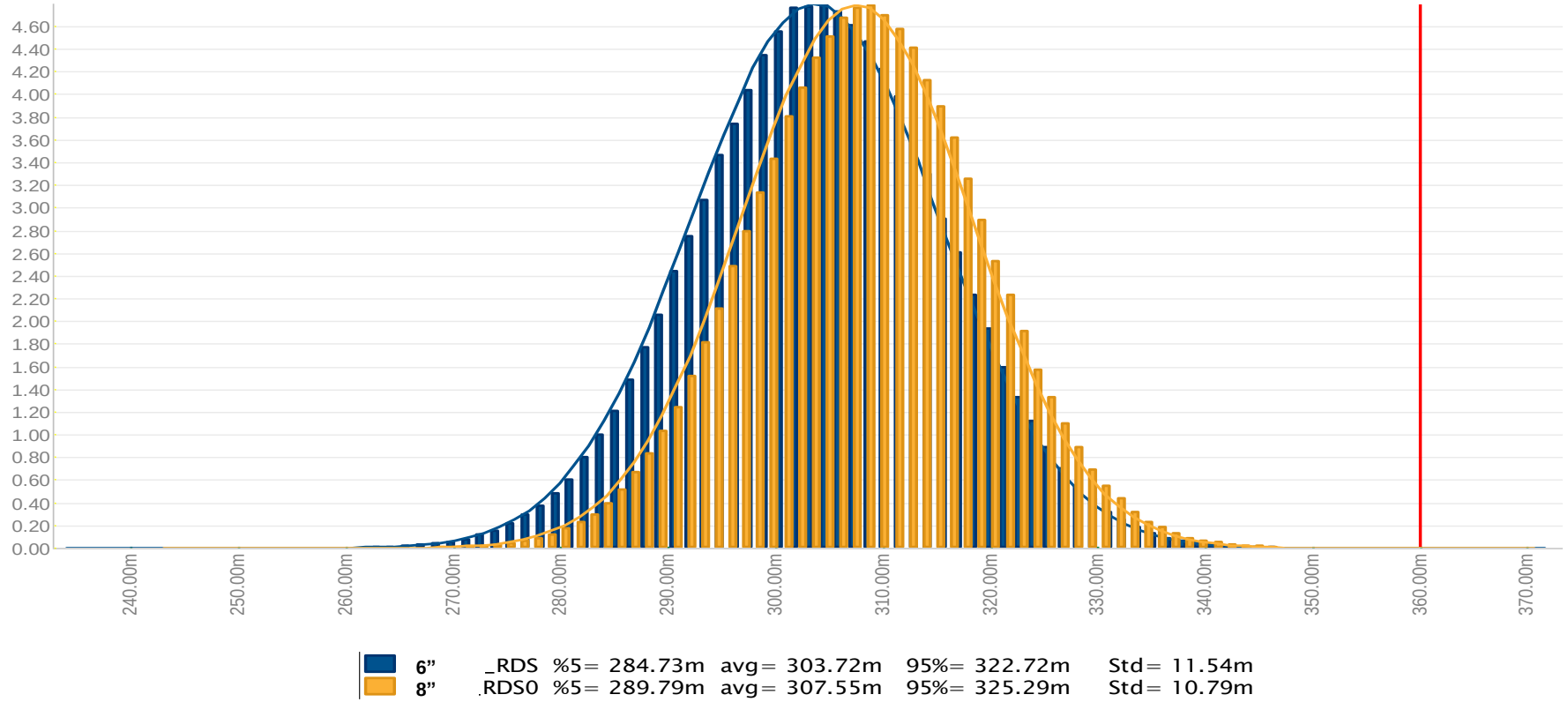


RDSon@5.5A

STP13NM60N

P-M263 RDSon

6" mass production Vs 8" preproduction



STU7NM60N -> 6" mass production Vs 8" pre-production

Static parameter distributions:

BVDSS @ 1mA; VTH @ 250uA; VSD @ 5A; RDSON@ 2.5A;

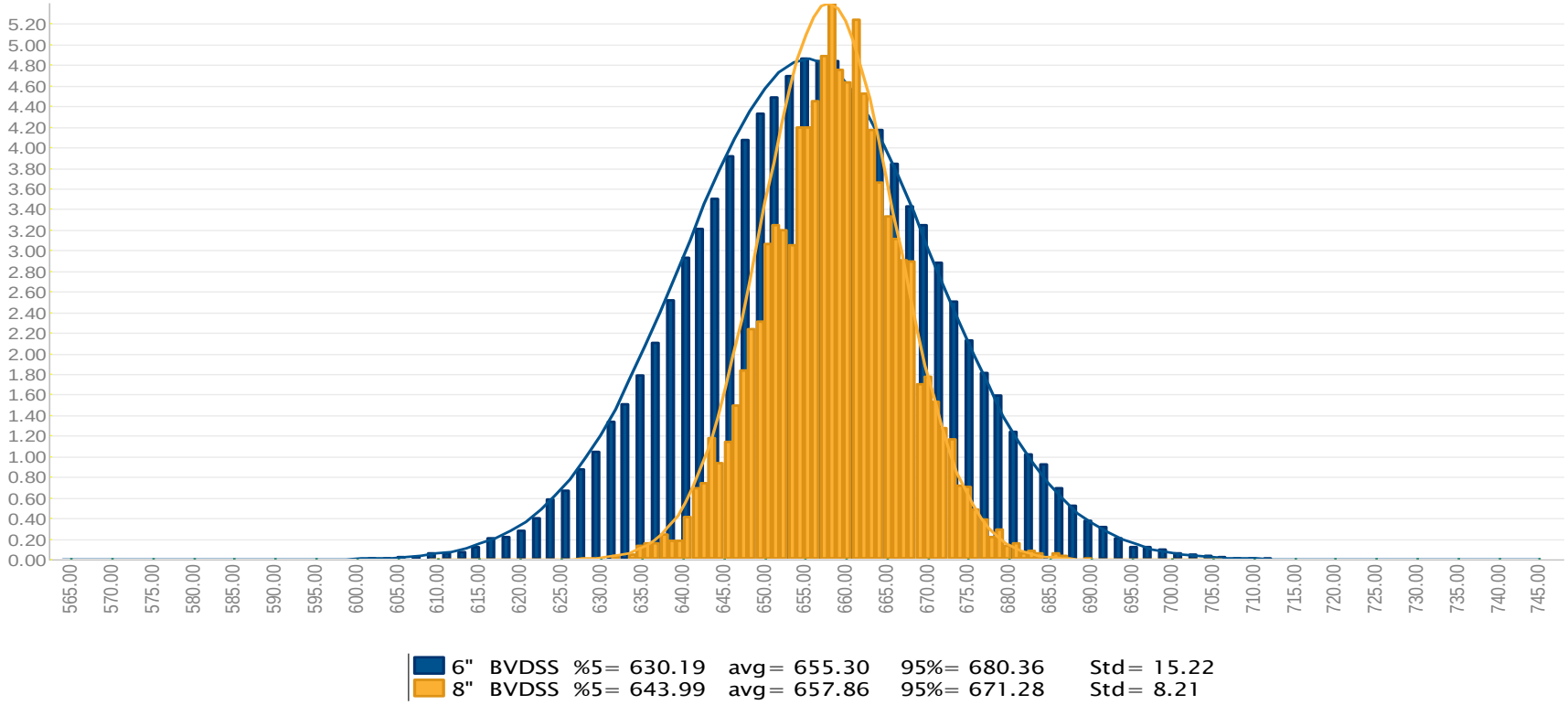
life.augmented

BVDSS@1mA

STU7NM60N

M260 - BVDSS@1mA

6" mass prod vs 8" preprod

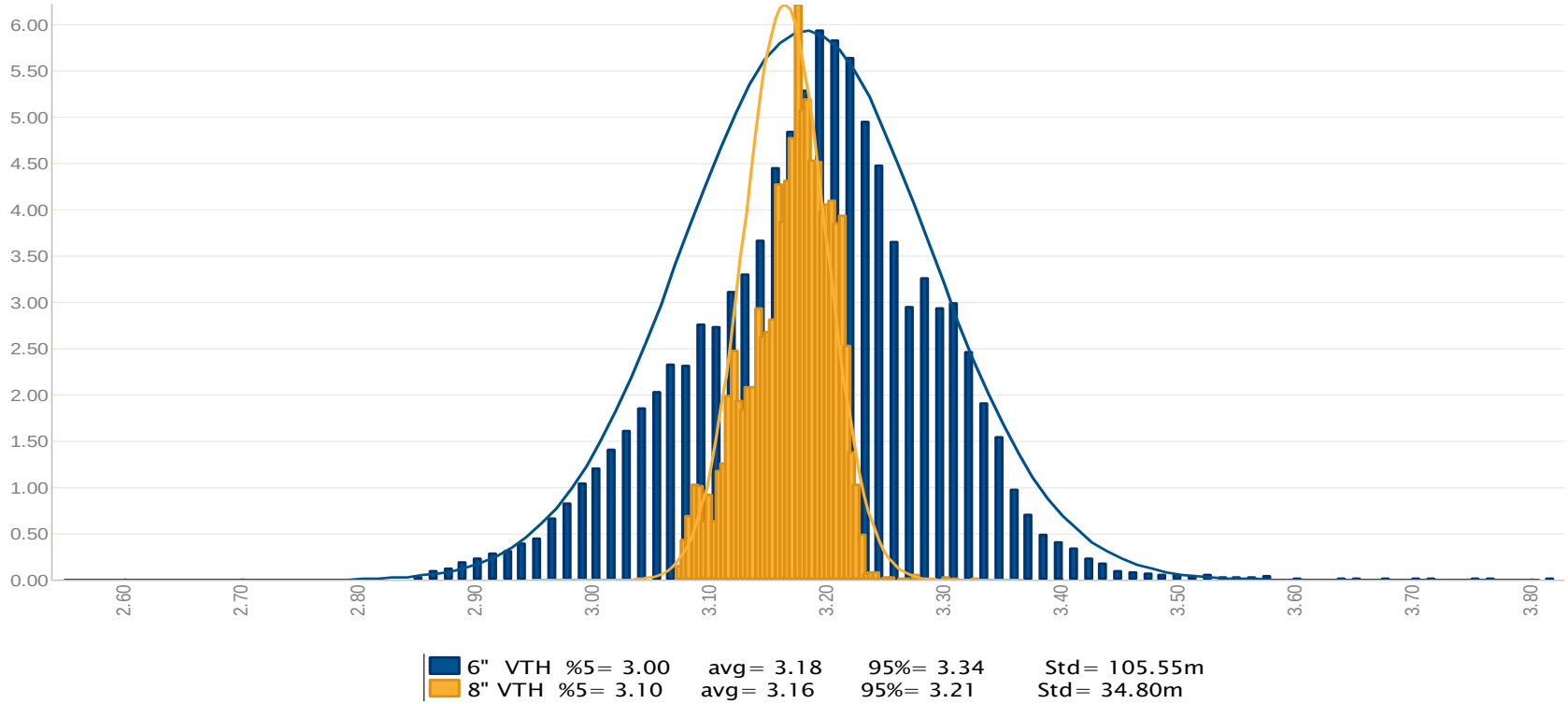


Vth@250uA

STU7NM60N

M260 - Vth@250uA

6" mass prod vs 8" preprod

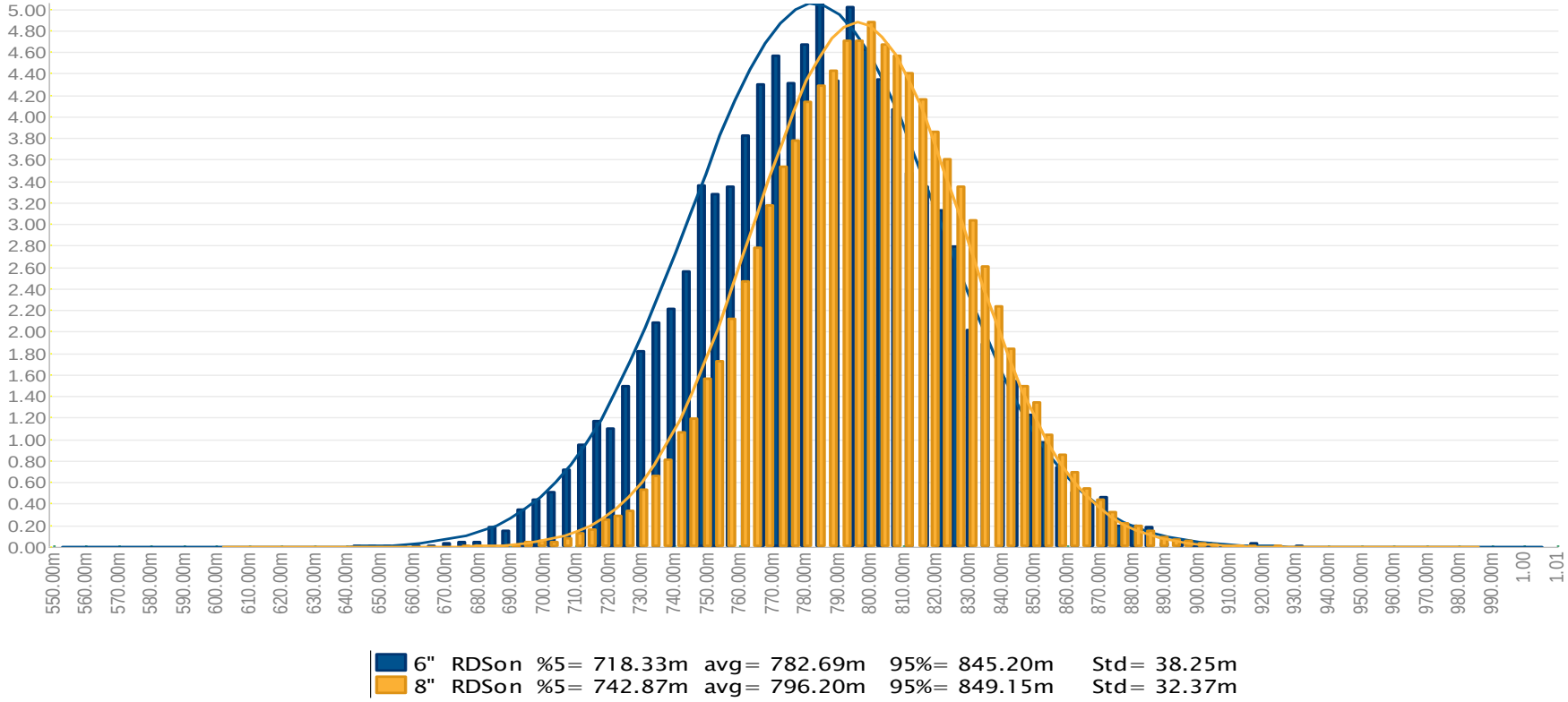


RDSon@ 2.5A

STU7NM60N

M260 - RDSon@ 2.5A

6" mass prod vs 8" preprod

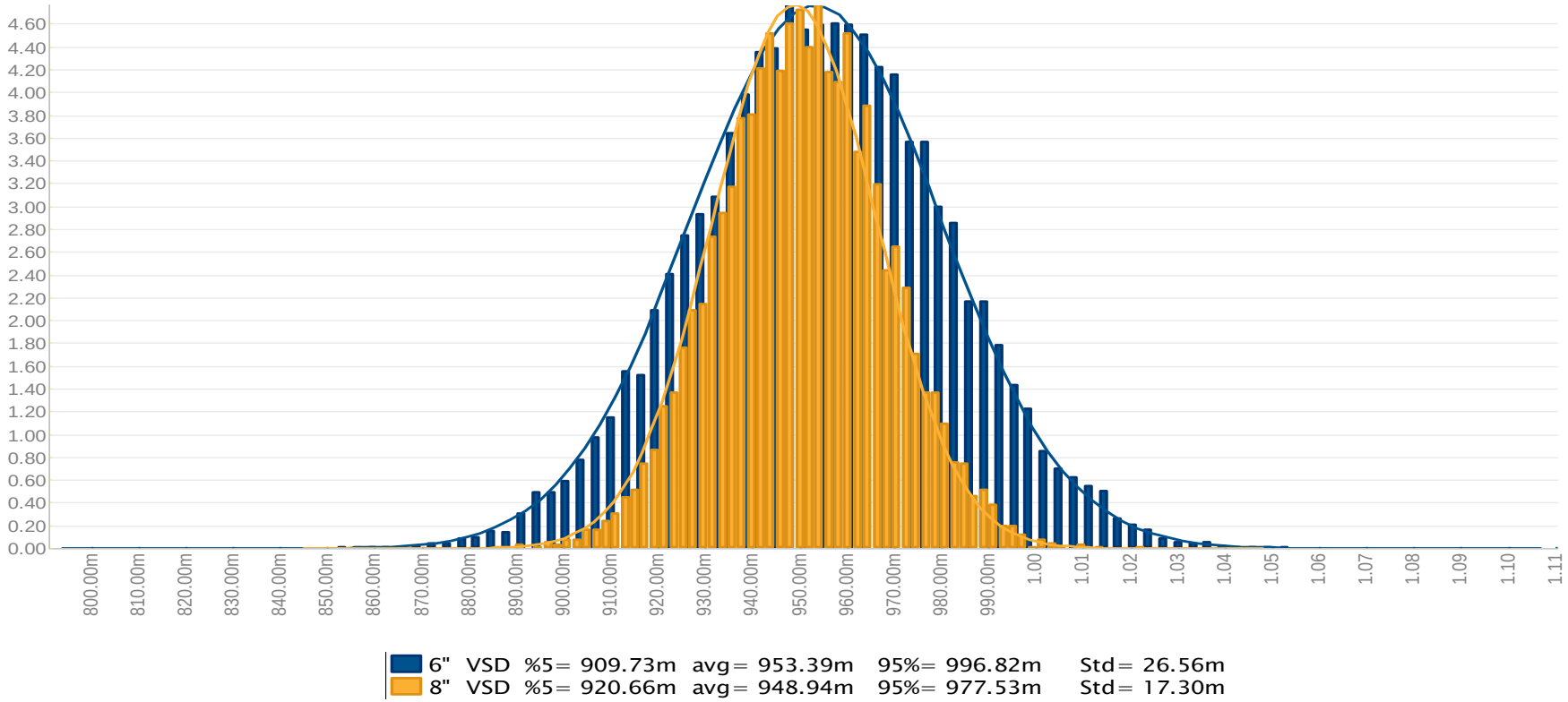


VSD@ 5A

STU7NM60N

M260 - VSD@ 5A

6" mass prod vs 8" preprod



Reliability Report

MDmesh™ II Technology, Power MOSFET Transistors,
8" Wafer size Front-end Capacity Extension
Ang Mo Kio (Singapore)

General Information	
Product Lines:	M260 – M263
Product Families:	Power MOSFET
P/Ns:	STU7NM60N (M260) STU13NM60N (M263) STP13NM60N (M263)
Product Group:	IPG
Product division:	Power Transistor Division
Package:	IPAK / TO-220
Silicon Process techn.:	MDmesh™ II Power MOSFET

Locations	
Wafer Diffusion Plants:	*Ang Mo Kio 8" (Singapore)*
EWS Plants:	Toa Payoh (Singapore)
Assembly and testing plant:	Shenzhen (China)
Reliability Lab:	*IPG-PTD Catania Reliability Lab.*

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	July 2014	8	A. Settinieri	C. Cappello	First issue

TABLE OF CONTENTS

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

2 GLOSSARY

DUT	Device Under Test
SS	Sample Size
HF	Halogen Free

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

Reliability evaluation for MDmesh™ II Technology, Power MOSFET Transistors, 8" Wafer size Front-end Capacity Extension - Ang Mo Kio (Singapore).

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. It is stressed that reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description

N-channel Power MOSFET

4.2 Construction note

D.U.T.: STU7NM60N LINE: M260 PACKAGE: IPAK

Wafer/Die fab. Information	
Wafer fab manufacturing location	Ang Mo Kio 8" (Singapore)
Technology	MDmesh™ II Power MOSFET
Die finishing back side	Ti/Ni/Ag
Die size	2410 x 2400 µm^2
Metal	AlSi
Passivation type	Nitride

Wafer Testing (EWS) information	
Electrical testing manufacturing location	Ang Mo Kio 8" (Singapore)
Test program	WPIS

Assembly information	
Assembly site	Shenzhen (China)
Package description	IPAK
Molding compound	HF Epoxy Resin
Frame material	Raw Copper
Die attach process	Soft Solder
Die attach material	Pb/Sn/Ag
Wire bonding process	Ultrasonic
Wires bonding materials	Al/Mg Gate – Al Source
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	Toa Payoh (Singapore)
Tester	IPTEST

D.U.T.: STU13NM60N LINE: M263 PACKAGE: IPAK

Wafer/Die fab. Information	
Wafer fab manufacturing location	Ang Mo Kio 8” (Singapore)
Technology	MDmesh™ II Power MOSFET
Die finishing back side	Ti/Ni/Ag
Die size	3950 x 2930 µm^2
Metal	AlSi
Passivation type	Nitride

Wafer Testing (EWS) information	
Electrical testing manufacturing location	Ang Mo Kio 8” (Singapore)
Test program	WPIS

Assembly information	
Assembly site	Shenzhen (China)
Package description	IPAK
Molding compound	HF Epoxy Resin
Frame material	Raw Copper
Die attach process	Soft Solder
Die attach material	Pb/Sn/Ag
Wire bonding process	Ultrasonic
Wires bonding materials	Al/Mg Gate – Al Source
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	Toa Payoh (Singapore)
Tester	IPTEST

D.U.T.: STP13NM60N LINE: M263 PACKAGE: TO-220

Wafer/Die fab. Information	
Wafer fab manufacturing location	Ang Mo Kio 8” (Singapore)
Technology	MDmesh™ II Power MOSFET
Die finishing back side	Ti/Ni/Ag
Die size	3950 x 2930 µm^2
Metal	AlSi
Passivation type	Nitride

Wafer Testing (EWS) information	
Electrical testing manufacturing location	Ang Mo Kio 8” (Singapore)
Test program	WPIS

Assembly information	
Assembly site	Shenzhen (China)
Package description	TO-220
Molding compound	HF Epoxy Resin
Frame material	Raw Copper
Die attach process	Soft Solder
Die attach material	Pb/Sn/Ag
Wire bonding process	Ultrasonic
Wires bonding materials	Al/Mg Gate – Al Source
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	Toa Payoh (Singapore)
Tester	IPTEST

5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Lot #	Process/ Package	Product Line	Comments
1	STU7NM60N	IPAK	Power MOSFET
2	STU13NM60N	IPAK	Power MOSFET
3	STP13NM60N	TO-220	Power MOSFET

5.2 Reliability test plan summary

Test	Std ref.	Conditions	SS	Steps	Failure/SS		
					LOT1 M260/IPAK	LOT2 M263/IPAK	LOT3 M263/TO-220
Die Oriented Tests							
HTRB	JESD22 A-108	TA = 150°C BIAS=480V	50 x 3 lots	168 H	0/50	0/50	0/50
				500 H	0/50	0/50	0/50
				1000 H	0/50	0/50	0/50
HTGB	JESD22 A-108	TA = 150°C BIAS=20V	50 x 3 lots	168 H	0/50	0/50	0/50
				500 H	0/50	0/50	0/50
				1000 H	0/50	0/50	0/50
HTSL	JESD22 A-103	TA = 150°C	50 x 3 lots	168 H	0/50	0/50	0/50
				500 H	0/50	0/50	0/50
				1000 H	0/50	0/50	0/50
Package Oriented Tests							
AC	JESD22 A-102	Pa=2Atm / TA=121°C	25 x 3 lots	96 H	0/25	0/25	0/25
TC	JESD22 A-104	TA = -65°C/150°C	25 x 3 lots	100 cy	0/25	0/25	0/25
				200 cy	0/25	0/25	0/25
				500 cy	0/25	0/25	0/25
TF/IOL	Mil-Std 750D Method 1037	ΔTC=105°C	25 x 3 lots	5Kcy	0/25	0/25	0/25
				10Kcy	0/25	0/25	0/25
H3TRB	JESD22 A-101	TA=85°C , RH=85% BIAS=100V	25 x 3 lots	168 H	0/25	0/25	0/25
				500 H	0/25	0/25	0/25
				1000 H	0/25	0/25	0/25

6 ANNEXES 6.0

6.1Tests Description

Test name	Description	Purpose
Die Oriented Tests		
HTRB High Temperature Reverse Bias **HTGB** High Temperature Forward (Gate) Bias	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: • low power dissipation; • max. supply voltage compatible with diffusion process and internal circuitry limitations;	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
Package Oriented Tests		
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
TF / IOL Thermal Fatigue / Intermittent Operating Life	The device is submitted to cycled temperature excursions generated by power cycles (ON/OFF) at T ambient.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
H3TRB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.

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