IA82527
Serial Communications Controller—CAN Protocol
Data Sheet

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3737 Princeton Drive NE, Suite 130, Albuquerque, NM 87107

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1. Introduction

The Innovasic Semiconductor IA82527 Controller Area Network (CAN) Serial Communications Controller is a form, fit, and function replacement for the original Intel® 82527 Serial Communications Controller.

These devices are produced using Innovasic's Managed IC Lifetime Extension System (MILES™). This cloning technology, which produces replacement ICs beyond simple emulations, is designed to achieve compatibility with the original device, including any "undocumented features." Please note that there may be some functional differences between the Innovasic device and the original device and customers should thoroughly test the device in system to ensure compatibility. Innovasic reports all known functional differences in the Errata section of this data sheet. Additionally, MILES™ captures the clone design in such a way that production of the clone can continue even as silicon technology advances.

The IA82527 Serial Communications Controller replaces the obsolete Intel 82527 device, allowing users to retain existing board designs, software compilers/assemblers, and emulation tools, thereby avoiding expensive redesign efforts.

1.1 General Description

CAN protocol uses a multi-master CSMA/CR (Carrier Sense, Multiple Access with Collision Resolution) bus to transfer message objects between network nodes.

The IA82527 support CAN Specification 2.0 Part A and B, standard and extended message frames, and has the capability to transmit, receive, and perform message filtering on standard and extended message frames.

The IA82527 can store 15 message objects of 8-byte data length. Each message object can be configured as either transmit or receive except for message object 15, which is receive-only. Message object 15 also provides a special acceptance mask designed to filter message identifiers that are received.

The IA82527 also provides a programmable acceptance mask that allows users to globally mask any identifier bits of the incoming message. This global mask can be used for both standard and extended message frames.

The IA82527 is capable of operating at 5.0 or 3.3 volts. This datasheet discusses both modes of operation. Where applicable, characteristics specific to either 3.3 or 5.0 volt operation are identified separately throughout this datasheet.

The IA82527 is manufactured in a reliable 5-volt process technology and is available in 44-lead PLCC or PQFP RoHS packages for the automotive temperature range (-40°C to 125°C).

1.2 Features

The primary features of the IA82527 are as follows:

- CAN Protocol Support
  - Specification 2.0, Part A and Part B
  - Standard ID Data and Remote Frames
  - Extended ID Data and Remote Frames

- CAN Bus Interface
  - Configurable Input Comparator
  - Configurable Output Driver
  - Programmable Bit Rate

- Global Mask, Programmable
  - Standard Message Identifier
  - Extended Message Identifier

- Message Objects
  - 14 Transmit/Receive Buffers
  - 1 Double Buffered Receive Buffer with Programmable Mask

- Flexible Status Interface

- CPU Interface Options
  - 16-Bit Multiplexed Intel Architecture
  - 8-Bit Multiplexed Intel Architecture
  - 8-Bit Multiplexed Non-Intel Architecture
  - 8-Bit Non-Multiplexed Non-Intel Architecture
  - Serial (SPI)

- I/O Ports (2)
  - 8-Bit
  - Bidirectional

- Flexible Interrupt Structure

- Programmable Clock Output

A detailed description of the IA82527, including the features listed above, is provided in Chapter 4, Functional Description.

2. Packaging, Pin Descriptions, and Physical Dimensions

2.1 Packages and Pinouts

The Innovasic Semiconductor IA82527 CAN Serial Communications Controller is available in the following RoHS packages:

- 44-Pin Plastic Leaded Chip Carrier (PLCC), equivalent to original Intel PLCC package
- 44-Pin Plastic Quad Flat Pack (PQFP), equivalent to original Intel QFP package

2.1.1 PLCC Package

The pinout for the PLCC Package is as shown in Figure 1. The corresponding pinout is provided in Table 1.

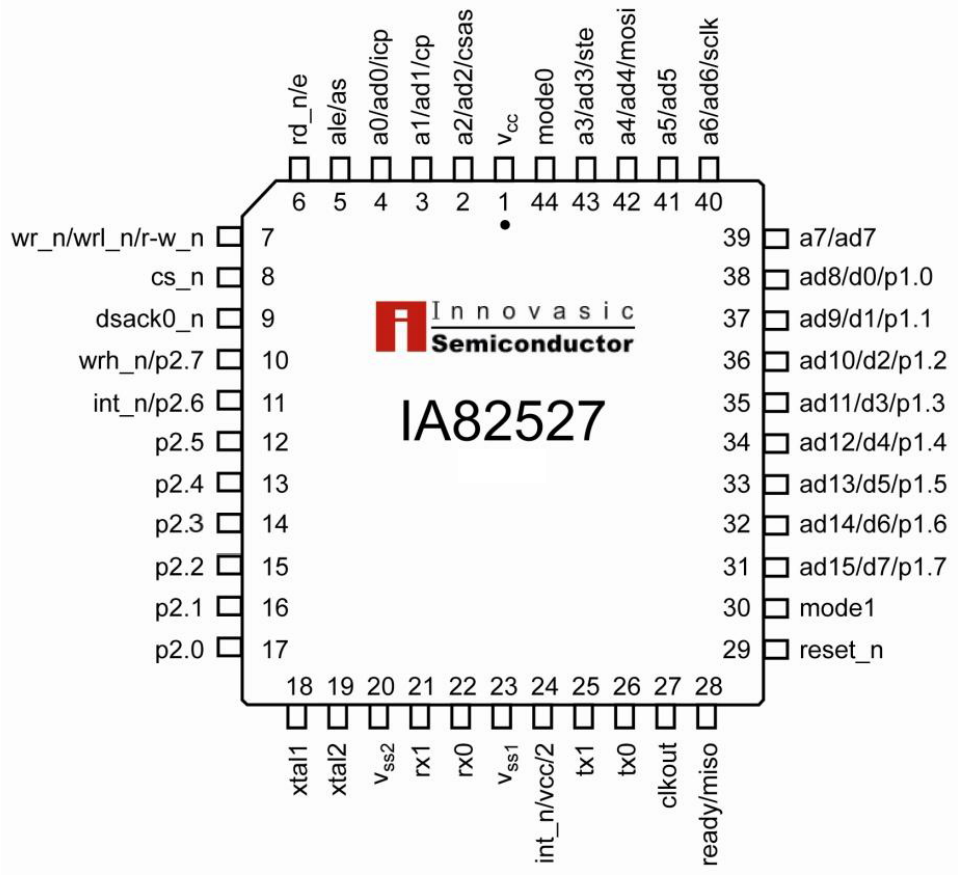


Figure 1. PLCC Package Diagram

Table 1. PLCC Pin List

Pin	Name
1	v_{cc}
2	a2/ad2/csas
3	a1/ad1/cp
4	a0/ad0/icp
5	ale/as
6	rd_n/e
7	wr_n/wrl_n/r-w_n
8	cs_n
9	dsack0_n
10	wrh_n/p2.7
11	int_n/p2.6

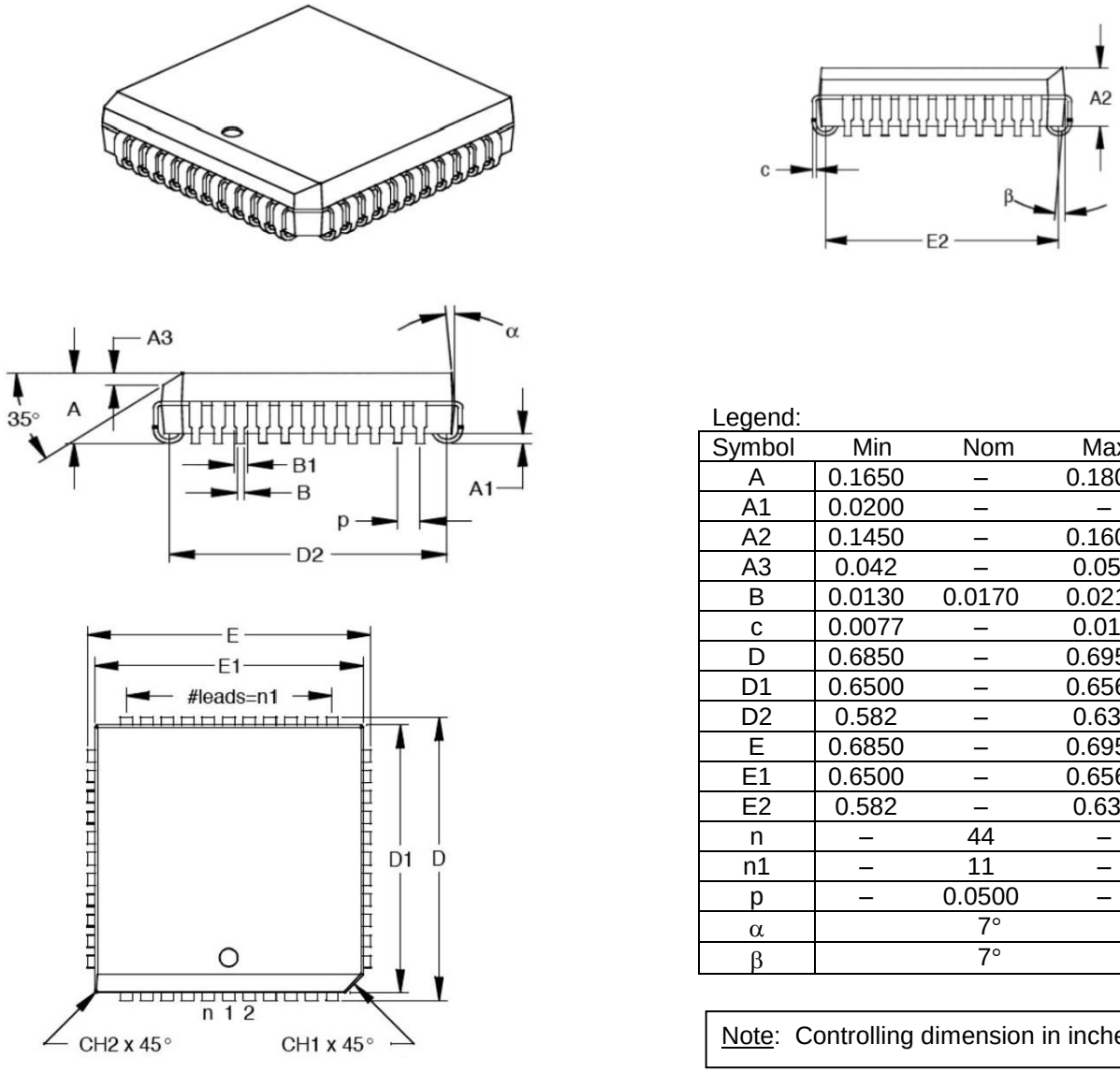
Pin	Name
12	p2.5
13	p2.4
14	p2.3
15	p2.2
16	p2.1
17	p2.0
18	xtal1
19	xtal2
20	v_{ss2}
21	rx1
22	rx0

Pin	Name
23	v_{ss1}
24	int_n/v_{cc}/2
25	tx1
26	tx0
27	clkout
28	ready/miso
29	reset_n
30	mode1
31	ad15/d7/p1.7
32	ad14/d6/p1.6
33	ad13/d5/p1.5

Pin	Name
34	ad12/d4/p1.4
35	ad11/d3/p1.3
36	ad10/d2/p1.2
37	ad9/d1/p1.1
38	ad8/d0/p1.0
39	a7/ad7
40	a6/ad6/sclk
41	a5/ad5
42	a4/ad4/mosi
43	a3/ad3/ste
44	mode0

2.1.2 PLCC Physical Dimensions

The physical dimensions for the PLCC are as shown in Figure 2.



Legend:

Symbol	Min	Nom	Max
A	0.1650	–	0.1800
A1	0.0200	–	–
A2	0.1450	–	0.1600
A3	0.042	–	0.056
B	0.0130	0.0170	0.0210
c	0.0077	–	0.015
D	0.6850	–	0.6950
D1	0.6500	–	0.6560
D2	0.582	–	0.638
E	0.6850	–	0.6950
E1	0.6500	–	0.6560
E2	0.582	–	0.638
n	–	44	–
n1	–	11	–
p	–	0.0500	–
α		7°	
β		7°	

Note: Controlling dimension in inches.

Figure 2. PLCC Physical Dimensions

2.1.3 PQFP Package

The pinout for the PQFP Package is as shown in Figure 3. The corresponding pinout is provided in Table 2.

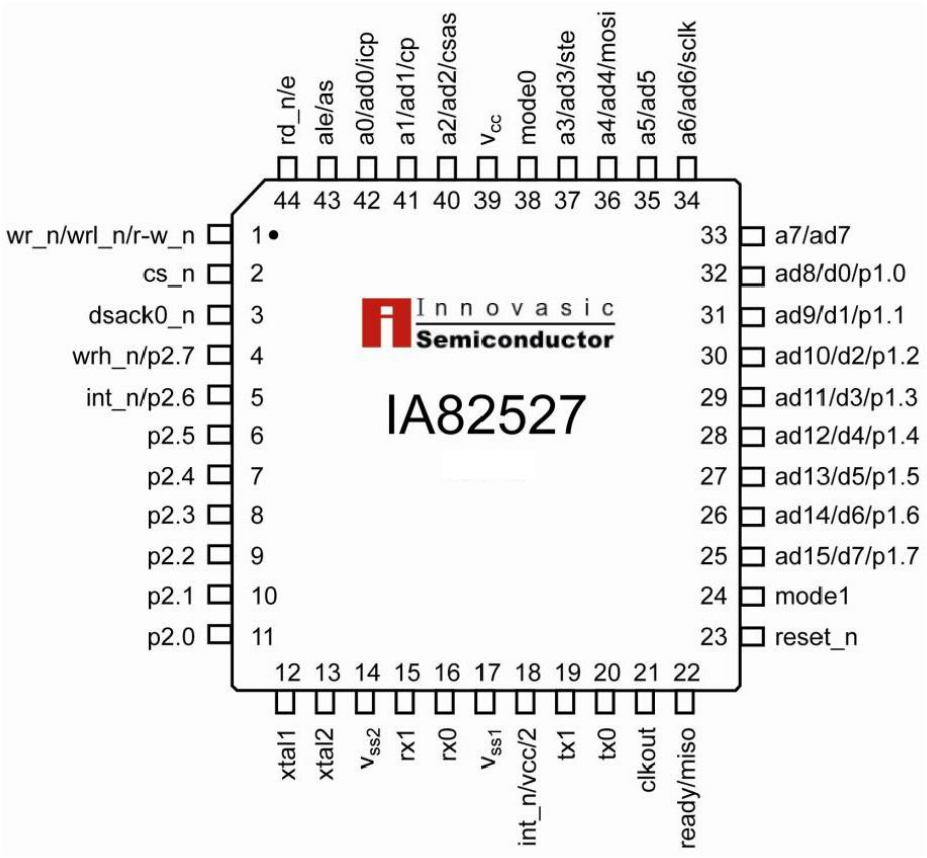


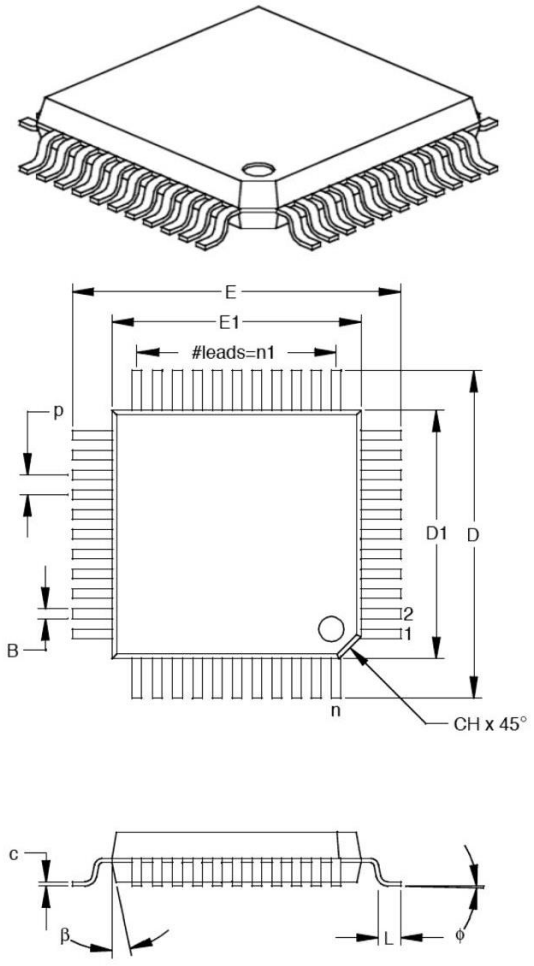
Figure 3. PQFP Package Diagram

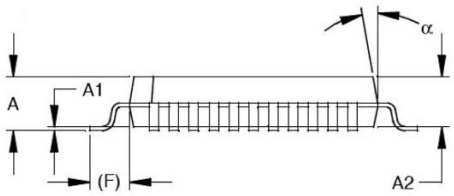
Table 2. PQFP Pin List

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	wr_n/wrl_n/r-w_n	12	xtal1	23	reset_n	34	a6/ad6/sclk
2	cs_n	13	xtal2	24	mode1	35	a5/ad5
3	dsack0_n	14	v_{ss2}	25	ad15/d7/p1.7	36	a4/ad4/mosi
4	wrh_n/p2.7	15	rx1	26	ad14/d6/p1.6	37	a3/ad3/ste
5	int_n/p2.6	16	rx0	27	ad13/d5/p1.5	38	mode0
6	p2.5	17	v_{ss1}	28	ad12/d4/p1.4	39	v_{cc}
7	p2.4	18	int_n/v_{cc}/2	29	ad11/d3/p1.3	40	a2/ad2/csas
8	p2.3	19	tx1	30	ad10/d2/p1.2	41	a1/ad1/cp
9	p2.2	20	tx0	31	ad9/d1/p1.1	42	a0/ad0/icp
10	p2.1	21	clkout	32	ad8/d0/p1.0	43	ale/as
11	p2.0	22	ready/miso	33	a7/ad7	44	rd_n/e

2.1.4 PQFP Physical Dimensions

The physical dimensions for the PQFP are as shown in Figure 4.





Legend:

Symbol	Min	Nom	Max
n	–	44	–
n1	–	11	–
p	–	0.031	–
A	–	–	0.096
A2	–	0.079	–
A1	–	0.010	–
L	0.019	0.025	0.031
(F)	–	0.047	–
E	0.478	0.488	0.498
D	0.478	0.488	0.498
E1	0.390	0.394	0.398
D1	0.390	0.394	0.398
c	0.005	0.007	0.009
B	0.011	0.014	0.017
CH	–	0.030	–
α	5°	–	16°
β	5°	–	16°
ϕ	0°	–	10°

Note: Controlling dimension in inches.

Figure 4. PQFP Physical Dimensions

2.2 Pin/Signal Descriptions

Descriptions of the pin and signal functions for the IA82527 Serial Communications Controller are provided in Table 3.

Several of the IA82527 pins have different functions depending on the operating mode of the device. Each of the different signals supported by a pin is listed and defined in Table 3, indexed alphabetically in the first column of the table. Additionally, the name of the pin associated with the signal as well as the pin numbers for both the PLCC and PQFP packages are provided in the "Pin" column. If the signal and pin names are the same, no entry is provided in the "Pin-Name" column.

Table 3. Pin/Signal Descriptions

Signal	Pin			Description
	Name	PLCC	PQFP	
a0	a0/ad0/icp	4	42	**a**ddress bits **7**–**0**. Input. Mode 3. When the IA82527 is configured to operate in the 8-bit non-multiplexed non-Intel architecture mode (Mode 3), these lines provide the 8-bit address bus input to the device.
a1	a1/ad1/cp	3	41	
a2	a2/ad2/csas	2	40	
a3	a3/ad3/ste	43	37	
a4	a4/ad4/mosi	42	36	
a5	a5/ad5	41	35	
a6	a6/ad6/sclk	40	34	
a7	a7/ad7	39	33	
ad0	a0/ad0/icp	4	42	**a**ddress/**d**ata bits **15**–**0**. Input/Output. Mode 1. When the IA82527 is configured to operate in the 16-bit multiplexed Intel architecture mode (Mode 1), these lines provide the 16-bit address bus (input) and the 16-bit data bus (input/output) for the device.
ad1	a1/ad1/cp	3	41	
ad2	a2/ad2/csas	2	40	
ad3	a3/ad3/ste	43	37	
ad4	a4/ad4/mosi	42	36	
ad5	a5/ad5	41	35	
ad6	a6/ad6/sclk	40	34	
ad7	a7/ad7	39	33	
ad8	ad8/d0/p1.0	38	32	
ad9	ad9/d1/p1.1	37	31	
ad10	ad10/d2/p1.2	36	30	
ad11	ad11/d3/p1.3	35	29	
ad12	ad12/d4/p1.4	34	28	
ad13	ad13/d5/p1.5	33	27	
ad14	ad14/d6/p1.6	32	26	
ad15	ad15/d7/p1.7	31	25	

Table 3. Pin/Signal Descriptions *(Continued)*

Signal	Pin			Description
	Name	PLCC	PQFP	
ale	ale/as	5	43	**a**ddress **l**atch **e**nable. Input. Active High. Mode 0 and Mode 1. When the IA82527 is configured to operate in either the 8-bit multiplexed Intel architecture mode (Mode 0) or the 16-bit multiplexed Intel architecture mode (Mode 1), this signal latches the address into the device during the address phase of the bus cycle.
as	ale/as	5	43	**a**ddress **s**trobe. Input. Active High. Mode 2. When the IA82527 is configured to operate in the 8-bit multiplexed non-Intel architecture mode (Mode 2), this signal latches the address into the device during the address phase of the bus cycle. If the IA82527 is configured to operate in Mode 3 (8-bit non-multiplexed non-Intel architecture), this pin must be tied high.
clkout	clkout	27	21	**cl**oc**k out**. Output (push-pull). This output provides a programmable clock frequency. The frequency is set via the Clockout Register (1FH) and can range from the frequency of the **xtal** (crystal) input to xtal/n, where n can be an integer value from 2 through 15. This output allows the IA82527 to clock other devices such as the host CPU. **For 3.3V operation the crystal or external oscillator must run at <=12 MHz to produce clock output.**
cp	a1/ad1/cp	3	41	**c**lock **p**hase. Input. Serial Interface Mode. When this input is a logic 0, data is sampled on the rising edge of sclk. When this input is a logic 1, data is sampled on the falling edge of sclk.
cs_n	cs_n	8	2	**c**hip **s**elect. Input. Active Low (Modes 0–3); Selectable Active Level (Serial Interface Mode). When the IA82527 is configured to operate in one of the parallel interface modes (Modes 0–3) or the Serial Interface Mode, this input, during its active state, selects the device allowing CPU access. For Serial Interface Mode operation, the active state is selectable (i.e., either high or low) via the IA8257 csas pin.
csas	a2/ad2/csas	2	40	**c**hip **s**elect **a**ctive **s**tate. Input. Serial Interface Mode. When this input is a logic 0, the cs_n input is configured to function active low. When this input is a logic 1, the cs_n input is configured to function active high.

Table 3. Pin/Signal Descriptions *(Continued)*

Signal	Pin			Description
	Name	PLCC	PQFP	
d0	ad8/d0/p1.0	38	32	**d**ata bits **7**–**0**. Input/Output. Mode 3. When the IA82527 is configured to operate in the 8-bit non-multiplexed non-Intel architecture mode (Mode 3), these lines provide the 8-bit data bus to the device.
d1	ad9/d1/p1.1	37	31	
d2	ad10/d2/p1.2	36	30	
d3	ad11/d3/p1.3	35	29	
d4	ad12/d4/p1.4	34	28	
d5	ad13/d5/p1.5	33	27	
d6	ad14/d6/p1.6	32	26	
d7	ad15/d7/p1.7	31	25	
dsack0_n	dsack0_n	9	3	**d**ata and **s**ize **ack**nowledge **0**. Output. Active Low (open drain with active pull-up). Mode 3 (asynchronous operation). When the IA82527 is configured to operate in the 8-bit non-multiplexed non-Intel architecture mode (Mode 3), this signal functions as follows: when the CPU reads from the IA82527, **dsack0_n** active low indicates that the data is valid; when the CPU writes to the IA82527, **dsack0_n** active low indicates that the data has been received. Note: The active pull-up circuitry drives **dsack0_n** high for 10ns to raise it to a 3.0V voltage level. After that, an external pull up is required to pull **dsack0_n** the remainder of the way to V_{SS}.
e	rd_n/e	6	44	**e**nable. Input. Active High. Mode 3 (synchronous). When the IA82527 is configured to operate in the 8-bit non-multiplexed non-Intel architecture mode (Mode 3), this signal functions as follows: when the CPU reads from or writes to the IA82527, **e** active high indicates that the address is valid.
icp	a0/ad0/icp	4	42	**i**dle **c**lock **p**olarity. Input. Serial Interface Mode. When this input is a logic 0, the polarity for the idle state of sclk is low. When this input is a logic 1, the polarity for the idle state of sclk is high.

Table 3. Pin/Signal Descriptions *(Continued)*

Signal	Pin			Description
	Name	PLCC	PQFP	
int_n	int_n/ V_{CC}/2	24	18	**int**errupt. Output (open collector). Active Low. On the IA82527, two pins can provide the interrupt (**int_n**) output; however, depending on the setting of the MUX bit in the CPU Interface Register (02H), only one of the pins will serve as the source of **int_n** as follows: • PLCC Package: – When the MUX bit of the CPU Interface Register is 0, pin 24 functions as the **int_n** output and pin 11 functions as **p2.6**. – When the MUX bit of the CPU Interface Register is 1, pin 11 functions as the **int_n** output and pin 24 functions as V_{cc}/2. • PQFP Package: – When the MUX bit of the CPU Interface Register is 0, pin 18 functions as the **int_n** output and pin 5 functions as **p2.6**. – When the MUX bit of the CPU Interface Register is 1, pin 5 functions as the **int_n** output and pin 18 functions as V_{cc}/2.
	int_n/p2.6	11	5	
miso	ready/miso	28	22	**m**aster **i**n **s**lave **o**ut. Output (open drain). Serial Interface Mode. When the IA82527 is configured to operate with a serial interface, **miso** is the serial data output.

Table 3. Pin/Signal Descriptions *(Continued)*

Signal	Pin			Description
	Name	PLCC	PQFP	
mode0	mode0	44	38	**mode**N (N = **1** or **0**). Input. The logic levels at the **mode0** and **mode1** inputs determine the operating mode (i.e., interface type) of the IA82527 as follows: mode1 mode0 Interface Type 0 0 8-bit multiplexed Intel 0 1 16-bit multiplexed Intel 1 0 8-bit multiplexed non-Intel 1 1 8-bit Non-multiplexed non-Intel The **mode1** and **mode0** inputs are also used to establish the Serial Interface Mode as follows: when the IA82527 is reset, if • **mode1** = 0 • **mode0** = 0 • rd_n = 0 • wr_n = 0 the Serial Interface Mode will be selected. The **mode1** and **mode0** pins are internally connected to weak pull-downs. These pins will be pulled low during reset if unconnected. Following reset, these pins will float.
mode1	mode1	30	24	
mosi	a4/ad4/mosi	42	36	**m**aster **o**ut **s**lave **i**n. Input. Serial Interface Mode. When the IA82527 is configured to operate with a serial interface, **mosi** is the serial data input.

Table 3. Pin/Signal Descriptions *(Continued)*

Signal	Pin			Description
	Name	PLCC	PQFP	
p1.0	ad8/d0/p1.0	38	32	**p**ort **1**, bit N (N = **7**–**0**). Input/Output (general-purpose). Mode 0, Mode 2, and Serial Interface Mode. Port 1 bits **p1.7**–**p1.0** can be individually programmed as inputs or outputs. Programming is accomplished by writing to the P1CONF Register (9FH). The 8 bits of the P1CONF Register, P1CONF7–P1CONF0, correspond directly to pins **p1.7**–**p1.0**. Writing a 0 to a bit in the P1CONF Register causes the corresponding pin to be configured as a high-impedance input. Writing a 1 to a bit in the P1CONF Register causes the corresponding pin to be configured as a push-pull output. All Port 1 pins have weak pull-ups until the port is configured by writing to the P1CONF Register. The default value of the P1CONF Register following a reset is 00H. Data is read from Port 1 via the P1IN Register (BFH). A logic 0 for any bit in this register means that a logic 0 was read from the corresponding pin; a logic 1 for any bit means that a logic 1 was read from the corresponding pin. The default value of the P1IN Register following a reset is FFH. Data is written to Port 1 via the P1OUT Register (DFH). Writing a logic 0 to any bit in this register means that a logic 0 is written to the corresponding pin; writing a logic 1 to any bit means that a logic 1 is written to the corresponding pin. The default value of the P1OUT Register following a reset is 00H.
p1.1	ad9/d1/p1.1	37	31	
p1.2	ad10/d2/p1.2	36	30	
p1.3	ad11/d3/p1.3	35	29	
p1.4	ad12/d4/p1.4	34	28	
p1.5	ad13/d5/p1.5	33	27	
p1.6	ad14/d6/p1.6	32	26	
p1.7	ad15/d7/p1.7	31	25	

Table 3. Pin/Signal Descriptions *(Continued)*

Signal	Pin			Description
	Name	PLCC	PQFP	
p2.0	p2.0	17	11	**p**ort **2**, bit N (N = **7**–**0**). Input/Output. Port 2 bits **p2.7**–**p2.0**, can be individually programmed as inputs or outputs. Programming is accomplished by writing to the P2CONF Register (AFH). The 8 bits of the P2CONF Register, P2CONF7–P2CONF0, correspond directly to pins **p2.7**–**p2.0**. Writing a 0 to a bit in the P2CONF Register causes the corresponding pin to be configured as a high-impedance input. Writing a 1 to a bit in the P2CONF Register causes the corresponding pin to be configured as a push-pull output. All Port 2 pins have weak pull-ups until the port is configured by writing to the P2CONF Register. The default value of the P1CONF Register following a reset is 00H. Data is read from Port 2 via the P2IN Register (CFH). A logic 0 for any bit in this register means that a logic 0 was read from the corresponding pin; a logic 1 for any bit means that a logic 1 was read from the corresponding pin. The default value of the P2IN Register following a reset is FFH. Data is written to Port 2 via the P2OUT Register (EFH). Writing a logic 0 to any bit in this register means that a logic 0 is written to the corresponding pin; writing a logic 1 to any bit means that a logic 1 is written to the corresponding pin. The default value of the P2OUT Register following a reset is 00H. Two bits of Port 2 (P2.7 and P2.6) have alternate functions based on CPU interface mode. See Section 4.1.3 I/O Ports.
p2.1	p2.1	16	10	
p2.2	p2.2	15	9	
p2.3	p2.3	14	8	
p2.4	p2.4	13	7	
p2.5	p2.5	12	6	
p2.6	int_n/p2.6	11	5	
p2.7	wrh_n/p2.7	10	4	
rd_n	rd_n/e	6	44	**r**ea**d**. Input. Active Low. Mode 0 and Mode 1. When **rd_n** is asserted (low), it causes the IA82527 to drive the data from the location being read onto the data bus.
ready	ready/miso	28	22	**ready**. Output (open drain). Active High. Mode 0 and Mode 1. When ready is asserted (high), it signals the completion of a bus cycle. The ready output is provided to force system CPU wait states as required.

Table 3. Pin/Signal Descriptions *(Continued)*

Signal	Pin			Description
	Name	PLCC	PQFP	
reset_n	reset_n	29	23	**reset**. Input. Active Low. When the **reset_n** signal is asserted (low), the IA82527 is initialized. There are two reset situations: Cold reset is a power-on reset. As V_{CC} is driven to a valid level (power on), the **reset_n** signal must be driven low for a minimum of 1 ms measured from a valid V_{CC} level. No falling edge on the reset_n pin is required during a cold reset. For warm reset, V_{CC} remains at a valid level (i.e., power is already on and remains on) while **reset_n** is driven low for a minimum of 1 ms.
r-w_n	wr_n/wrl_n/r-w_n	7	1	**r**ead-**w**rite. Input. Active High (read)-Active Low (write). Mode 2 and Mode 3. When **r-w_n** is high, it signals a read cycle. When **r-w_n** is low, it signals a write cycle.
rx0	rx0	22	16	Receive (**rx**), lines **0** and **1**. Input. Pins **rx0** and **rx1** are the inputs to the IA82527 from the CAN bus lines. These pins connect internally to the receiver input comparator. Serial data from the CAN bus can be received using both **rx0** and **rx1** or by using only **rx0** as follows: • When the CoBy Bit in the Bus Configuration Register (2FH) is a 0, **rx0** and **rx1** are connected to the input comparator **rx0** is connected to the non-inverting input and **rx1** is connected to the inverting input). A recessive level is read when **rx0** > **rx1**. A dominant level is read when **rx1** > **rx0**. • When the CoBy Bit in the Bus Configuration Register (2FH) is a 1, input comparison is disabled, and **rx0**, which is still connected to the non-inverting input of the comparator, is the CAN bus line input. For this configuration, the DcR0 bit of the Bus Configuration Register must be a 0. After a cold reset (power on), the default configuration is the use of both **rx0** and **rx1** for the CAN bus input.
rx1	rx1	21	15	
sclk	a6/ad6/sclk	40	34	**s**erial **cl**oc**k**. Input. Serial Interface Mode. The **sclk** pin is the serial clock input to the IA82527 (slave device). The clock signal is provided by the master device.

Table 3. Pin/Signal Descriptions *(Continued)*

Signal	Pin			Description
	Name	PLCC	PQFP	
ste	a3/ad3/ste	43	37	**s**ynchronization **t**ransmission **e**nable. Input. Serial interface Mode. The logic level at the **ste** pin enables the transmission of the synchronization bytes through the IA82527 miso pin while the master device transmits the Address and Control Byte as follows: • When a logic 0 is placed on the **ste** pin, the synchronization bytes sent through the miso pin are 00H and 00H. • When a logic 1 is placed on the **ste** pin, the synchronization bytes sent through the miso pin are AAH and 55H. The IA82527 sends the synchronization bytes after the cs_n signal has been asserted
tx0	tx0	26	20	Transmit (**tx**), lines **0** and **1**. Output (push-pull). Pins **tx0** and **tx1** are the outputs from the IA82527 to the CAN bus lines. During a recessive bit, **tx0** is high and **tx1** is low. During a dominant bit, **tx0** is low and **tx1** is high.
tx1	tx1	25	19	
V_{CC}	V_{CC}	1	39	Power (**V_{CC}**). This pin provides power for the IA82527 device. It must be connected to a +5V DC power source.
$V_{CC}/2$	int_n/ $V_{CC}/2$	24	18	Reference Voltage, ISO Physical Layer (**$V_{CC}/2$**). Output. The **$V_{CC}/2$** pin provides a reference voltage for the ISO low-speed physical layer: • 2.38V DC (minimum) to 2.60V DC (maximum) (V_{CC} = +5.0V; $I_{OUT} \leq 75$ µA) • 1.46V DC (minimum) to 1.688V DC (maximum) (V_{CC} = +3.3V; $I_{OUT} \leq 75$ µA) This pin only functions as **$V_{CC}/2$** when the MUX bit of the CPU Interface Register (02H) is 1.
V_{SS1}	V_{SS1}	23	17	Ground, Digital (**V_{SS1}**). This pin provides the digital ground (0V) for the IA82527. It must be connected to a V_{SS} board plane.
V_{SS2}	V_{SS2}	20	14	Ground, Analog (**V_{SS2}**). This pin provides the ground (0V) for the IA82527 analog comparator. It must be connected to a V_{SS} board plane.
wr_n	wr_n/wrl_n/r-w_n	7	1	**wr**ite. Input. Active Low. Mode 0. When **wr_n** is asserted (low), it signals a write cycle.

Table 3. Pin/Signal Descriptions *(Continued)*

Signal	Pin			Description
	Name	PLCC	PQFP	
wrh_n	wrh_n/p2.7	10	4	**wr**ite **h**igh byte. Input. Active Low. Mode 1. When **wrh_n** is asserted (low), it signals a write cycle for the high byte of data (bits 15–8).
wrl_n	wr_n/wrl_n/r-w_n	7	1	**wr**ite **l**ow byte. Input. Active Low. Mode 1. When **wrl_n** is asserted (low), it signals a write cycle for the low byte of data (bits 7–0).
xtal1	xtal1	18	12	Crystal (**xtal**) **1**. Input. The **xtal1** pin is the input connection for an external crystal that drives the IA82527 internal oscillator. (When an external crystal is used, it is connected between this pin and the **xtal2** pin—see next table entry.) If an external oscillator or clock source is used to drive the IA82527 instead of a crystal, the **xtal1** pin is the input for this clock source.
xtal2	xtal2	19	13	Crystal (**xtal**) **2**. Output (push-pull). The **xtal2** pin is the output connection for an external crystal that drives the IA82527 internal oscillator. (When an external crystal is used, it is connected between this pin and the **xtal1** pin—see previous table entry.) If an external oscillator or clock source is used to drive the IA82527 instead of a crystal, **xtal2** must be left unconnected (i.e., must be floated). Additionally, the **xtal2** output must not be used as a clock source for other system components.

3. Maximum Ratings, Thermal Characteristics, and DC Parameters

For the Innovasic Semiconductor IA82527 Serial Communications Controller, the absolute maximum ratings, thermal characteristics, and DC parameters are provided in Tables 4 through 6, respectively.

Additionally, the DC parameters of the ISO Physical Layer are provided in Table 7.

Table 4. Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	−55°C to +150°C
Case Temperature under Bias	−40°C to +125°C
Supply Voltage with Respect to V_{SS}	−0.3V to +7.0V
Voltage on Pins other than Supply with Respect to V_{SS}	−0.3V to V_{DD} +0.3V

Table 5. Thermal Characteristics

Symbol	Characteristic	Value	Units
T_A	Ambient Temperature	-40°C to 125°C	°C
P_D	Power Dissipation	MHz × ICC × V/1000	W
Θ_{Ja}	44-Pin PLCC Package	30	°C/W
	44-Pin PQFP Package	38.4	
T_J	Average Junction Temperature	$T_A + (P_D \times \Theta_{Ja})$	°C

Table 6. DC Parameters

Symbol	Parameter	Min	Max	Units	Notes
V_{CC}	Supply Voltage	3.0	5.5	V	–
V_{IL}	Voltage, Input Low	–	0.8	V	All pins except XTAL1, rx0 for comparator bypass mode
V_{IL1}	Voltage, Input Low	–	0.3*V_{CC}	V	XTAL1, rx0 for comparator bypassed
V_{IH}	Voltage, Input High	2.4	–	V	reset_n hysteresis = 200mV All pins except XTAL1, rx0 for comparator bypass mode
V_{IH1}	Voltage, Input High	0.7* V_{CC}	–	V	XTAL1, rx0 for comparator bypassed
V_{OL}	Voltage, Output Low	–	0.45	V	ISO Physical Layer DC Parameters (see Table 7). All pins except tx0, tx1, XTAL2 , I_{OL} = 1.6 mA.
V_{OH}	Voltage, Output High	V_{CC} − 0.8	–	V	ISO Physical Layer DC Parameters tx0, tx1, XTAL2 (see Table 7). CLKOUT I_{OH} = −80 µA. All other I_{OH} pins = −200 µA.
I_{LEAK}	Input Leakage Current	–	±10	µA	$V_{SS} < V_{IN} < V_{CC}$
C_{IN}	Pin Capacitance	–	10	pF	$f_{CRYSTAL}$ = 1 KHz
I_{CC}	Supply Current	–	3	mA/MHz	$f_{CRYSTAL}$ = 16 MHz, all pins are driven to V_{SS} or V_{CC}
$I_{SLEEP-E}$	Sleep Current	–	800	µA	V_{CC}/2 enabled, no load
$I_{SLEEP-D}$	Sleep Current	–	150		V_{CC}/2 disabled
I_{PD}	Power-Down Current	–	25		xtal1 clocked, all pins driven to V_{SS} or V_{CC}

Table 7. ISO Physical Layer DC Parameters

Signal	Parameter	Min	Max	Units	Notes
rx0 & rx1, tx0 & tx1	Input Voltage	−0.5	V_{CC} + 0.5	V	–
	Common Mode Range	V_{ss} + 1.0	V_{CC} − 1.0	V	–
	Differential Input Threshold	±100	–	mV	–
	Delay 1: receive comparator input delay + tx0/tx1 output delay	–	60 **(@5.0V)** 110 **(@3.3V)**	ns ns	Load on tx0/tx1 = 100 pF, rx0/rx1 differential = +100 mV to −100 mV
	Delay 2: rx0 pin delay (comparator bypassed) + tx0/tx1 output delay	–	50 **(@5.0V)** 60 **(@3.3V)**	ns ns	Load on tx0/tx1 = 100 pF
	Source Current on tx0, tx1	−10	–	mA	V_{OUT} = V_{CC} − 1.0 V
	Sink Current on tx0, tx1	10	–	mA	V_{OUT} = 1.0 V
	Input Hysteresis for rx0/rx1	–	0	V	–
V_{CC}/2	Reference Voltage	2.38	2.62	V	I_{OUT} ≤ 75 µA, V_{CC} = **5.0 V**
		1.46	1.688	V	I_{OUT} ≤ 75 µA, V_{CC} = **3.3 V**
All ratings listed are for the temperature range T_A = −40°C to +125°C (V_{CC} = 5V ± 10%) or (V_{CC} = 3.0 -3.6V).					

4. Functional Description

4.1 Hardware Architecture

A block diagram of the IA82527 CAN Serial Communications Controller is shown in Figure 5. The primary architectural features of the device are as follows:

- CAN Controller
- Message RAM
- CPU Interface
- I/O Ports
- Programmable Clock Output

These features are briefly described in the following subsections.

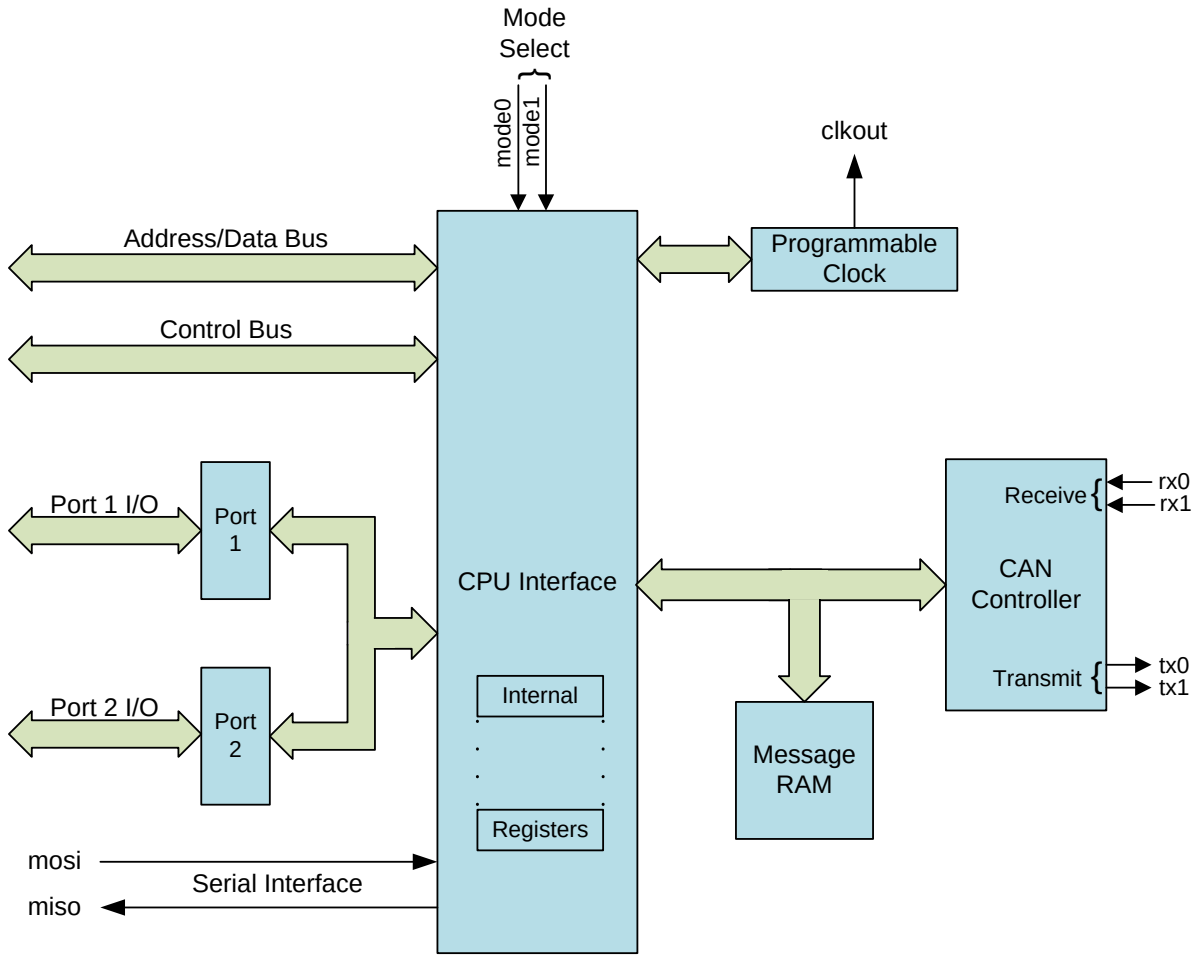


Figure 5. Functional Block Diagram

4.1.1 CAN Controller

The CAN Controller block of the IA82527 supports the interface to the CAN Bus via the rx0, rx1, tx0, and tx1 lines. The CAN Controller manages the transceiver logic, error management logic, and the message objects, controlling the data stream between the Message RAM (parallel data) and the CAN Bus (serial data).

4.1.2 Message RAM

The Message RAM block of the IA82527 provides the interface buffer between the system CPU and the CAN Bus. The IA82527 Message RAM provides storage for 15 message objects of 8-byte data length. The Message RAM is Dual Port RAM allowing the CPU and the CAN controller simultaneous access to the Message RAM.

4.1.3 CPU Interface

The IA82527 is can be interfaced to many commonly used microcontrollers. There are four parallel interface options and a serial interface option.

Different interface options, or modes, are selected using interface mode pins, mode1 and mode0. The parallel interface modes that can be selected are as follows:

- 8-bit Intel multiplexed address and data buses
- 16-bit Intel multiplexed address and data buses
- 8-bit non- Intel multiplexed address and data buses
- 8-bit non-multiplexed address and data buses

The serial interface mode is fully compatible with the Motorola® SPI protocol and will interface to most commonly used serial interfaces. The serial interface is implemented in slave mode only, and responds to the master using the specially designed serial interface protocol. The serial interface mode interconnection scheme is shown in Figure 6.

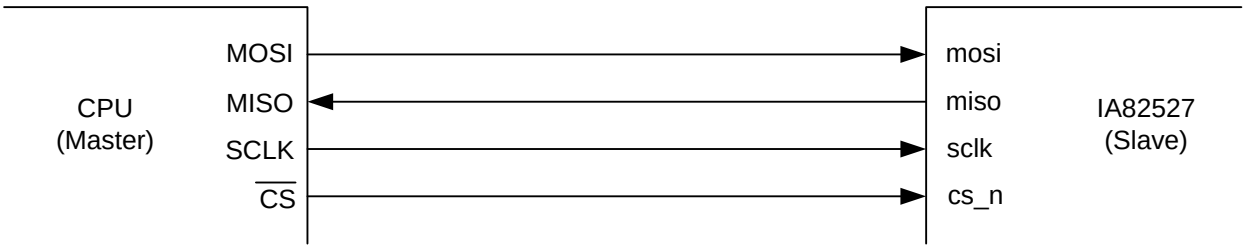


Figure 6. mosi/miso Connection

4.1.3 I/O Ports

The IA82527 contains two 8-bit General Purpose Input Output (GPIO) ports. Each GPIO port is selectable or programmable as either an input or an output. CPU interface modes may use some of the GPIO pins or signals, precluding their use as GPIO. Six bits of GPIO Port 2 (p2.5 to p2.0) are always available as GPIO. GPIO Port 2 bits 6 and 7 (p2.6 and p2.7) have alternate functions as the alternate source for int_n and as the wrh_n input for CPU mode 2 and may be available as GPIO depending on the CPU mode. GPIO Port 1 is available for use as GPIO in CPU modes 0, 2, and SPI and is not available in CPU modes 1 and 3.

4.1.4 Programmable Clock Output

Using an oscillator, clock divider register, and a driver circuit, the IA82527 provides a programmable clock output. The output frequency range available is from the external crystal frequency to that frequency divided by 15. The clock output allows the IA82527 to drive other devices such as the host CPU. The slew rate of the clkout signal is selectable via the CLKOUT Register (1FH).

4.2 Address Map

The IA82527 includes 256 8-bit locations that provide device configuration registers and message storage. The address map is shown in Table 8.

4.3 CAN Message Objects

Each CAN message object has a unique identifier and can be configured as either transmit or receive, except for message object 15. Message object 15 is a double-buffered receive-only buffer with a special mask design to allow select groups of different message identifiers to be received. Each message object contains registers for control and status bits.

All message objects have separate transmit and receive interrupts and status bits that allow the host CPU to determine when a message frame has been sent or received. The IA82527 implements a global masking feature that allows the user to globally mask any identifier bits of the incoming message. This mask is programmable, which permits application-specific message identification.

The Message Object Structure is shown in Table 9.

Table 8. Address Map

Address	Register/Message
00H	Control Register
01H	Status Register
02H	CPU Interface Register
03H	Reserved
04–05H	High-Speed Read Register
06–07H	Global Mask—Standard
08–0BH	Global Mask—Extended
0C-0FH	Message 15 Mask
10–1EH	Message 1
1FH	CLKOUT Register
20–2EH	Message 2
2FH	Bus Configuration Register
30–3EH	Message 3
3FH	Bit Timing Register 0
40–4EH	Message 4
4FH	Bit Timing Register 1
50–5EH	Message 5
5FH	Interrupt Register
60–6EH	Message 6
6FH	Reserved
70H–7EH	Message 7
7FH	Reserved
80–8EH	Message 8
8FH	Reserved
90–9EH	Message 9
9FH	P1CONF Register
A0–AEH	Message 10
AFH	P2CONF Register
B0–BEH	Message 11
BFH	P1IN Register
C0–CEH	Message 12
CFH	P2IN Register
D0–DEH	Message 13
DFH	P1OUT Register
E0–EEH	Message 14
EFH	P2OUT Register
F0–FEH	Message 15
FFH	Serial Reset Address Register

Table 9. Message Object Structure

Offset (Base Address +n)	Message Component
+0	Control Register 0
+1	Control Register 1
+2	Arbitration Register 0
+3	Arbitration Register 1
+4	Arbitration Register 2
+5	Arbitration Register 3
+6	Message Configuration Register
+7	Data Byte 0
+8	Data Byte 1
+9	Data Byte 2
+10	Data Byte 3
+11	Data Byte 4
+12	Data Byte 5
+13	Data Byte 6
+14	Data Byte 7

5. AC Specifications

The AC characteristics of the IA82527 are provided in the figures and tables of this chapter.

The IA82527 can be configured to operate in the following parallel and serial CPU interface modes:

- Mode 0: 8-Bit Multiplexed Intel Architecture
- Mode 1: 16-Bit Multiplexed Intel Architecture
- Mode 2: 8-Bit Multiplexed Non-Intel Architecture
- Mode 3: 8-Bit Non-Multiplexed Non-Intel Architecture
- Serial Interface Mode

The AC characteristics of these modes in operation are provided as follows:

- Mode 0 and Mode 1: General Bus Timing (Tables 10 and 11/Figure 7)
- Mode 0 and Mode 1: Ready Timing for Read Cycle (Table 10 and 11/Figure 8)
- Mode 0 and Mode 1: Ready Timing for Write Cycle with No Write Pending (Table 10 and 11/Figure 9)
- Mode 0 and Mode 1: Ready Timing for Write Cycle with Write Pending (Table 10 and 11/Figure 10)
- Mode 2: General Bus Timing (Table 12 and 13/Figure 11)
- Mode 3: Asynchronous Operation, Read Cycle (Table 14 and 15/Figure 12)
- Mode 3: Asynchronous Operation, Write Cycle (Table 14 and 15/Figure 13)
- Mode 3: Synchronous Operation, Read Cycle (Table 16 and 17/Figure 14)
- Mode 3: Synchronous Operation, Write Cycle (Table 16 and 17/Figure 15)
- Serial Interface Mode: icp = 0 and cp = 0 (Table 18 and 19/Figure 16)
- Serial Interface Mode: icp = 1 and cp = 1 (Table 18 and 19/Figure 17)

Table 10. Mode 0 and Mode 1: General Bus and Ready Timing for 5.0V Operation

Symbol	Parameter	Minimum	Maximum
$1/t_{XTAL}$	Oscillator Frequency	8 MHz	16 MHz
$1/t_{SCLK}$	System Clock Frequency	4 MHz	10 MHz
$1/t_{MCLK}$	Memory Clock Frequency	2 MHz	8 MHz
t_{AVLL}	Address Valid to ale Low	7.5 ns	–
t_{LLAX}	Address Hold after ale Low	10 ns	–
t_{LHLL}	ale High Time	30 ns	–
t_{LLRL}	ale Low to rd_n Low	20 ns	–
t_{CLLL}	cs_n Low to ale Low	10 ns	–
t_{QVWH}	Data Setup to wr_n or wrh_n High	27 ns	–
t_{WHQX}	Input Data Hold after wr_n or wrh_n High	10 ns	–
t_{WLWH}	wr_n or wrh_n Pulse Width	30 ns	–
t_{WHLH}	wr_n or wrh_n High to Next ale High	8 ns	–
t_{WHCH}	wr_n or wrh_n High to cs_n High	0 ns	–
t_{RLRH}	rd_n Pulse Width. This time is long enough to initiate a double read cycle by loading the High Speed Registers (04H, 05H), but is too short to read from 04H and 05H (see t_{RLDV}).	40 ns	–
t_{RLDV}	rd_n Low to Data Valid (only for Registers 02H, 04H, 05H)	0 ns	55 ns
t_{RLDV1}	rd_n Low Data to Data Valid (for all Registers except 02H, 04H, 05H) for Read Cycle without a Previous Write[a]	–	1.5 t_{MCLK} + 100 ns
t_{RLDV1}	rd_n Low Data to Data Valid (for all Registers except 02H, 04H, 05H) for Read Cycle with a Previous Write	–	3.5 t_{MCLK} + 100 ns
t_{RHDZ}	Data Float after rd_n High	0 ns	45 ns
t_{CLYV}	cs_n Low to ready Setup (Load Capacitance on the ready Output = 50 pF, V_{OL} = 1.0 V)	–	32 ns
	cs_n Low to ready Setup (Load Capacitance on the ready Output = 50 pF, V_{OL} = 0.45 V)	–	40 ns
t_{WLYZ}	wr_n or wrh_n Low to ready Float for a Write Cycle if No Previous Write is Pending	–	145 ns
t_{HYZ}	End of Last Write to ready Float for a Write Cycle if a Previous Write Cycle is Active[b]	–	2 t_{MCLK} + 100 ns
t_{RLYZ}	rd_n Low to ready Float (for all registers except 02H, 04H, 05H) for Read Cycle without a Previous Write[a]	–	2 t_{MCLK} + 100 ns
t_{RLYZ}	rd_n Low to ready Float (for all registers except 02H, 04H, 05H) for Read Cycle with a Previous Write	–	4 t_{MCLK} + 100 ns
t_{WHDV}	wr_n or wrh_n High to Output Data Valid on Port 1 or Port 2	t_{MCLK}	2 t_{MCLK} + 500 ns
t_{COPO}	clkout Period (CD_V is the value loaded in the CLKOUT Register representing the clkout divisor)	(CD_V + 1) × t_{OSC}	–
t_{CHCL}	clkout High Period (CD_V is the value loaded in the CLKOUT Register representing the clkout divisor)	(CD_V + 1) × ½ t_{OSC} – 10	(CD_V + 1) × ½ t_{OSC} + 15

[a]A "Read Cycle without a Previous Write" is where a read cycle follows a write cycle and there is greater than 2×t_{MCLK} between the rising edge of wr_n or wrh_n and the falling edge of rd_n.
[b]A "Previous Write Cycle is Active" is where the rising edge of wr_n or wrh_n for the second write is less than 2×t_{MCLK} after the rising edge of wr_n or wrh_for the first write.

Table 11. Mode 0 and Mode 1: General Bus and Ready Timing for 3.3V Operation

Symbol	Parameter	Minimum	Maximum
$1/t_{XTAL}$	Oscillator Frequency	8 MHz	16 MHz
$1/t_{SCLK}$	System Clock Frequency	4 MHz	10 MHz
$1/t_{MCLK}$	Memory Clock Frequency	2 MHz	8 MHz
t_{AVLL}	Address Valid to ale Low	7.5 ns	–
t_{LLAX}	Address Hold after ale Low	10 ns	–
t_{LHLL}	ale High Time	30 ns	–
t_{LLRL}	ale Low to rd_n Low	20 ns	–
t_{CLLL}	cs_n Low to ale Low	10 ns	–
t_{QVWH}	Data Setup to wr_n or wrh_n High	27 ns	–
t_{WHQX}	Input Data Hold after wr_n or wrh_n High	10 ns	–
t_{WLWH}	wr_n or wrh_n Pulse Width	30 ns	–
t_{WHLH}	wr_n or wrh_n High to Next ale High	8 ns	–
t_{WHCH}	wr_n or wrh_n High to cs_n High	0 ns	–
t_{RLRH}	rd_n Pulse Width. This time is long enough to initiate a double read cycle by loading the High Speed Registers (04H, 05H), but is too short to read from 04H and 05H (see t_{RLDV}).	40 ns	–
t_{RLDV}	rd_n Low to Data Valid (only for Registers 02H, 04H, 05H)	0 ns	75 ns
t_{RLDV1}	rd_n Low Data to Data Valid (for all Registers except 02H, 04H, 05H) for Read Cycle without a Previous Write[a]	–	1.5 t_{MCLK} + 100 ns
t_{RLDV1}	rd_n Low Data to Data Valid (for all Registers except 02H, 04H, 05H) for Read Cycle with a Previous Write	–	3.5 t_{MCLK} + 100 ns
t_{RHDZ}	Data Float after rd_n High	0 ns	50 ns
t_{CLYV}	cs_n Low to ready Setup (Load Capacitance on the ready Output = 50 pF, V_{OL} = 1.0 V)	–	32 ns
	cs_n Low to ready Setup (Load Capacitance on the ready Output = 50 pF, V_{OL} = 0.45 V)	–	40 ns
t_{WLYZ}	wr_n or wrh_n Low to ready Float for a Write Cycle if No Previous Write is Pending	–	145 ns
HYZ	End of Last Write to ready Float for a Write Cycle if a Previous Write Cycle is Active[b]	–	2 t_{MCLK} + 100 ns
t_{RLYZ}	rd_n Low to ready Float (for all registers except 02H, 04H, 05H) for Read Cycle without a Previous Write[a]	–	2 t_{MCLK} + 100 ns
t_{RLYZ}	rd_n Low to ready Float (for all registers except 02H, 04H, 05H) for Read Cycle with a Previous Write	–	4 t_{MCLK} + 100 ns
t_{WHDV}	wr_n or wrh_n High to Output Data Valid on Port 1 or Port 2	t_{MCLK}	2 t_{MCLK} + 500 ns
t_{COPO}	clkout Period (CD_V is the value loaded in the CLKOUT Register representing the clkout divisor)	(CD_V + 1) × t_{OSC}	–
t_{CHCL}	clkout High Period (CD_V is the value loaded in the CLKOUT Register representing the clkout divisor)	(CD_V + 1) × ½ t_{OSC} – 10	(CD_V + 1) × ½ t_{OSC} + 15

[a]A "Read Cycle without a Previous Write" is where a read cycle follows a write cycle and there is greater than 2×t_{MCLK} between the rising edge of wr_n or wrh_n and the falling edge of rd_n.
[b]A "Previous Write Cycle is Active" is where the rising edge of wr_n or wrh_n for the second write is less than 2×t_{MCLK} after the rising edge of wr_n or wrh_for the first write.

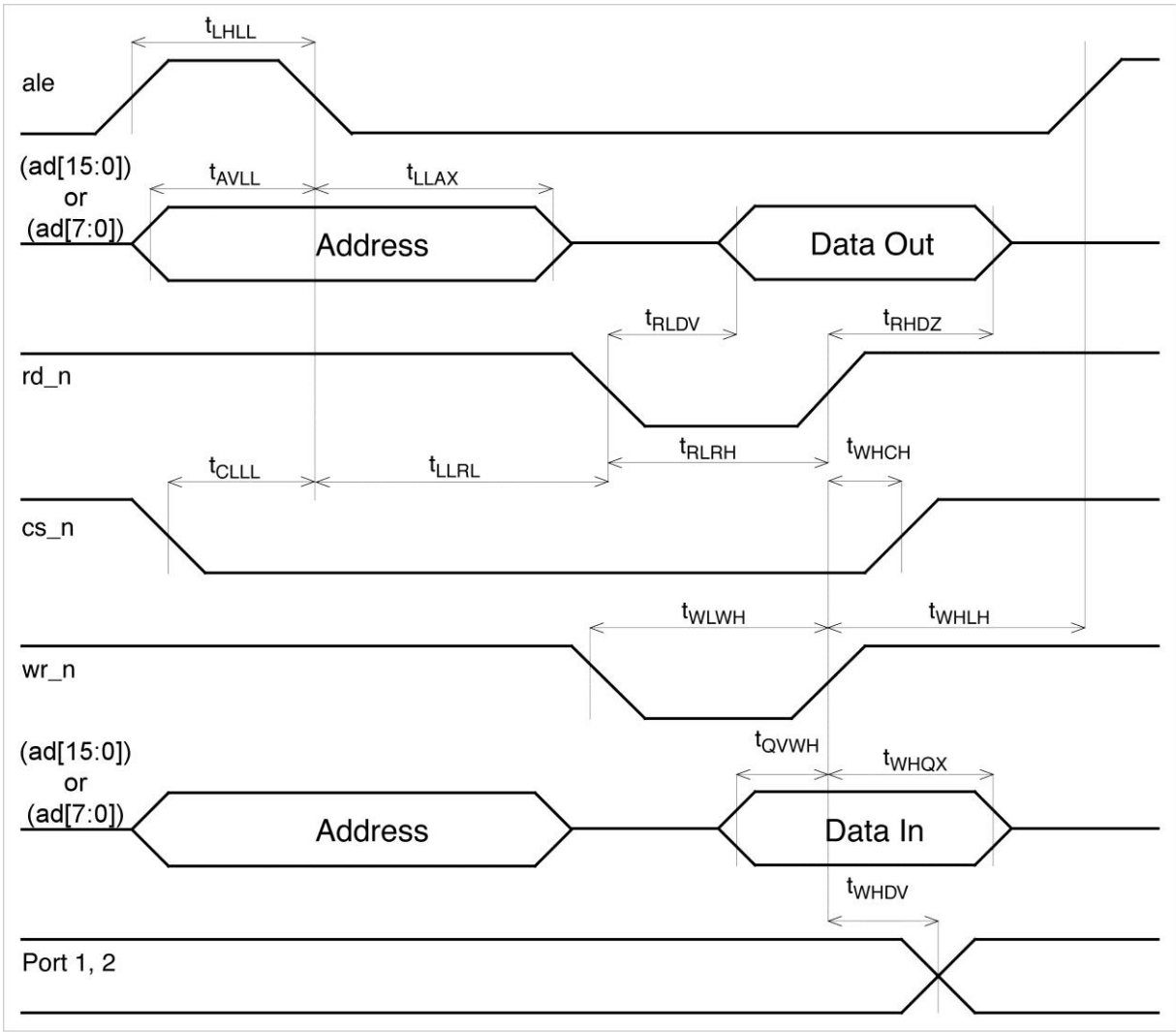


Figure 7. Mode 0 and Mode 1: General Bus Timing

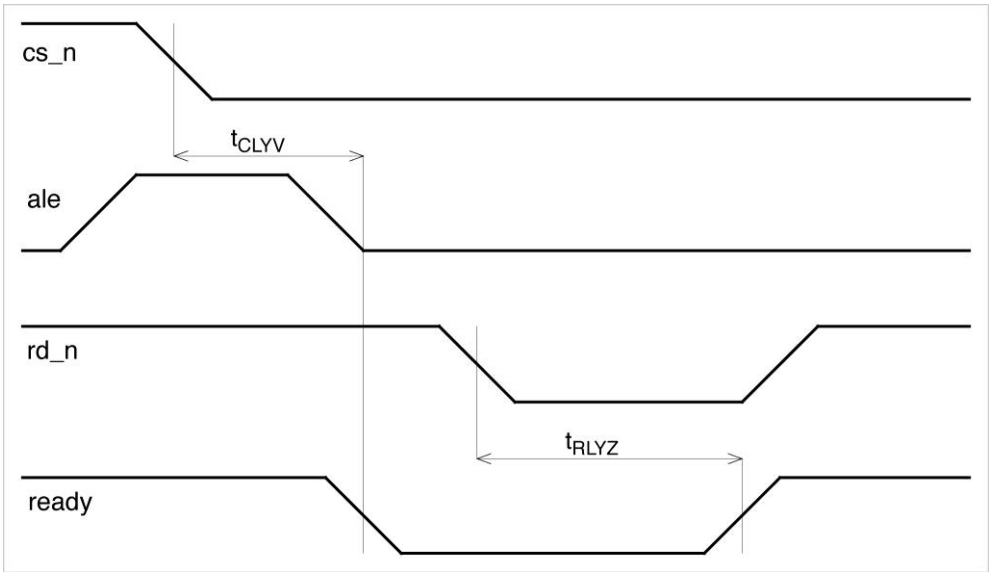


Figure 8. Mode 0 and Mode 1: Ready Timing for Read Cycle

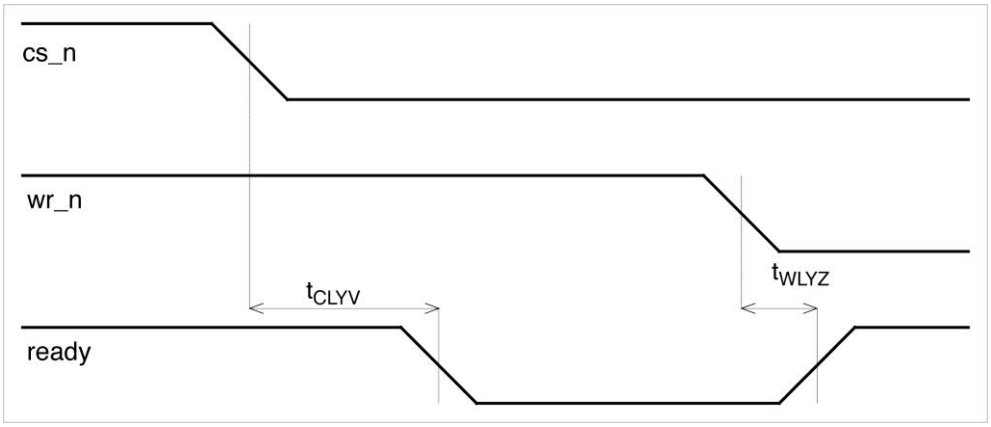


Figure 9. Mode 0 and Mode 1: Ready Timing for Write Cycle with No Write Pending

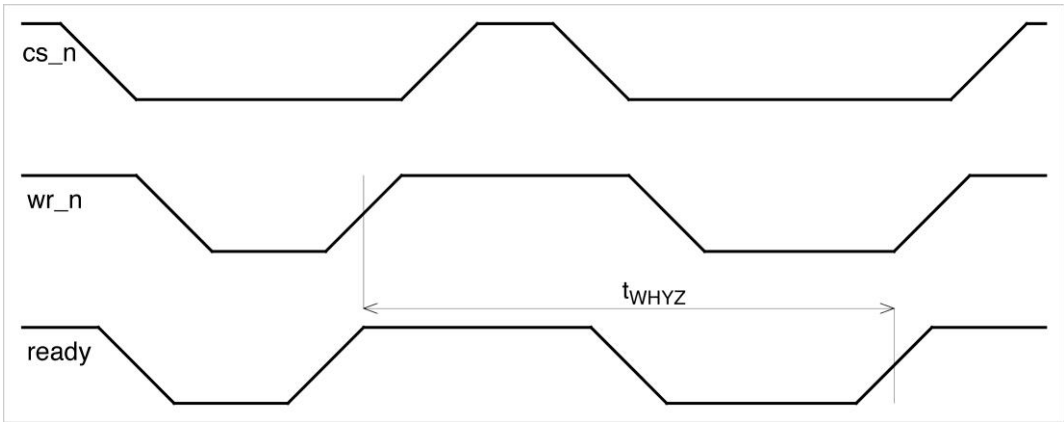


Figure 10. Mode 0 and Mode 1: Ready Timing for Write Cycle with Write Active

Table 12. Mode 2: General Bus Timing for 5.0V Operation

Symbol	Parameter	Minimum	Maximum
$1/t_{XTAL}$	Oscillator Frequency	8 MHz	16 MHz
$1/t_{SCLK}$	System Clock Frequency	4 MHz	10 MHz
$1/t_{MCLK}$	Memory Clock Frequency	2 MHz	8 MHz
t_{AVSL}	Address Valid to as Low	7.5 ns	–
t_{SLAX}	Address Hold after as Low	10 ns	–
t_{ELDZ}	Data Float after e Low	0 ns	45 ns
t_{EHDV}	e High to Data Valid for Registers 02H, 04H, 05H	0 ns	45 ns
	e High to Data Valid (all Registers except for 02H, 04H, 05H) for Read Cycle without a Previous Write[a]	–	1.5 t_{mclk} + 100 ns
	e High to Data Valid (all Registers except for 02H, 04H, 05H) for Read Cycle with a Previous Write	–	3.5 t_{mclk} + 100 ns
t_{QVEL}	Data Setup to e Low	30 ns	–
t_{ELQX}	Input Data Hold after e Low	20 ns	–
t_{ELDV}	e Low to Output Data Valid on Port 1/2	t_{mclk}	2 t_{mclk} + 500 ns
t_{EHEL}	e High Time	45 ns	
t_{ELEL}	End of previous write (Last E Low) to E Low for Write Cycle	2 t_{mclk}	
t_{SHSL}	as High Time	30 ns	–
t_{RSEH}	Setup Time of r-w_n to e High	30 ns	–
t_{SLEH}	as Low to e High	20 ns	–
t_{CLSL}	cs_n Low to as Low	20 ns	–
t_{ELCH}	e Low to cs_n High	0 ns	–
t_{COPD}	clkout Period (CD_V is the value loaded in the CLKOUT Register representing the clkout divisor)	$(CD_V + 1) \times t_{OSC}$	
t_{CHCL}	clkout High Period (CD_V is the value loaded in the CLKOUT Register representing the clkout divisor)	$(CD_V + 1) \times ½$ $t_{OSC} - 10$	$(CD_V + 1) \times ½$ $t_{OSC} + 15$

[a]A “Read Cycle without a Previous Write” is where a read cycle follows a write cycle and where the falling edge of e for the write and the rising edge of e for the read are separated by at least $2 \times t_{MCLK}$.

Table 13. Mode 2: General Bus Timing for 3.3V Operation

Symbol	Parameter	Minimum	Maximum
$1/t_{XTAL}$	Oscillator Frequency	8 MHz	16 MHz
$1/t_{SCLK}$	System Clock Frequency	4 MHz	10 MHz
$1/t_{MCLK}$	Memory Clock Frequency	2 MHz	8 MHz
t_{AVSL}	Address Valid to as Low	7.5 ns	–
t_{SLAX}	Address Hold after as Low	10 ns	–
t_{ELDZ}	Data Float after e Low	0 ns	45 ns
t_{EHDV}	e High to Data Valid for Registers 02H, 04H, 05H	0 ns	45 ns
	e High to Data Valid (all Registers except for 02H, 04H, 05H) for Read Cycle without a Previous Write[a]	–	1.5 t_{mclk} + 100 ns
	e High to Data Valid (all Registers except for 02H, 04H, 05H) for Read Cycle with a Previous Write	–	3.5 t_{mclk} + 100 ns
t_{QVEL}	Data Setup to e Low	30 ns	–
t_{ELQX}	Input Data Hold after e Low	20 ns	–
t_{ELDV}	e Low to Output Data Valid on Port 1/2	t_{mclk}	2 t_{mclk} + 500 ns
t_{EHEL}	e High Time	45 ns	
t_{ELEL}	End of previous write (Last E Low) to E Low for Write Cycle	2 t_{mclk}	
t_{SHSL}	as High Time	30 ns	–
t_{RSEH}	Setup Time of r-w_n to e High	30 ns	–
t_{SLEH}	as Low to e High	20 ns	–
t_{CLSL}	cs_n Low to as Low	20 ns	–
t_{ELCH}	e Low to cs_n High	0 ns	–
t_{COPD}	clkout Period (CD_V is the value loaded in the CLKOUT Register representing the clkout divisor)	$(CD_V + 1) \times t_{OSC}$	
t_{CHCL}	clkout High Period (CD_V is the value loaded in the CLKOUT Register representing the clkout divisor)	$(CD_V + 1) \times ½$ $t_{OSC} - 10$	$(CD_V + 1) \times ½$ $t_{OSC} + 15$

[a]A “Read Cycle without a Previous Write” is where a read cycle follows a write cycle and where the falling edge of e for the write and the rising edge of e for the read are separated by at least $2 \times t_{MCLK}$.

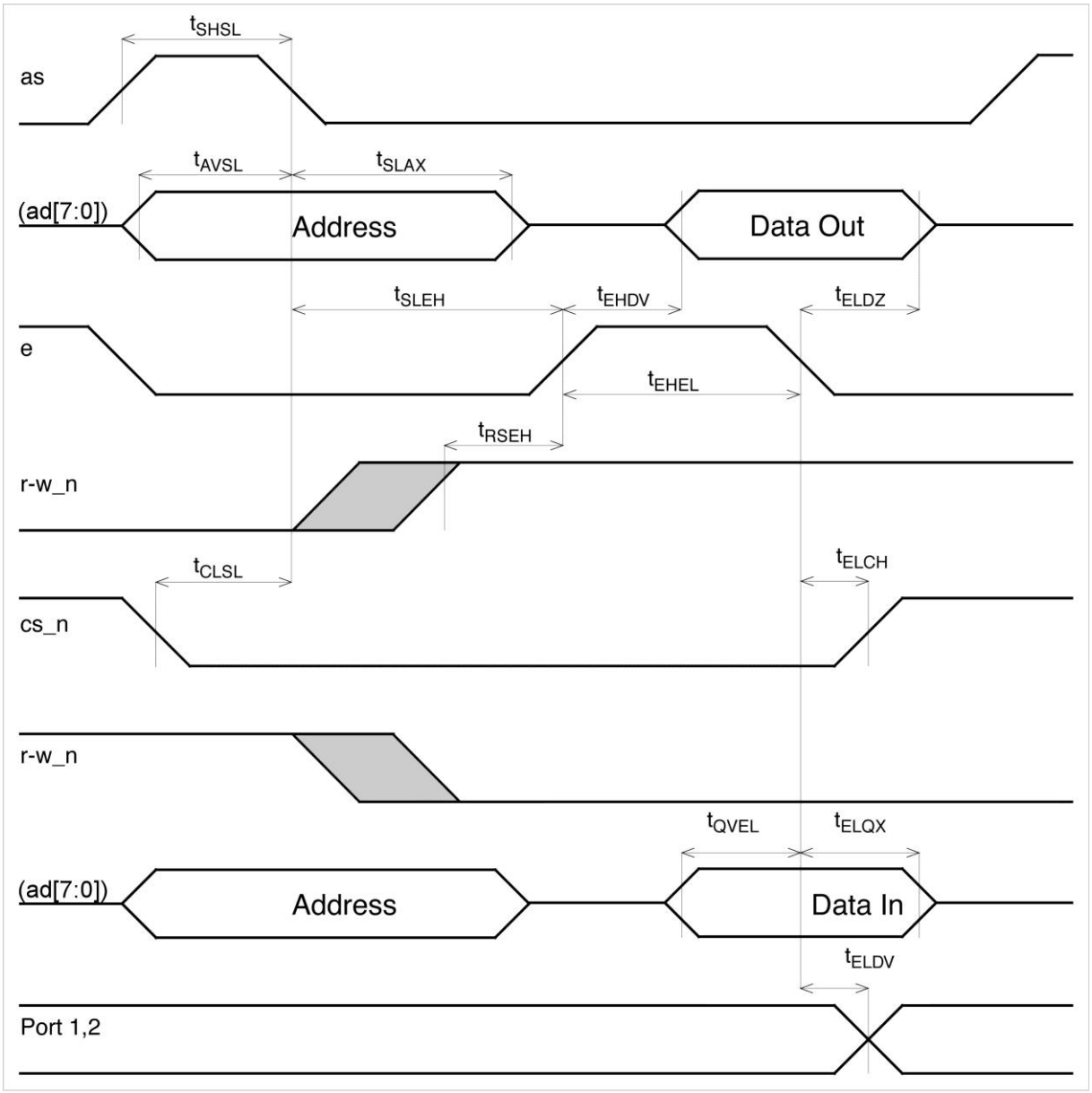


Figure 11. Mode 2: General Bus Timing

Table 14. Mode 3: Asynchronous Operation Timing for 5.0V Operation

Symbol	Parameter	Minimum	Maximum
$1/t_{XTAL}$	Oscillator Frequency	8 MHz	16 MHz
$1/t_{SCLK}$	System Clock Frequency	4 MHz	10 MHz
$1/t_{MCLK}$	Memory Clock Frequency	2 MHz	8 MHz
t_{AVCL}	Address or r-w_n Valid to cs_n Low Setup	3 ns	–
t_{CLDV}	cs_n Low to Data Valid (for High-Speed Registers 02H, 04H, and 05H)	0 ns	55 ns
	cs_n Low to Data Valid (for Low-Speed Registers) Read Cycle without Previous Write[a]	0 ns	1.5 t_{MCLK} + 100 ns
	cs_n Low to Data Valid (for Low-Speed Registers) Read Cycle with Previous Write	0 ns	3.5 t_{MCLK} + 100 ns
t_{KLDV}	dsack0_n Low to Output Data Valid (for High-Speed Read Registers)	–	23 ns
	dsack0_n Low to Output Data Valid (for Low-Speed Read Registers)	0 ns	–
t_{CHDV}	Input Data Hold after cs_n High	15 ns	–
t_{CHDH}	Output Data Hold after cs_n High	0 ns	–
t_{CHDZ}	cs_n High to Output Data Float	–	35 ns
t_{CHKH_1}	cs_n High to dsack0_n = 2.4V (an on-chip pull-up will drive dsack0_n to approximately 2.4V; an external pull-up is required to drive this signal to a higher voltage)	0 ns	55 ns
t_{CHKH_2}	cs_n High to dsack0_n = 2.8V	–	150 ns
t_{CHKZ}	cs_n High to dsack0_n Float	0 ns	100 ns
t_{CHCL}	cs_n Width between Successive Cycles	25 ns	–
t_{CHAI}	cs_n High to Address Invalid	7 ns	–
t_{CHRI}	cs_n High to r-w_n Invalid	5 ns	–
t_{CLCH}	cs_n Width Low	65 ns	–
t_{DVCH}	CPU Write Data Valid to cs_n High	20 ns	–
t_{CLKL}	cs_n Low to dsack0_n Low (for High- and Low-Speed Registers) Write Cycle without Previous Write	0 ns	67 ns
t_{CHKL}	End of Previous Write (cs_n High) to dsack0_n Low for a Write Cycle with a Previous Write[b]	0 ns	2 t_{MCLK} + 145 ns
t_{COPD}	clkout Period (CD_V is the value loaded in the CLKOUT Register representing the clkout divisor)	(CD_V + 1) × t_{OSC}	
t_{CHCL}	clkout High Period (CD_V is the value loaded in the CLKOUT Register representing the clkout divisor)	(CD_V + 1) × ½ t_{OSC} – 10	(CD_V + 1) × ½ t_{OSC} + 15

[a] A "Read Cycle without Previous Write" is where a read cycle follows a write cycle and where the rising edge of cs_n for the write and the falling edge of cs_n for the read are separated by at least 2 × t_{MCLK}.
[b] A "Write Cycle with a Previous Write" is a write cycle following a previous write cycle where the rising edge of cs_n for the first write and the rising edge of cs_n for the second write are separated by at least 2 × t_{MCLK}.

Table 15. Mode 3: Asynchronous Operation Timing for 3.3V Operation

Symbol	Parameter	Minimum	Maximum
$1/t_{XTAL}$	Oscillator Frequency	8 MHz	16 MHz
$1/t_{SCLK}$	System Clock Frequency	4 MHz	10 MHz
$1/t_{MCLK}$	Memory Clock Frequency	2 MHz	8 MHz
t_{AVCL}	Address or r-w_n Valid to cs_n Low Setup	3 ns	–
t_{CLDV}	cs_n Low to Data Valid (for High-Speed Registers 02H, 04H, and 05H)	0 ns	60 ns
	cs_n Low to Data Valid (for Low-Speed Registers) Read Cycle without Previous Write[a]	0 ns	1.5 t_{MCLK} + 100 ns
	cs_n Low to Data Valid (for Low-Speed Registers) Read Cycle with Previous Write	0 ns	3.5 t_{MCLK} + 100 ns
t_{KLDV}	dsack0_n Low to Output Data Valid (for High-Speed Read Registers)	–	35 ns
	dsack0_n Low to Output Data Valid (for Low-Speed Read Registers)	0 ns	–
t_{CHDV}	Input Data Hold after cs_n High	15 ns	–
t_{CHDH}	Output Data Hold after cs_n High	0 ns	–
t_{CHDZ}	cs_n High to Output Data Float	–	35 ns
t_{CHKH_1}	cs_n High to dsack0_n = 2.4V (an on-chip pull-up will drive dsack0_n to approximately 2.4V; an external pull-up is required to drive this signal to a higher voltage)	0 ns	55 ns
t_{CHKH_2}	cs_n High to dsack0_n = 2.8V	–	150 ns
t_{CHKZ}	cs_n High to dsack0_n Float	0 ns	100 ns
t_{CHCL}	cs_n Width between Successive Cycles	25 ns	–
t_{CHAI}	cs_n High to Address Invalid	7 ns	–
t_{CHRI}	cs_n High to r-w_n Invalid	6.5 ns	–
t_{CLCH}	cs_n Width Low	65 ns	–
t_{DVCH}	CPU Write Data Valid to cs_n High	20 ns	–
t_{CLKL}	cs_n Low to dsack0_n Low (for High- and Low-Speed Registers) Write Cycle without Previous Write	0 ns	67 ns
t_{CHKL}	End of Previous Write (cs_n High) to dsack0_n Low for a Write Cycle with a Previous Write[b]	0 ns	2 t_{MCLK} + 145 ns
t_{COPD}	clkout Period (CD_V is the value loaded in the CLKOUT Register representing the clkout divisor)	(CD_V + 1) × t_{OSC}	
t_{CHCL}	clkout High Period (CD_V is the value loaded in the CLKOUT Register representing the clkout divisor)	(CD_V + 1) × ½ t_{OSC} – 10	(CD_V + 1) × ½ t_{OSC} + 15

[a]A "Read Cycle without Previous Write" is where a read cycle follows a write cycle and where the rising edge of cs_n for the write and the falling edge of cs_n for the read are separated by at least 2 × t_{MCLK}.
[b]A "Write Cycle with a Previous Write" is a write cycle following a previous write cycle where the rising edge of cs_n for the first write and the rising edge of cs_n for the second write are separated by at least 2 × t_{MCLK}.

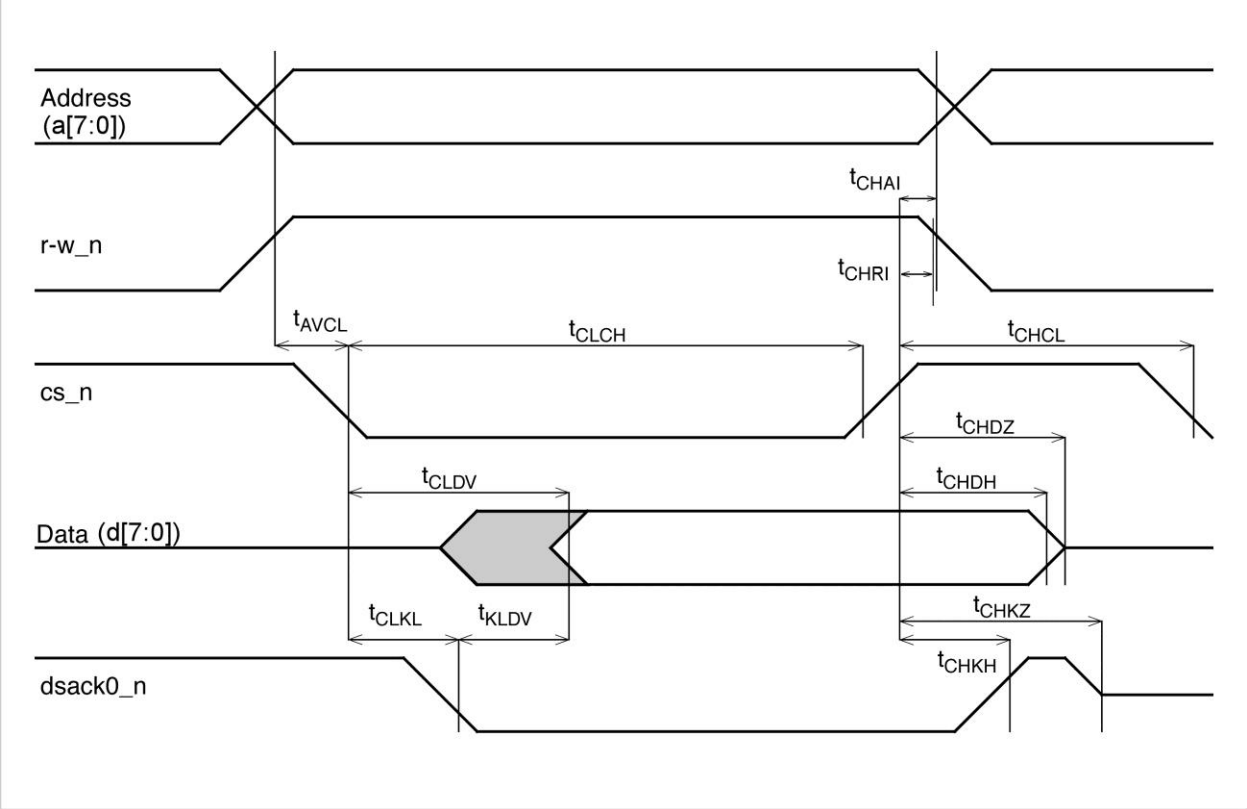


Figure 12. Mode 3: Asynchronous Operation, Read Cycle

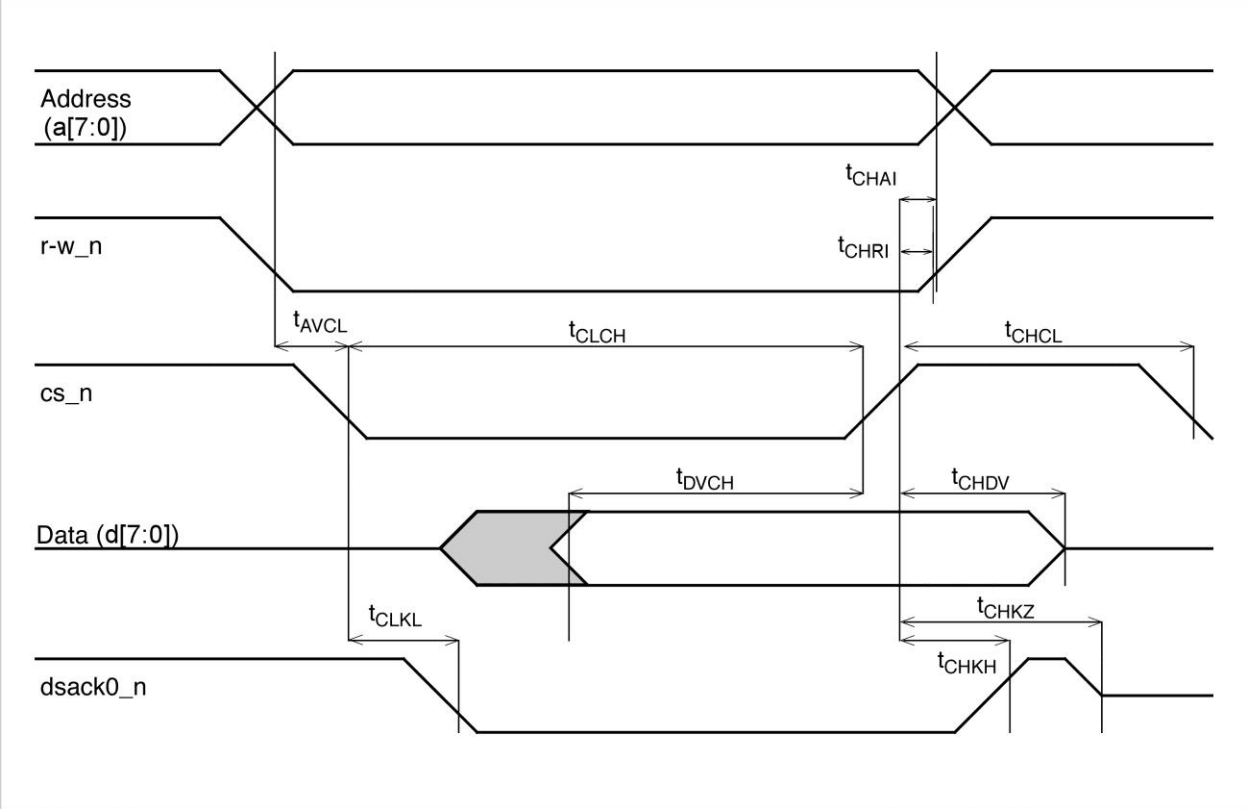


Figure 13. Mode 3: Asynchronous Operation, Write Cycle

Table 16. Mode 3: Synchronous Operation Timing for 5.0V Operation

Symbol	Parameter	Minimum	Maximum
$1/t_{XTAL}$	Oscillator Frequency	8 MHz	16 MHz
$1/t_{SCLK}$	System Clock Frequency	4 MHz	10 MHz
$1/t_{MCLK}$	Memory Clock Frequency	2 MHz	8 MHz
t_{EHDV}	e High to Data Valid (for High-Speed Registers 02H, 04H, and 5H)	–	55 ns
	e High to Data Valid (for Low-Speed Registers) Read Cycle without Previous Write[a]	–	1.5 t_{MCLK} + 100 ns
	e High to Data Valid (for Low-Speed Registers) Read Cycle with Previous Write	–	3.5 t_{MCLK} + 100 ns
t_{ELDH}	Data Hold after e Low for a Read Cycle	5 ns	–
t_{ELDZ}	Data Float after e Low	–	35 ns
t_{ELDV}	Data Hold after e Low for a Write Cycle	15 ns	–
t_{AVEH}	Address and r-w_n to e Setup	25 ns	–
t_{ELAV}	Address and r-w_n Valid after e Falls	15 ns	–
t_{CVEH}	cs_n Valid to e High	0 ns	–
t_{ELCV}	cs_n Valid after e Low	0 ns	–
t_{DVEL}	Data Setup to e Low	55 ns	–
t_{EHEL}	e Active Width	100 ns	–
t_{AVAV}	Start of a Write Cycle after a Previous Write Access	2 t_{MCLK}	–
t_{AVCL}	Address or r-w_n to cs_n Low Setup	3 ns	–
t_{CHAI}	cs_n High Address Invalid	7 ns	–
t_{COPD}	clkout Period (CD_V is the value loaded in the CLKOUT Register representing the clkout divisor)	(CD_V + 1) × t_{OSC}	
t_{CHCL}	clkout High Period (CD_V is the value loaded in the CLKOUT Register representing the clkout divisor)	(CD_V + 1) × ½ t_{OSC} – 10	(CD_V + 1) × ½ t_{OSC} + 15

[a]A “Read Cycle without Previous Write” is where a read cycle follows a write cycle and where the falling edge of e for the write cycle and the rising edge of e for the read cycle are separated by at least 2 × t_{MCLK}.

Table 17. Mode 3: Synchronous Operation Timing for 3.3V Operation

Symbol	Parameter	Minimum	Maximum
$1/t_{XTAL}$	Oscillator Frequency	8 MHz	16 MHz
$1/t_{SCLK}$	System Clock Frequency	4 MHz	10 MHz
$1/t_{MCLK}$	Memory Clock Frequency	2 MHz	8 MHz
t_{EHDV}	e High to Data Valid (for High-Speed Registers 02H, 04H, and 5H)	–	60 ns
	e High to Data Valid (for Low-Speed Registers) Read Cycle without Previous Write[a]	–	1.5 t_{MCLK} + 100 ns
	e High to Data Valid (for Low-Speed Registers) Read Cycle with Previous Write	–	3.5 t_{MCLK} + 100 ns
t_{ELDH}	Data Hold after e Low for a Read Cycle	5 ns	–
t_{ELDZ}	Data Float after e Low	–	50 ns
t_{ELDV}	Data Hold after e Low for a Write Cycle	15 ns	–
t_{AVEH}	Address and r-w_n to e Setup	25 ns	–
t_{ELAV}	Address and r-w_n Valid after e Falls	15 ns	–
t_{CVEH}	cs_n Valid to e High	0 ns	–
t_{ELCV}	cs_n Valid after e Low	0 ns	–
t_{DVEL}	Data Setup to e Low	55 ns	–
t_{EHEL}	e Active Width	100 ns	–
t_{AVAV}	Start of a Write Cycle after a Previous Write Access	2 t_{MCLK}	–
t_{AVCL}	Address or r-w_n to cs_n Low Setup	3 ns	–
t_{CHAI}	cs_n High Address Invalid	7 ns	–
t_{COPD}	clkout Period (CD_V is the value loaded in the CLKOUT Register representing the clkout divisor)	(CD_V + 1) × t_{OSC}	
t_{CHCL}	clkout High Period (CD_V is the value loaded in the CLKOUT Register representing the clkout divisor)	(CD_V + 1) × ½ t_{OSC} – 10	(CD_V + 1) × ½ t_{OSC} + 15

[a]A “Read Cycle without Previous Write” is where a read cycle follows a write cycle and where the falling edge of e for the write cycle and the rising edge of e for the read cycle are separated by at least 2 × t_{MCLK}.

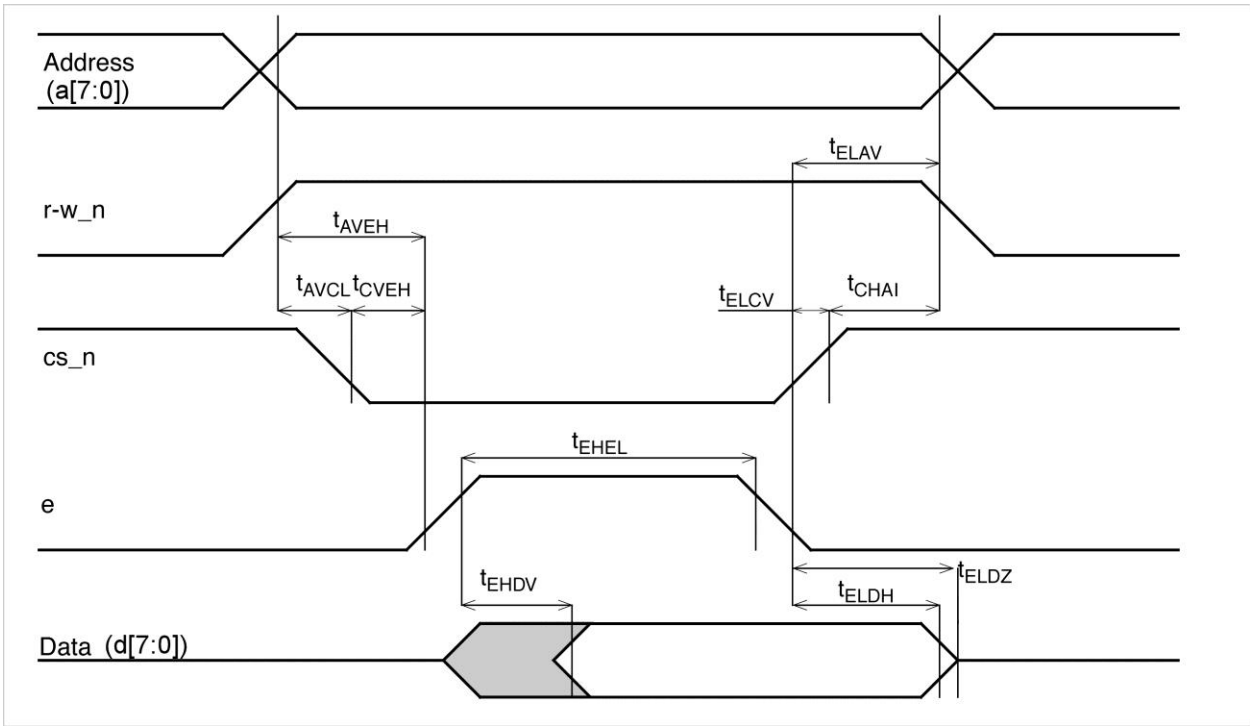


Figure 14. Mode 3: Synchronous Operation, Read Cycle Timing

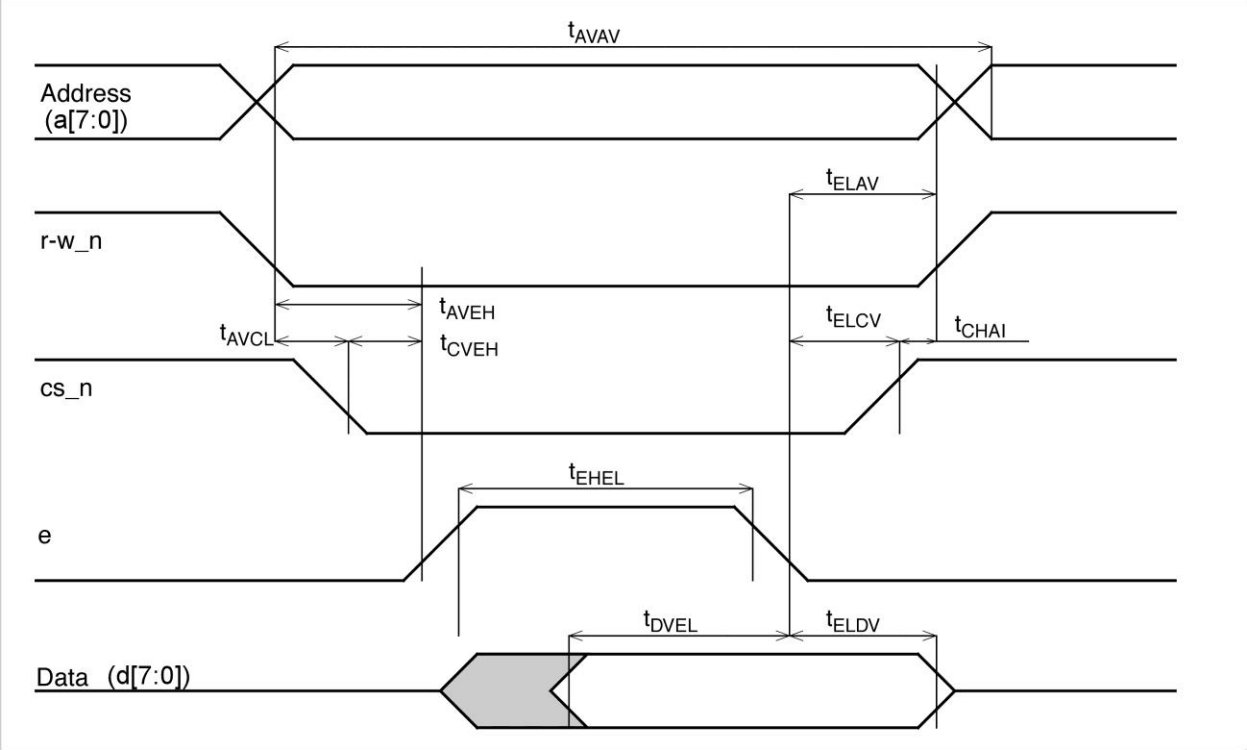


Figure 15. Mode 3: Synchronous Operation, Write Cycle Timing

Table 18. Serial Interface Mode Timing for 5.0V Operation

Symbol	Parameter	Minimum	Maximum
sclk	Serial Port Interface Clock	0.5 MHz	8 MHz
t_{CYC}	1/sclk	125 ns	2000 ns
t_{SKHI}	Minimum Clock High Time	65 ns	–
t_{SKLO}	Minimum Clock Low Time	65 ns	–
t_{LEAD}	Enable Lead Time	70 ns	–
t_{LAG}	Enable Lag Time	109 ns	–
t_{ACC}	Access Time	–	60 ns
t_{PDO}	Maximum Data Out Delay Time	–	59 ns
t_{HO}	Minimum Data Out Hold Time	0 ns	–
t_{DIS}	Maximum Data Out Disable Time	–	665 ns
t_{SETUP}	Minimum Data Setup Time	35 ns	–
t_{HOLD}	Minimum Data Hold Time	84 ns	–
t_{RISE}	Maximum Time for Input to go from V_{OL} to V_{OH}	–	100 ns
t_{FALL}	Maximum Time for input to go from V_{OH} to V_{OL}	–	100 ns
t_{CS}	Minimum Time between Consecutive cs_n Assertions	670 ns	–
t_{COPD}	clkout Period (CD_V is the value loaded in the CLKOUT Register representing the clkout divisor)	$(CD_V + 1) \times t_{OSC}$	
t_{CHCL}	clkout High Period (CD_V is the value loaded in the CLKOUT Register representing the clkout divisor)	$(CD_V + 1) \times ½$ $t_{OSC} - 10$	$(CD_V + 1) \times ½$ $t_{OSC} + 15$

Table 19. Serial Interface Mode Timing for 3.3V Operation

Symbol	Parameter	Minimum	Maximum
sclk	Serial Port Interface Clock	0.5 MHz	8 MHz
t_{CYC}	1/sclk	125 ns	2000 ns
t_{SKHI}	Minimum Clock High Time	65 ns	–
t_{SKLO}	Minimum Clock Low Time	65 ns	–
t_{LEAD}	Enable Lead Time	70 ns	–
t_{LAG}	Enable Lag Time	109 ns	–
t_{ACC}	Access Time	–	60 ns
t_{PDO}	Maximum Data Out Delay Time	–	59 ns
t_{HO}	Minimum Data Out Hold Time	0 ns	–
t_{DIS}	Maximum Data Out Disable Time	–	665 ns
t_{SETUP}	Minimum Data Setup Time	35 ns	–
t_{HOLD}	Minimum Data Hold Time	84 ns	–
t_{RISE}	Maximum Time for Input to go from V_{OL} to V_{OH}	–	100 ns
t_{FALL}	Maximum Time for input to go from V_{OH} to V_{OL}	–	100 ns
t_{CS}	Minimum Time between Consecutive cs_n Assertions	670 ns	–
t_{COPD}	clkout Period (CD_V is the value loaded in the CLKOUT Register representing the clkout divisor)	$(CD_V + 1) \times t_{OSC}$	
t_{CHCL}	clkout High Period (CD_V is the value loaded in the CLKOUT Register representing the clkout divisor)	$(CD_V + 1) \times ½$ $t_{OSC} - 10$	$(CD_V + 1) \times ½$ $t_{OSC} + 15$

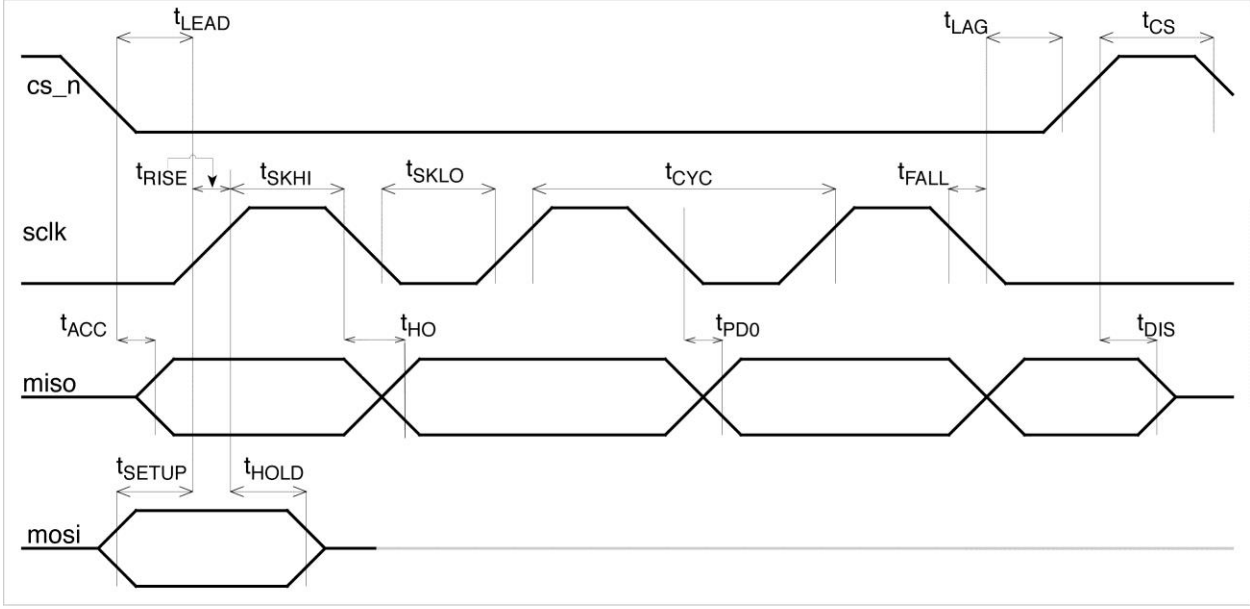


Figure 16. Serial Interface Mode: icp = 0 and cp = 0

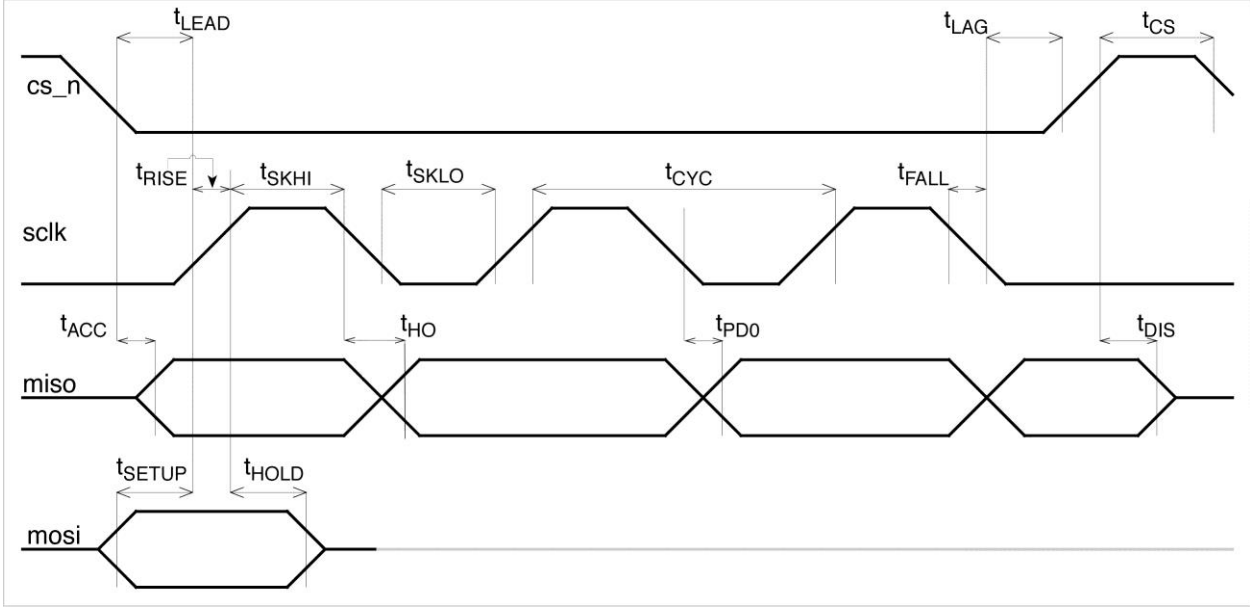


Figure 17. Serial Interface Mode: icp = 1 and cp = 1

6. Innovasic Part Number Cross-Reference

Table 20 cross-references the current Innovasic part number with the corresponding Intel part number.

Table 20. Innovasic Part Number Cross-Reference

Innovasic Part Number	Intel Part Number	Package Type	Temperature Grades
IA82527PQF44AR2 (lead free–RoHS)	AS82527 AS82527F8 QE82527	44-Pin PQFP	Automotive
IA82527PLC44AR2 (lead free–RoHS)	AN82527 AN82527F8 QX82527 TN82527 EN82527	44-Pin PLCC	Automotive

Other packages and temperature grades may also be available.

7. Errata

7.1 Summary

Errata No.	Problem	Version 2 Part Numbers IA82527PQF44AR2 IA82527PLC44AR2
1	The CPU writes to Msg Box 15 RAM cannot be read back if MsgVal is set.	Exists
2	Setting the IntPnd bit to 1 from CPU interface will not cause Interrupt.	Exists
3	An unintended Remote Frame may be generated.	Exists
4	Majority Logic sample mode delays start of ACK bit transmission by one time quanta.	Exists
5	dsack0_n signal may not respond properly under certain conditions.	Exists
6	Behavior of double buffered Msgbox15 differs from the OEM device.	Exists

7.2 Detail

Errata No. 1

Problem: The CPU writes to Msg Box 15 RAM cannot be read back if MsgVal is set.

Description: If the MsgVal bit (Bits [7–6]) of Msg Box 15 Control_0 register (0xF0) is set, any CPU writes to the Msg Box 15 arbitration 0–3 registers (0xF2–0xF5), and data 0–7 registers (0xF7–0xFE) will operate properly, however CPU reads of these registers will return unknown data. In other words, any CPU data written to Msg Box 15 will not be read back correctly if the MsgVal bit is set. If the MsgVal bit (Bits [7–6]) of Msg Box 15 Control_0 register (0xF0) is reset, CPU data written can be read back normally.

Workaround: The workaround is to clear the MsgVal bit (Bits [7–6]) of Msg Box 15 Control_0 register (0xF0) before trying to read back any CPU data written to the Msg Box 15 arbitration 0–3 registers (0xF2–0xF5), and data 0–7 registers (0xF7–0xFE).

Errata No. 2

Problem: Setting the IntPnd bit to 1 from CPU interface will not cause Interrupt.

Description: During normal operation, a CAN message event sets the IntPnd bit of Control 0 Register of the appropriate message box (assuming appropriate interrupt enables are set), and the interrupt signal is asserted. The CPU will then reset IntPnd to clear the interrupt. The errata issue occurs if the user directly sets the IntPnd bit via the CPU interface, no interrupt will be generated.

Workaround: None.

Errata No. 3

Problem: An unintended Remote Frame may be generated.

Description: If a Message Box is set to receive and a Remote Frame with a matching ID and Data Length Code (DLC) is received, the IA82527 will generate an unexpected Remote Frame for the ID in the Message Box instead of just acknowledging the CAN message.

A Message Box configured as follows may lead to this scenario, as explained below:

1. A Message Box is set with an ID in the Arbitration Registers to match the ID of Remote Frame.
2. The Message Box Control_0 Register has MsgVal(Bits[7-6]) in the set state.
3. The Message Box Control_1 Register has all fields in the reset state.
4. The Message Box Configuration Register has the Dir bit (bit 3) reset to 0 for receive.
5. The Message Box Configuration Register has the DLC field set to match the DLC of the Remote Frame.

When the IA82527 sees a Remote Frame that matches the Message Box ID and DLC, the IA82527 will generate the expected RX_OK status change interrupt. The IA82527 will also generate an unexpected RX interrupt for the Message Box that matches the ID of the Remote Frame if the RXIE field of the Message Box Control_0 register is in the set state. In addition, the IA82527 will generate an unexpected Remote Frame for the ID in the Message Box.

Workaround: In a system that uses remote frames, only use a single Remote Frame Requester for a single Remote Frame Responder.

Errata No. 4

Problem: Majority Logic sample mode delays start of ACK bit transmission by one time quanta.

Description: When the SPL bit (Bit 7) of the Bit Timing Register 1 (0x4F) is set to 1 to enable the 3 sample Majority Logic mode, the transmission of the ACK bit in response to a received CAN frame will be time shifted by 1 time quanta. With sufficient cable propagation delays and propagation delays through CAN transceiver parts, CAN nodes on the CAN bus may see the ACK bit being a 0 shifted over into its ACK delimiter bit time and flag this as an error.

Workaround: Use Single Sample mode instead of Majority Logic Sample Mode. The SPL bit of the Bit Timing Register 1 (bit 7 of address 0x4F) should be a 0.

Errata No. 5

Problem: dsack0_n signal may not respond properly under certain conditions.

Description: Under certain conditions when the cs_n is asserted near the edge of xtal1 the dsack0_n signal may not be properly generated. Depending on the clock divider settings sys_clk and mem_clk at address 0x02, if the setup or hold time for cs_n with respect to xtal1 edge (rising or falling) is violated, it is possible that dsack0_n will not respond to the cycle. This can cause problems for systems that are dependent upon dsack0_n to occur before releasing cs_n to finish the cycle. Note: The cycle still operates correctly in respect to reading or writing of data, only the dsack0_n signal may not be generated.

Workaround:

Workaround #1: Do not use dsack0_n as part of the bus cycle timing.

Workaround #2: cs_n must meet the following timing relationship with regards to the xtal1 clock edge:

sys clock divide	edge of xtal1	setup (ns)	hold (ns)
1 dsc=0	rise	7	16
2 dsc=1	fall	7	16

IA82527 Errata Concerning Behavior of double buffered Msgbox 15

Errata No. 6

Problem: Behavior of double buffered Msgbox15 differs from the OEM device. There are several facets to this errata which are all tightly coupled.

Errata No. 6.1

Problem: Receiving a second message while reading the first stored message may corrupt the data being read.

Description: If a second CAN message is stored to MsgBox 15 during the time the information from the first message is being read, a byte of this data may reflect that of the new message being stored. When using double reads, this corrupted data may be captured in the High Speed Read Register when the low speed register is accessed. When using single reads this corrupted data may appear on the external data bus for a very brief amount of time (2 – 6ns). If the data from the first message is retrieved prior to receiving the second message, this will not be a problem.

Workaround: Because of the coupled nature of these errata, the workaround must address all facets together. Figure 18 provides the description of a software workaround that addresses errata 6.1 and 6.2.

Errata No. 6.2

Problem: Control Register 0 and Control Register 1 have different behavior than the OEM part when two messages have been stored before either message is processed.

Description: IntPnd and NewDat are not automatically reasserted after being cleared to acknowledge the first message. MsgLst will be asserted after the second message is received while NewDat is set. RmtPnd will be asserted after the second message is received while NewDat is set. See Table 21 and Table 22 for differences.

Workaround: Because of the coupled nature of these errata, the workaround must address all facets together. Figure 18 provides the description of a software workaround that addresses errata 6.1 and 6.2.

Errata No. 6.3

Problem: Receiving a third message before the first two messages are processed can cause data to be lost.

Description: If a third message is stored before the NewDat and RmtPnd bits are cleared, the

Arbitration ID information for the first message will be overwritten by that of the third. In addition, the Arbitration ID information of the second message will be kept instead of being replaced by that of the third. See Table 23 and Table 24 for differences.
Workaround: There is no workaround for errata 6.3. To avoid this situation, user systems must be implemented such that no more than two messages can be received by this mailbox in the time between interrupt services.

Differences in MsgBox 15 behavior for Control Register 0 and Control Register 1.

Table 21. OEM part behavior

Action	RmtPnd	NewDat	MsgLst	IntPnd	Int_n
Before any CAN messages received	0	0	0	0	1
1st CAN message received	0	1	0	1	0
2nd CAN message received	0	1	0	1	0
MPU reads 1st CAN message ID, DLC, DATA	0	1	0	1	0
MPU writes IntPnd = RESET	0	1	0	1	0
MPU writes RmtPnd = RESET	0	1	0	1	0
MPU writes NewDat = RESET	0	1	0	1	0
MPU reads 2nd CAN message ID, DLC, DATA	0	1	0	1	0
MPU writes IntPnd = RESET	0	1	0	1	0
MPU writes RmtPnd = RESET	0	1	0	1	0
MPU writes NewDat = RESET	0	0	0	0	1

Table 22. IA82527 part behavior

Action	RmtPnd	NewDat	MsgLst	IntPnd	Int_n
Before any CAN messages received	0	0	0	0	1
1st CAN message received	0	1	0	1	0
2nd CAN message received	1	1	1	1	0
MPU reads 1st CAN message ID, DLC, DATA	1	1	1	1	0
MPU writes IntPnd = RESET	1	1	1	0	1
MPU writes RmtPnd = RESET	0	1	1	0	1
MPU writes NewDat = RESET	0	0	1	0	1
MPU reads 2nd CAN message ID, DLC, DATA	0	0	1	0	1
MPU writes IntPnd = RESET	0	0	1	0	1
MPU writes RmtPnd = RESET	0	0	1	0	1
MPU writes NewDat = RESET	0	0	0	0	1

Table 23. CAN MESSAGES SENT

MSG	ID	DLC	DATA
1	0x111	4	0x00, 0x01, 0x02, 0x03
2	0x222	5	0x04, 0x05, 0x06, 0x07, 0x08
3	0x333	6	0x09,0x0A, 0x0B, 0x0C, 0x0D, 0x0E

Table 24. CAN MESSAGES RECEIVED

MSG	ID	DLC	DATA
1	0x333	4	0x00, 0x01, 0x02, 0x03
3	0x222	6	0x09,0x0A, 0x0B, 0x0C, 0x0D, 0x0E

Note that the IDs have been corrupted.

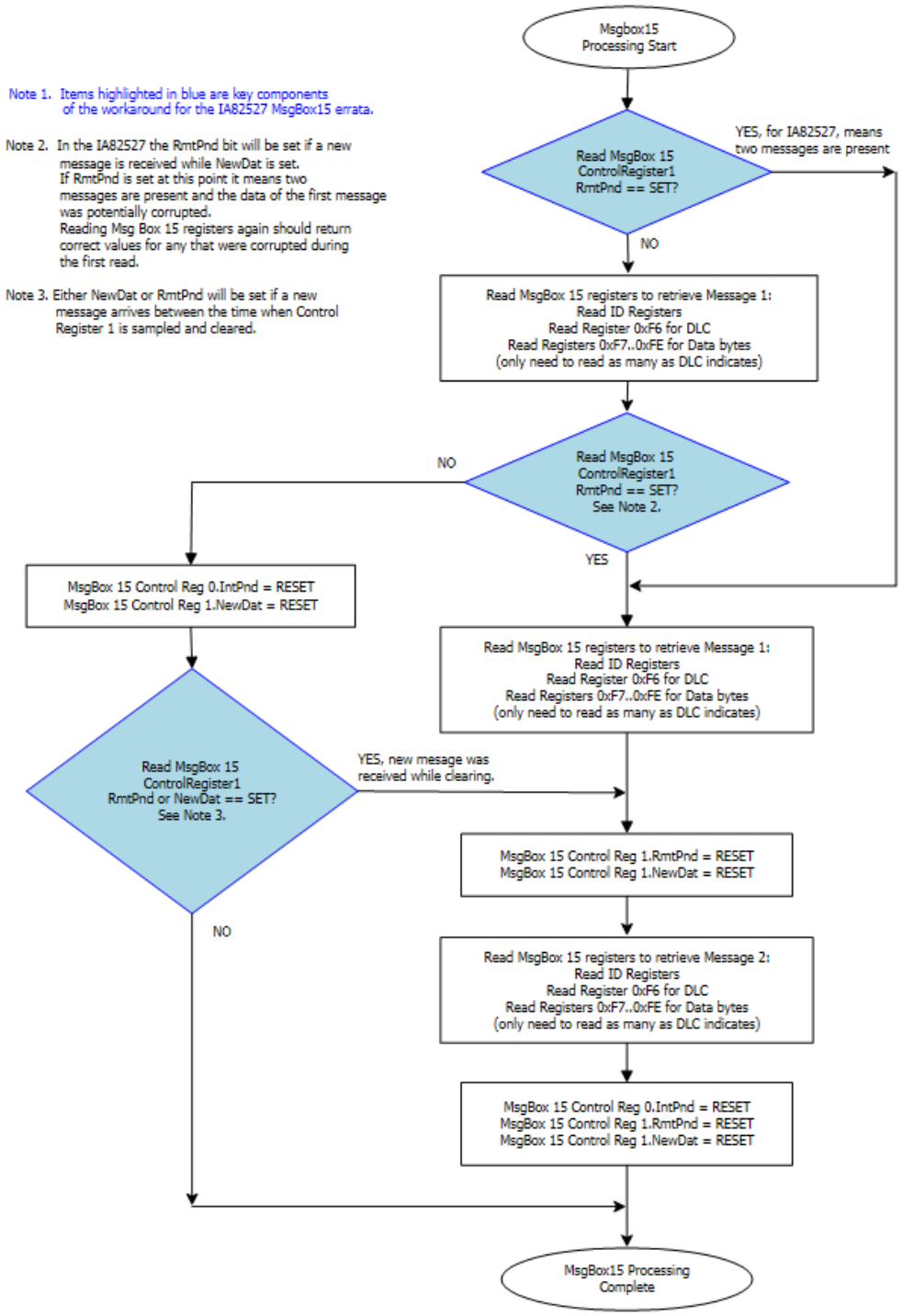


Figure 18. Flow chart of software workaround for errata number 6.1 and 6.2

8. Revision History

Table 25 presents the sequence of revisions to document IA211080504.

Table 25. Revision History

Date	Revision	Description	Page(s)
August 12, 2008	00	First edition released.	NA
August 25, 2008	01	Errata No. 5 added.	49, 50
March 12, 2009	02	IA82527 - Rev 2 part marking and cross reference information added; Errata No. 6 added.	48, 49, 51
March 27, 2009	03	Updated PLCC package dimensions	11
April 29, 2009	04	Updated Tables 3, 6, 10, 11, 12, 14 to revise various ratings and descriptions; Updated Errata section to remove errata associated with pre-production parts and to add one new errata.	21, 26, 34, 38, 40, 46, 49, 50
June 1, 2009	05	Updated to include information for operation at 3.3V, and added Errata 4.	6, 16, 26, 27, 33-51, 54-56
Sept. 16, 2009	06	Corrected Tables 5 and 7 regarding ambient temperature range.	25, 27
December 20, 2012	07	Added Errata #5.	58
January 9, 2015	08	Modified the chip compatibility statement.	6
January 15, 2015	09	Added Errata #6 and associated diagrams/tables.	57-61

Date	Revision	Description	Page(s)
February 3, 2015	10	Modified Errata #6 and associated diagrams/tables.	57-60
February 25, 2015	11	Modified the description of Errata #6.1	57

9. For Further Information

The Innovasic Semiconductor IA82527 Controller Area Network (CAN) Serial Communications Controller is a form, fit, and function replacement for the original Intel® 82527 Serial Communications Controller.

The Innovasic Support Team wants our information to be complete, accurate, useful, and easy to understand. Please feel free to contact our experts at Innovasic at any time with suggestions, comments, or questions.

Innovasic Support Team
5635 Jefferson Street NE
Suite A
Albuquerque, NM 87109

(505) 883-5263
Fax: (505) 883-5477
Toll Free: (888) 824-4184
E-mail: support@innovasic.com
Website: http://www.Innovasic.com