MC14042B

Quad Transparent Latch

The MC14042B Quad Transparent Latch is constructed with MOS P−channel and N−channel enhancement mode devices in a single monolithic structure. Each latch has a separate data input, but all four latches share a common clock. The clock polarity (high or low) used to strobe data through the latches can be reversed using the polarity input. Information present at the data input is transferred to outputs Q and $\overline{Q}$ during the clock level which is determined by the polarity input. When the polarity input is in the logic "0" state, data is transferred during the low clock level, and when the polarity input is in the logic "1" state the transfer occurs during the high clock level.

Features

- Buffered Data Inputs
- Common Clock
- Clock Polarity Control
- Q and $\overline{Q}$ Outputs
- Double Diode Input Protection
- Supply Voltage Range = 3.0 Vdc to 1 8 Vdc
- Capable of Driving Two Low−power TTL Loads or One Low−power Schottky TTL Load Over the Rated Temperature Range
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- This Device is Pb−Free and is RoHS Compliant

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	−0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 1)	500	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8−Second Soldering)	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

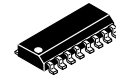1. Temperature Derating: "D/DW" Packages: −7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.
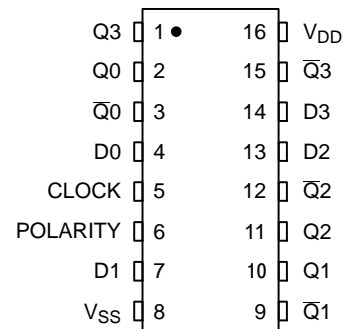
PIN ASSIGNMENT
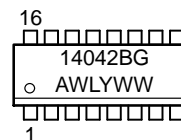
Q3	1 •	16	V_{DD}
Q0	2	15	$\overline{Q}3$
$\overline{Q}0$	3	14	D3
D0	4	13	D2
CLOCK	5	12	$\overline{Q}2$
POLARITY	6	11	Q2
D1	7	10	Q1
V_{SS}	8	9	$\overline{Q}1$

MARKING DIAGRAM

16
14042BG
○ AWLYWW
1

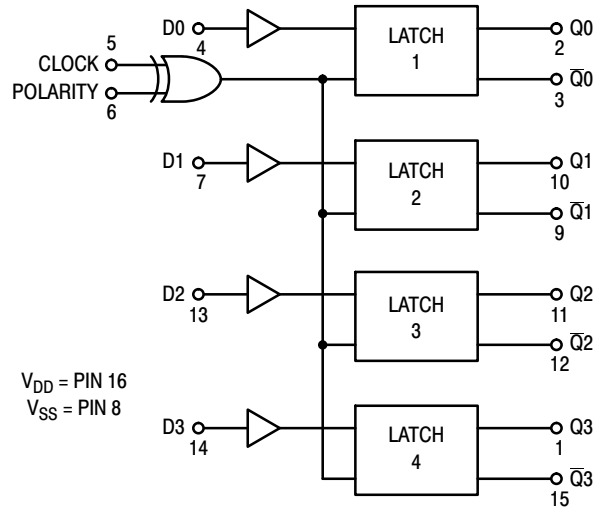|	
A	= Assembly Location
WL	= Wafer Lot
YY, Y	= Year
WW	= Work Week
G	= Pb−Free Indicator

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

MC14042B

TRUTH TABLE

Clock	Polarity	Q
0	0	Data
1	0	Latch
1	1	Data
0	1	Latch

LOGIC DIAGRAM

V_{DD} = PIN 16
V_{SS} = PIN 8

ORDERING INFORMATION

Device	Package	Shipping†
MC14042BDG	SOIC−16 (Pb−Free)	48 Units / Rail
NLV14042BDG*	SOIC−16 (Pb−Free)	48 Units / Rail
MC14042BDR2G	SOIC−16 (Pb−Free)	2500 Units / Tape & Reel
NLV14042BDR2G*	SOIC−16 (Pb−Free)	2500 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

MC14042B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V$_{SS}$)

Characteristic		Symbol	V$_{DD}$ Vdc	−55°C Min	−55°C Max	25°C Min	25°C Typ (Note 2)	25°C Max	125°C Min	125°C Max	Unit
Output Voltage "0" Level V$_{in}$ = V$_{DD}$ or 0		V$_{OL}$	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
			10	–	0.05	–	0	0.05	–	0.05	
			15	–	0.05	–	0	0.05	–	0.05	
"1" Level V$_{in}$ = 0 or V$_{DD}$		V$_{OH}$	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
			10	9.95	–	9.95	10	–	9.95	–	
			15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level (V$_O$ = 4.5 or 0.5 Vdc) (V$_O$ = 9.0 or 1.0 Vdc) (V$_O$ = 13.5 or 1.5 Vdc)		V$_{IL}$	5.0	–	1.5	–	2.25	1.5	–	1.5	Vdc
			10	–	3.0	–	4.50	3.0	–	3.0	
			15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level (V$_O$ = 0.5 or 4.5 Vdc) (V$_O$ = 1.0 or 9.0 Vdc) (V$_O$ = 1.5 or 13.5 Vdc)		V$_{IH}$	5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
			10	7.0	–	7.0	5.50	–	7.0	–	
			15	11	–	11	8.25	–	11	–	
Output Drive Current (V$_{OH}$ = 2.5 Vdc) Source (V$_{OH}$ = 4.6 Vdc) (V$_{OH}$ = 9.5 Vdc) (V$_{OH}$ = 13.5 Vdc)		I$_{OH}$	5.0	−3.0	–	−2.4	−4.2	–	−1.7	–	mAdc
			5.0	−0.64	–	−0.51	−0.88	–	−0.36	–	
			10	−1.6	–	−1.3	−2.25	–	−0.9	–	
			15	−4.2	–	−3.4	−8.8	–	−2.4	–	
(V$_{OL}$ = 0.4 Vdc) Sink (V$_{OL}$ = 0.5 Vdc) (V$_{OL}$ = 1.5 Vdc)		I$_{OL}$	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
			10	1.6	–	1.3	2.25	–	0.9	–	
			15	4.2	–	3.4	8.8	–	2.4	–	
Input Current		I$_{in}$	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Capacitance (V$_{in}$ = 0)		C$_{in}$	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (Per Package)		I$_{DD}$	5.0	–	1.0	–	0.002	1.0	–	30	µAdc
			10	–	2.0	–	0.004	2.0	–	60	
			15	–	4.0	–	0.006	4.0	–	120	
Total Supply Current (Notes 3 & 4) (Dynamic plus Quiescent, Per Package) (C$_L$ = 50 pF on all outputs all buffers switching)		I$_T$	5.0	I$_T$ = (1.0 µA/kHz) f + I$_{DD}$							µAdc
			10	I$_T$ = (2.0 µA/kHz) f + I$_{DD}$							
			15	I$_T$ = (3.0 µA/kHz) f + I$_{DD}$							

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
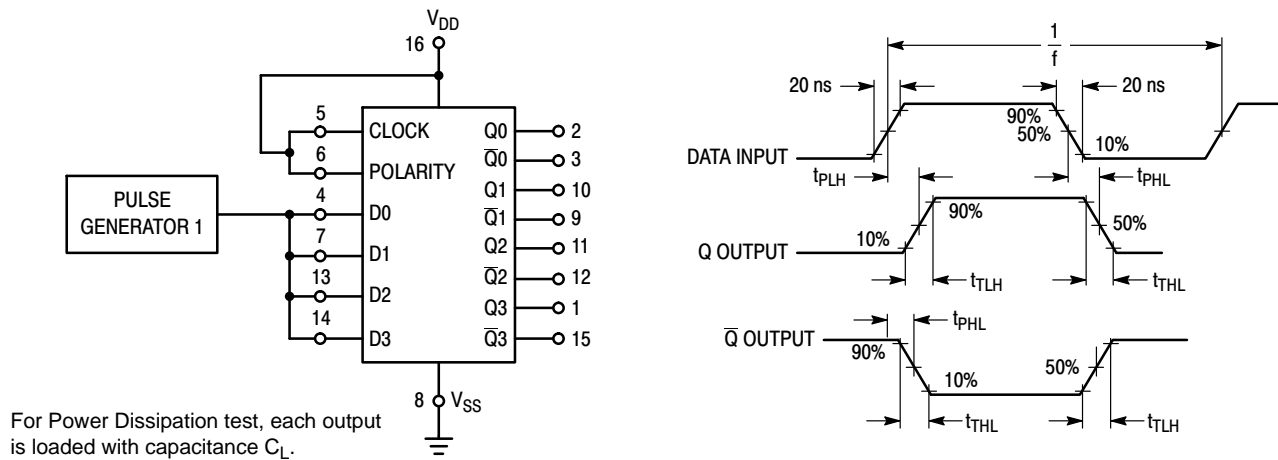3. The formulas given are for the typical characteristics only at 25°C.
4. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L − 50)\ Vfk$$

where: I$_T$ is in µA (per package), C$_L$ in pF, V = (V$_{DD}$ − V$_{SS}$) in volts, f in kHz is input frequency, and k = 0.004.

MC14042B

SWITCHING CHARACTERISTICS (Note 5) (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ (Note 6)	Max	Unit
Output Rise and Fall Time t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns	t_{TLH}, t_{THL}	5.0 10 15	– – –	100 50 40	200 100 80	ns
Propagation Delay Time, D to Q, $\overline{Q}$ t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 135 ns t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 57 ns t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 35 ns	t_{PLH}, t_{PHL}	5.0 10 15	– – –	220 90 60	440 180 120	no
Propagation Delay Time, Clock to Q, $\overline{Q}$ t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 135 ns t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 57 ns t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 35 ns	t_{PLH}, t_{PHL}	5.0 10 15	– – –	220 90 60	440 180 120	ns
Clock Pulse Width	t_{WH}	5.0 10 15	300 100 80	150 50 40	– – –	ns
Clock Pulse Rise and Fall Time	t_{TLH}, t_{THL}	5.0 10 15	– – –	– – –	15 5.0 4.0	µs
Hold Time	t_h	5.0 10 15	100 50 40	50 25 20	– – –	ns
Setup Time	t_{su}	5.0 10 15	50 30 25	0 0 0	– – –	ns

5. The formulas given are for the typical characteristics only at 25°C.
6. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

MC14042B

**Figure 1. AC and Power Dissipation Test Circuit and Timing Diagram
(Data to Output)**

NOTE: C_L connected to output under test.

*Input clock rise time is 20 ns except for maximum rise time test.
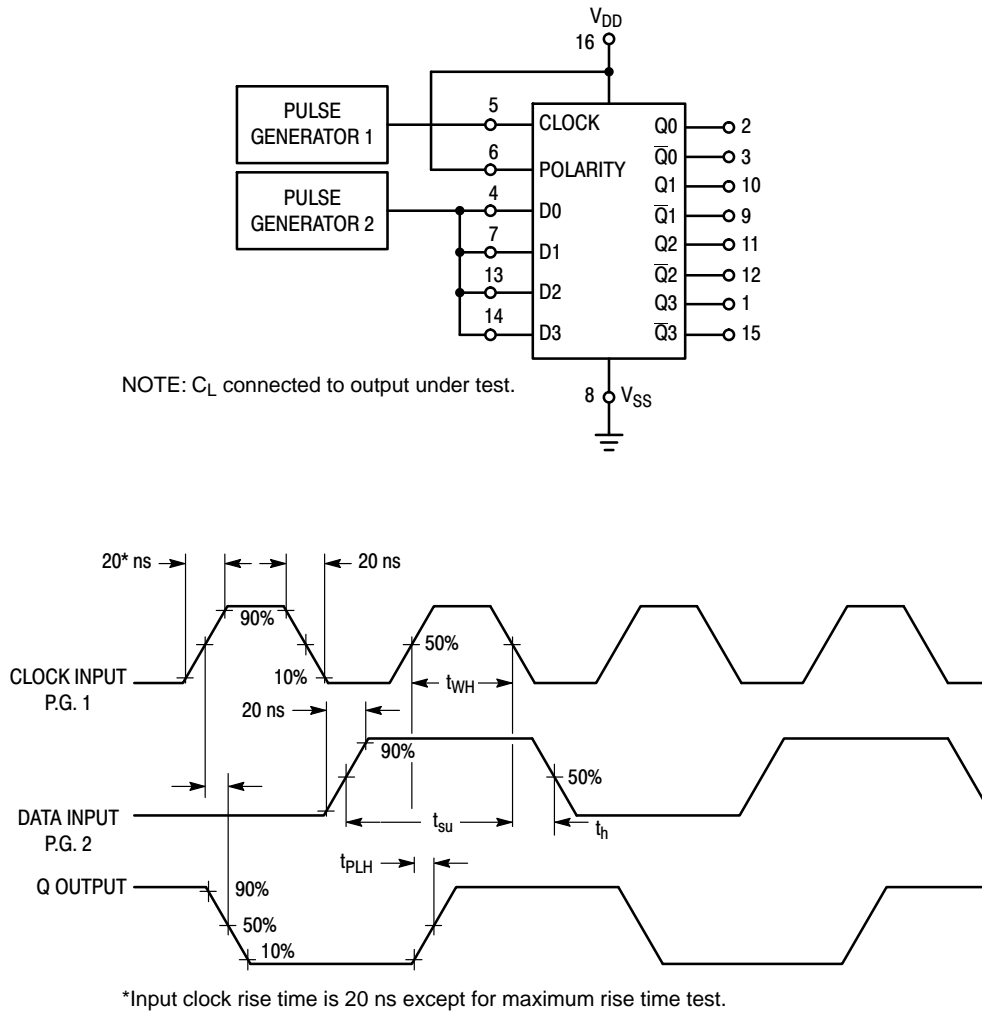
**Figure 2. AC Test Circuit and Timing Diagram
(Clock to Output)**

SOIC−16
CASE 751B−05
ISSUE K

DATE 29 DEC 2006

SCALE 1:1

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

⊕ 0.25 (0.010) Ⓜ B Ⓢ

⊕ 0.25 (0.010) Ⓜ T B Ⓢ A Ⓢ

STYLE 1:
PIN 1. COLLECTOR
2. BASE
3. EMITTER
4. NO CONNECTION
5. EMITTER
6. BASE
7. COLLECTOR
8. COLLECTOR
9. BASE
10. EMITTER
11. NO CONNECTION
12. EMITTER
13. BASE
14. COLLECTOR
15. EMITTER
16. COLLECTOR

STYLE 2:
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION
4. CATHODE
5. CATHODE
6. NO CONNECTION
7. ANODE
8. CATHODE
9. CATHODE
10. ANODE
11. NO CONNECTION
12. CATHODE
13. CATHODE
14. NO CONNECTION
15. ANODE
16. CATHODE

STYLE 3:
PIN 1. COLLECTOR, DYE #1
2. BASE, #1
3. EMITTER, #1
4. COLLECTOR, #1
5. COLLECTOR, #2
6. BASE, #2
7. EMITTER, #2
8. COLLECTOR, #2
9. COLLECTOR, #3
10. BASE, #3
11. EMITTER, #3
12. COLLECTOR, #3
13. COLLECTOR, #4
14. BASE, #4
15. EMITTER, #4
16. COLLECTOR, #4

STYLE 4:
PIN 1. COLLECTOR, DYE #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. COLLECTOR, #3
6. COLLECTOR, #3
7. COLLECTOR, #4
8. COLLECTOR, #4
9. BASE, #4
10. EMITTER, #4
11. BASE, #3
12. EMITTER, #3
13. BASE, #2
14. EMITTER, #2
15. BASE, #1
16. EMITTER, #1

STYLE 5:
PIN 1. DRAIN, DYE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. DRAIN, #3
6. DRAIN, #3
7. DRAIN, #4
8. DRAIN, #4
9. GATE, #4
10. SOURCE, #4
11. GATE, #3
12. SOURCE, #3
13. GATE, #2
14. SOURCE, #2
15. GATE, #1
16. SOURCE, #1

STYLE 6:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. CATHODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE
15. ANODE
16. ANODE

STYLE 7:
PIN 1. SOURCE N-CH
2. COMMON DRAIN (OUTPUT)
3. COMMON DRAIN (OUTPUT)
4. GATE P-CH
5. COMMON DRAIN (OUTPUT)
6. COMMON DRAIN (OUTPUT)
7. COMMON DRAIN (OUTPUT)
8. SOURCE P-CH
9. SOURCE P-CH
10. COMMON DRAIN (OUTPUT)
11. COMMON DRAIN (OUTPUT)
12. COMMON DRAIN (OUTPUT)
13. GATE N-CH
14. COMMON DRAIN (OUTPUT)
15. COMMON DRAIN (OUTPUT)
16. SOURCE N-CH

SOLDERING FOOTPRINT

8X
6.40

16X 1.12

16X
0.58

1.27
PITCH

DIMENSIONS: MILLIMETERS

DOCUMENT NUMBER:	98ASB42566B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	SOIC−16		**PAGE 1 OF 1**

PUBLICATION ORDERING INFORMATION

◊