NTHD4502N

MOSFET – Power, Dual, N-Channel, ChipFET

30 V, 3.9 A

Features

- Planar Technology Device Offers Low $R_{DS(on)}$ and Fast Switching Speed
- Leadless ChipFET Package has 40% Smaller Footprint than TSOP–6. Ideal Device for Applications Where Board Space is at a Premium.
- ChipFET Package Exhibits Excellent Thermal Capabilities. Ideal for Applications Where Heat Transfer is Required.
- These Devices are Pb–Free and are RoHS Compliant

Applications

- DC–DC Buck or Boost Converters
- Low Side Switching
- Optimized for Battery and Low Side Switching Applications in Computing and Portable Equipment

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain–to–Source Voltage			V_{DSS}	30	V
Gate–to–Source Voltage			V_{GS}	±20	V
Continuous Drain Current (Note 1)	Steady State	T_A = 25°C	I_D	2.9	A
		T_A = 85°C		2.1	
	t ≤ 5 s	T_A = 25°C		3.9	
Power Dissipation (Note 1)	Steady State	T_A = 25°C	P_D	1.13	W
	t ≤ 5 s			2.1	
Continuous Drain Current (Note 2)	Steady State	T_A = 25°C	I_D	2.2	A
		T_A = 85°C		1.6	
Power Dissipation (Note 2)		T_A = 25°C	P_D	0.64	W
Pulsed Drain Current	t_p = 10 μs		I_{DM}	12	A
ESD Capability (Note 3)	C = 100 pF, R_S = 1500 Ω		ESD–HBM	125	V
Operating Junction and Storage Temperature			T_J, T_{STG}	–55 to 150	°C
Source Current (Body Diode)			I_S	2.5	A
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T_L	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces).
2. Surface Mounted on FR4 Board using the minimum recommended pad size (Cu area = 0.214 in sq).
3. ESD Rating Information: HBM Class 0.

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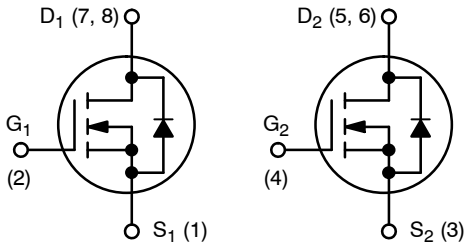
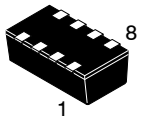
$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	I_D MAX
30 V	80 mΩ @ 10 V	3.9 A
	110 mΩ @ 4.5 V	

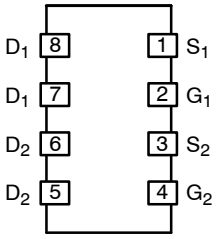


N–Channel MOSFET

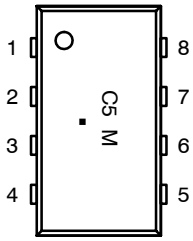


ChipFET
CASE 1206A
STYLE 2

PIN CONNECTIONS



MARKING DIAGRAM



C5 = Specific Device Code
M = Month Code
▪ = Pb–Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NTHD4502NT1G	ChipFET (Pb–Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction−to−Ambient − Steady State (Note 4)	$R_{\theta JA}$	110	°C/W
Junction−to−Ambient − t ≤ 5 s (Note 4)	$R_{\theta JA}$	60	
Junction−to−Ambient − Steady State (Note 5)	$R_{\theta JA}$	195	
Junction−to−Foot − Steady State (Note 5)	$R_{\theta JF}$	40	

4. Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces).
5. Surface Mounted on FR4 Board using the minimum recommended pad size (Cu area = 0.214 in sq).

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA	30	36		V
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 24 V			1.0	μA
		V_{GS} = 0 V, V_{DS} = 24 V, T_J = 125°C			10	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
ON CHARACTERISTICS (Note 6)						
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250 μA	1.0	1.65	3.0	V
Drain−to−Source On−Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 2.9 A		78	85	mΩ
		V_{GS} = 4.5 V, I_D = 2.2 A		105	140	
Forward Transconductance	g_{FS}	V_{DS} = 15 V, I_D = 2.9 A		3.8		S
CHARGES AND CAPACITANCES						
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1.0 MHz, V_{DS} = 15 V		140		pF
Output Capacitance	C_{OSS}			53		
Reverse Transfer Capacitance	C_{RSS}			16		
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1.0 MHz, V_{DS} = 24 V		135	250	pF
Output Capacitance	C_{OSS}			42	75	
Reverse Transfer Capacitance	C_{RSS}			13	25	
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 15 V, I_D = 2.9 A		3.6	7.0	nC
Threshold Gate Charge	$Q_{G(TH)}$			0.3		
Gate−to−Source Charge	Q_{GS}			0.6		
Gate−to−Drain Charge	Q_{GD}			0.7		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 4.5 V, V_{DS} = 24 V, I_D = 2.9 A		1.9		nC
Threshold Gate Charge	$Q_{G(TH)}$			0.3		
Gate−to−Source Charge	Q_{GS}			0.6		
Gate−to−Drain Charge	Q_{GD}			0.9		

6. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

ELECTRICAL CHARACTERISTICS (continued) (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
DRAIN−SOURCE DIODE CHARACTERISTICS						
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 2.5 A		0.85	1.2	V
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, I_S = 2.9 A, dI_S/dt = 100 A/μs		8.6		ns
Reverse Recovery Charge	Q_{RR}			4.0		nC
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, I_S = 1.0 A, dI_S/dt = 100 A/μs		8.4		ns
Reverse Recovery Charge	Q_{RR}			4.0		nC
SWITCHING CHARACTERISTICS (Note 7)						
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 10 V, V_{DD} = 24 V, I_D = 1 A, R_G = 6 Ω		6.5	12	ns
Rise Time	t_r			5.4	10	
Turn−Off Delay Time	$t_{d(OFF)}$			14.9	25	
Fall Time	t_f			1.8	5.0	
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 4.5 V, V_{DD} = 24 V, I_D = 2.9 A, R_G = 2.5 Ω		7.8		ns
Rise Time	t_r			12.6		
Turn−Off Delay Time	$t_{d(OFF)}$			9.6		
Fall Time	t_f			2.8		

7. Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES

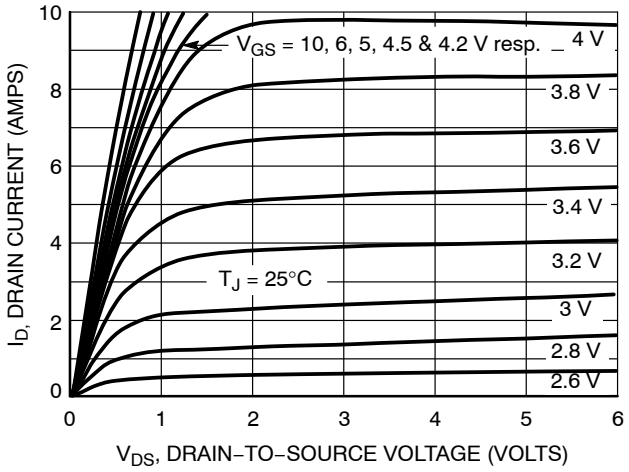


Figure 1. On−Region Characteristics

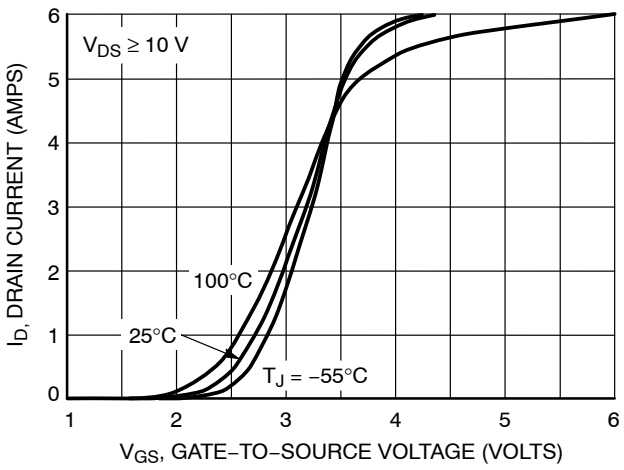


Figure 2. Transfer Characteristics

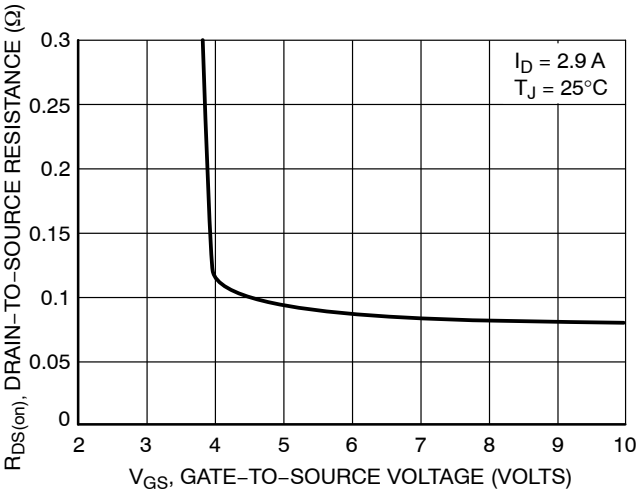


Figure 3. On−Resistance vs. Gate−to−Source Voltage

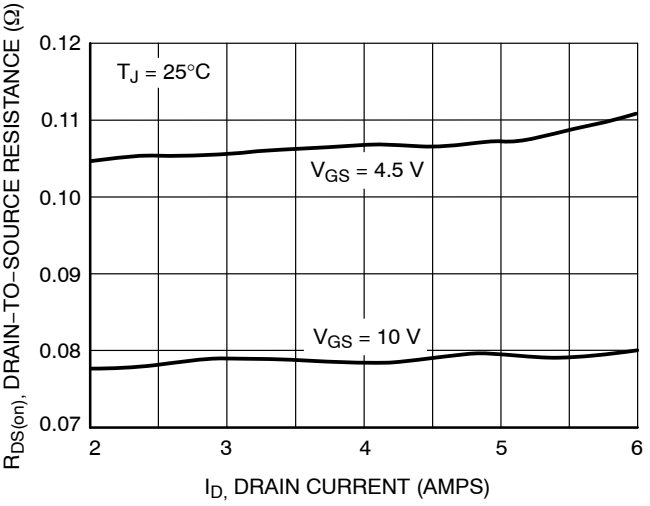


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

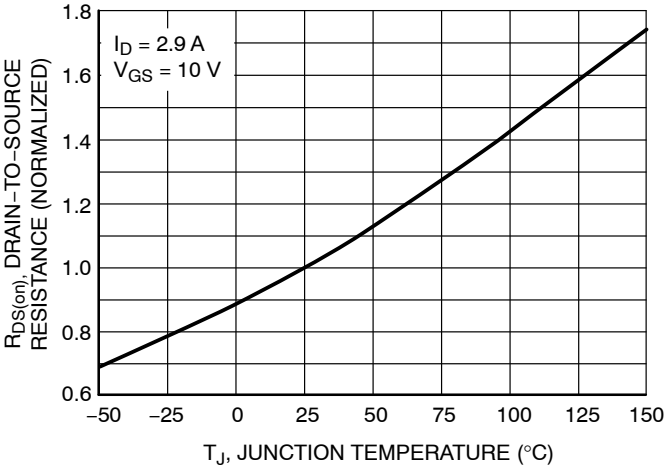


Figure 5. On−Resistance Variation with Temperature

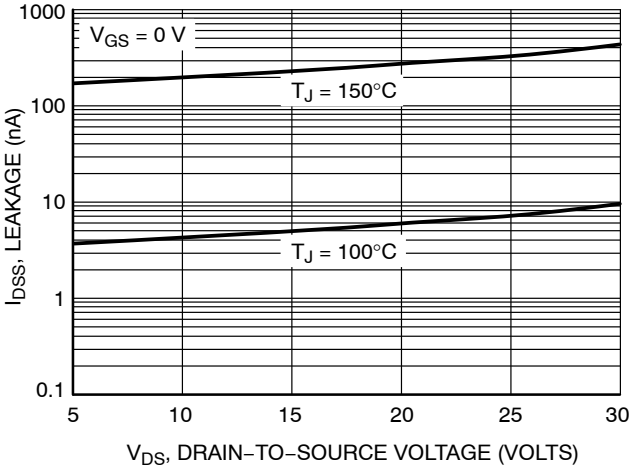


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL PERFORMANCE CURVES

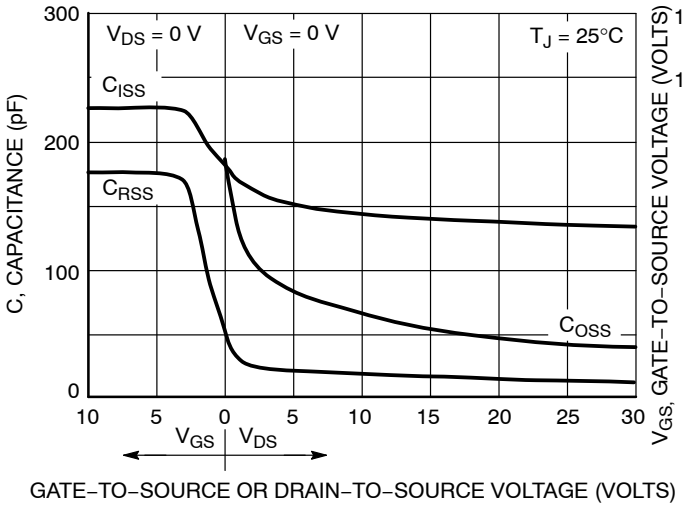


Figure 7. Capacitance Variation

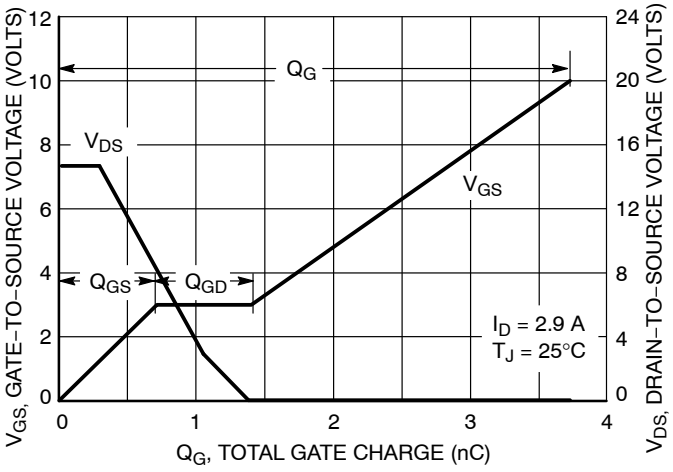


Figure 8. Gate−to−Source and Drain−to−Source Voltage vs. Total Charge

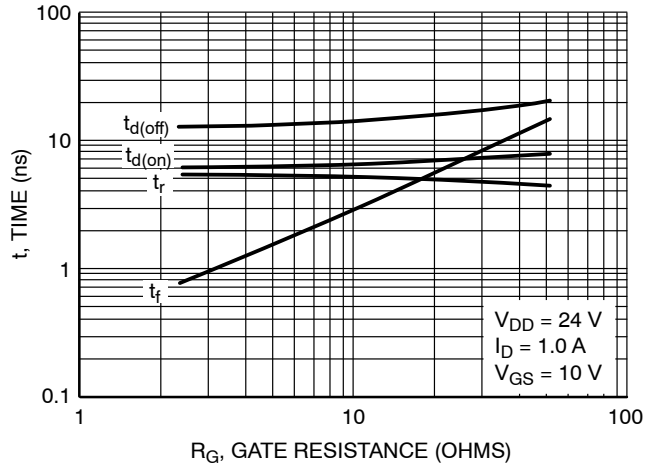


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

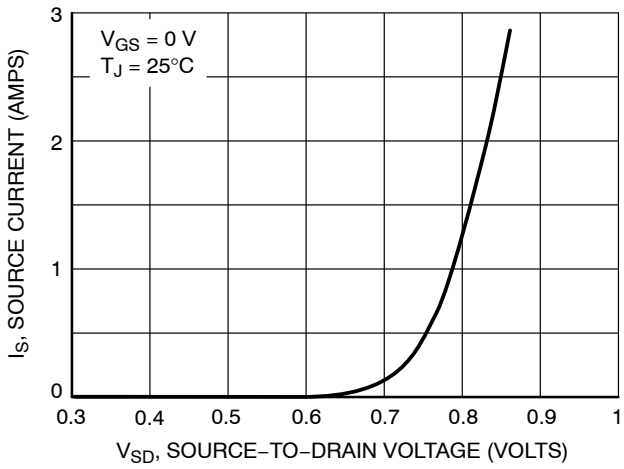


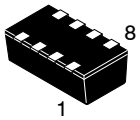
Figure 10. Diode Forward Voltage vs. Current

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

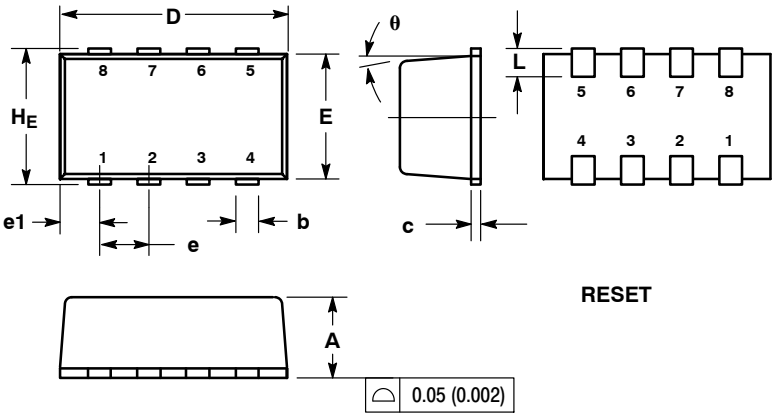
ON Semiconductor®

ChipFET™
CASE1206A−03
ISSUE K

DATE 19 MAY 2009



SCALE 1:1



RESET

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MOLD GATE BURRS SHALL NOT EXCEED 0.13 MM PER SIDE.
4. LEADFRAME TO MOLDED BODY OFFSET IN HORIZONTAL AND VERTICAL SHALL NOT EXCEED 0.08 MM.
5. DIMENSIONS A AND B EXCLUSIVE OF MOLD GATE BURRS.
6. NO MOLD FLASH ALLOWED ON THE TOP AND BOTTOM LEAD SURFACE.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	1.00	1.05	1.10	0.039	0.041	0.043
b	0.25	0.30	0.35	0.010	0.012	0.014
c	0.10	0.15	0.20	0.004	0.006	0.008
D	2.95	3.05	3.10	0.116	0.120	0.122
E	1.55	1.65	1.70	0.061	0.065	0.067
e	0.65 BSC			0.025 BSC		
e1	0.55 BSC			0.022 BSC		
L	0.28	0.35	0.42	0.011	0.014	0.017
H_E	1.80	1.90	2.00	0.071	0.075	0.079
θ	5° NOM			5° NOM		

STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. GATE
5. SOURCE
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 2:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

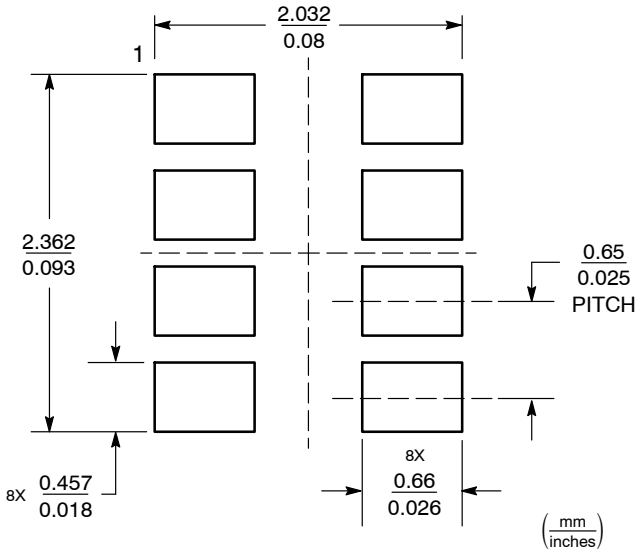
STYLE 3:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 4:
PIN 1. COLLECTOR
2. COLLECTOR
3. COLLECTOR
4. BASE
5. EMITTER
6. COLLECTOR
7. COLLECTOR
8. COLLECTOR

STYLE 5:
PIN 1. ANODE
2. ANODE
3. DRAIN
4. DRAIN
5. SOURCE
6. GATE
7. CATHODE
8. CATHODE

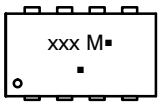
STYLE 6:
PIN 1. ANODE
2. DRAIN
3. DRAIN
4. GATE
5. SOURCE
6. DRAIN
7. DRAIN
8. CATHODE / DRAIN

SOLDERING FOOTPRINT



Basic Style

GENERIC MARKING DIAGRAM*



xxx = Specific Device Code
M = Month Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present.

OPTIONAL SOLDERING FOOTPRINTS ON PAGE 2

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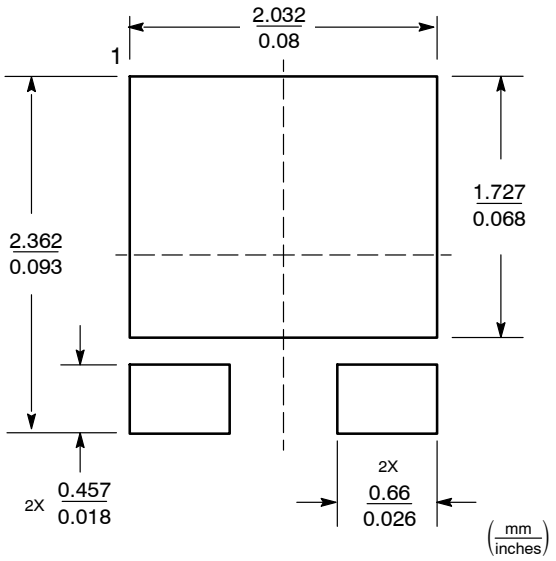
DESCRIPTION:	**ChipFET**	**PAGE 1 OF 2**

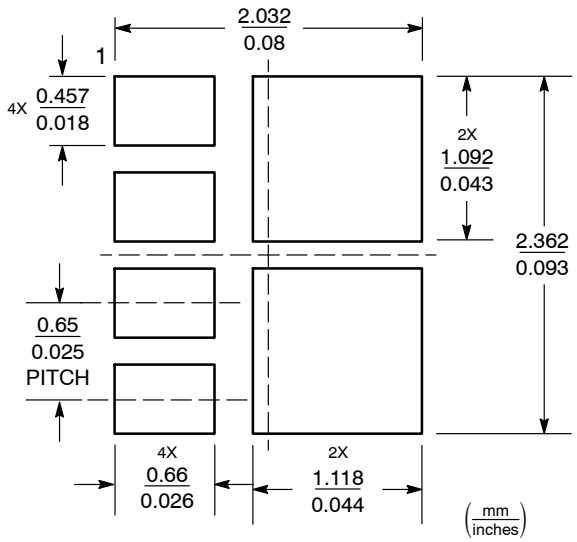
ChipFET™
CASE 1206A−03
ISSUE K

DATE 19 MAY 2009

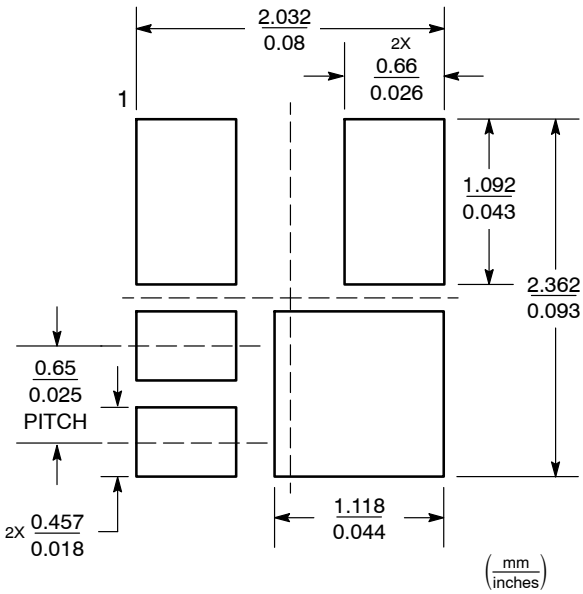
ADDITIONAL SOLDERING FOOTPRINTS*



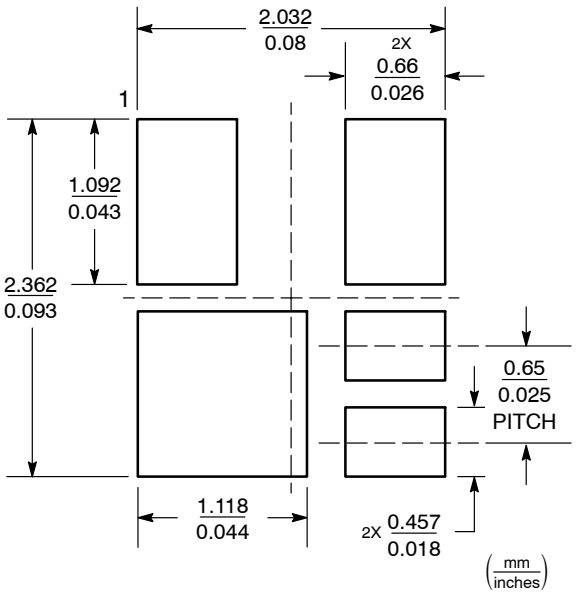
Styles 1 and 4



Style 2



Style 3



Style 5

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	**ChipFET**	**PAGE 2 OF 2**

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