NCP4353, NCP4354

Secondary Side SMPS OFF Mode Controller for Low Standby Power

The NCP4353/4 is a secondary side SMPS controller designed for use in applications which require extremely low no load power consumption. The device is capable of detecting “no load” conditions and entering the power supply into a low consumption OFF mode. During OFF mode, the primary side controller is turned off and energy is provided by the output capacitors thus eliminating the power consumption required to maintain regulation. During OFF mode, the output voltage relaxes and is allowed to decrease to an adjustable level. Once more energy is required, the NCP4353/4 automatically restarts the primary side controller. The NCP4353/4 controls the primary side controller with an “Active OFF” signal, meaning that it drives optocoupler current during OFF mode to pull−down the FB pin of the primary controller.

During normal power supply operation, the NCP4353/4 provides integrated voltage feedback regulation, replacing the need for a shunt regulator. The A versions include a current regulation loop in addition to voltage regulation. Feedback control as well as ON/OFF signal can be provided with only one optocoupler.

The NCP4354 includes a LED driver pin implemented with an open drain MOSFET driven by a 1 kHz square wave with a 12.5% duty cycle when primary side is in regulation for indication purpose.

The NCP4353 is available in TSOP−6 package while the NCP4354 is available in SOIC−8 package.

Features

- Operating Input Voltage Range: 2.5 V to 36.0 V
- Supply Current < 100 μA
- ±0.5% Reference Voltage Accuracy (T_J = 25°C)
- Constant Voltage and Constant Current (A versions) Control Loop
- Indication LED PWM Modulated Driver (NCP4354x)
- Designed for use with NCP1246 Fixed Frequency PWM Controller
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Offline Adapters for Notebooks, Game Stations and Printers
- High Power AC−DC Converters for TVs, Set−Top Boxes, Monitors, etc.

DEVICE OPTIONS

	NCP4353A	NCP4353B	NCP4354A	NCP4354B
Adjustable V_{min}	No	Yes	Yes	Yes
Current Regulation	Yes	No	Yes	No
LED Driver	No	No	Yes	Yes
Package	TSOP−6	TSOP−6	SOIC−8	SOIC−8

ON Semiconductor®

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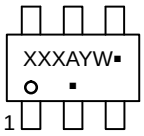
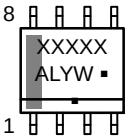
MARKING DIAGRAMS

TSSOP−6
CASE 318G



SOIC−8
CASE 751

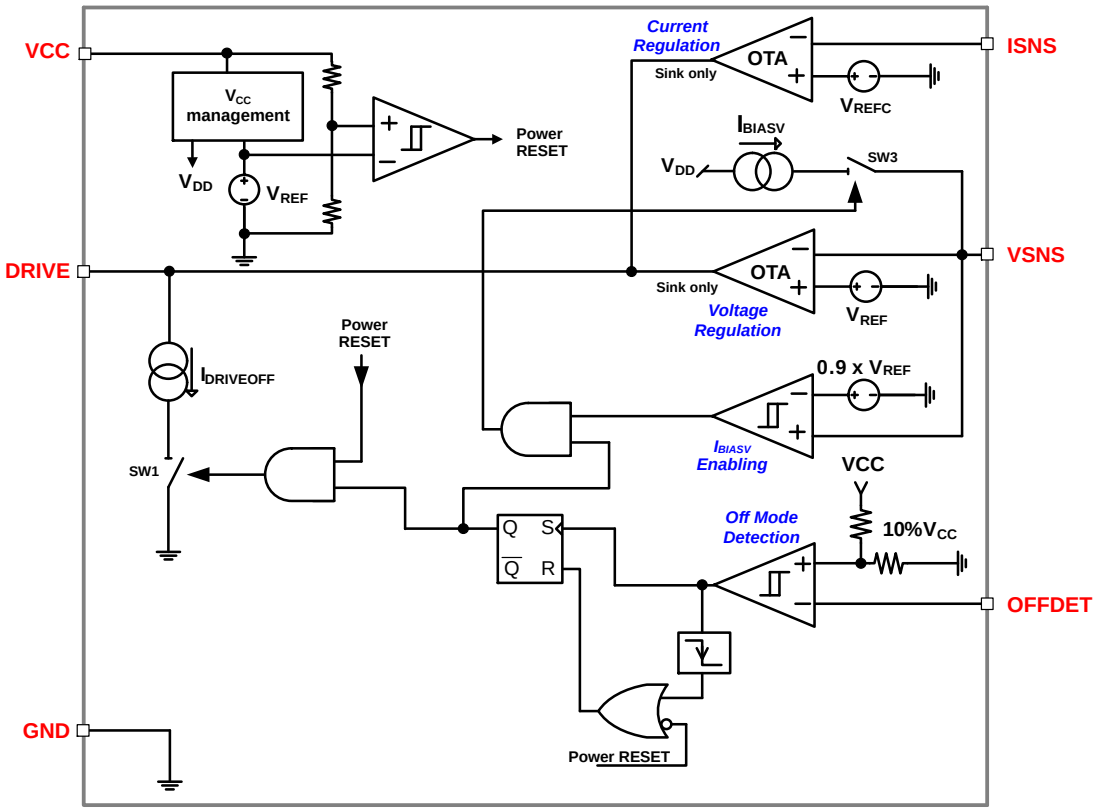


A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

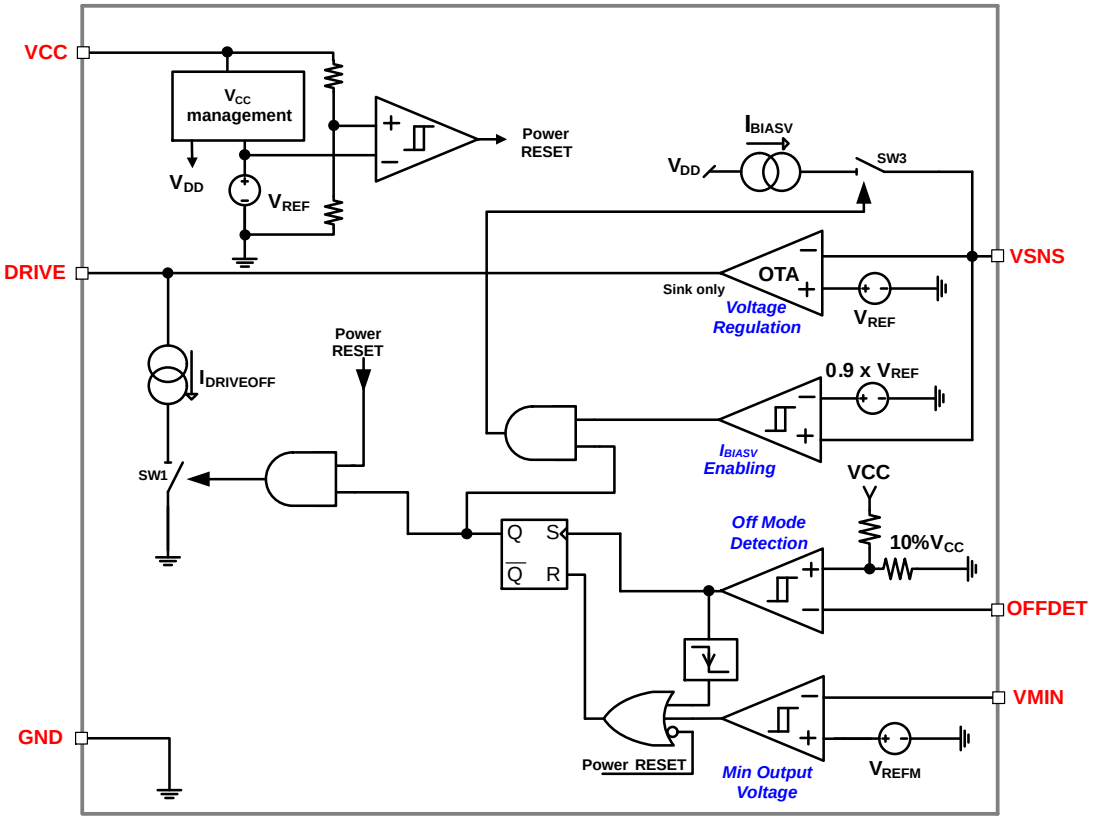
(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 15 of this data sheet.

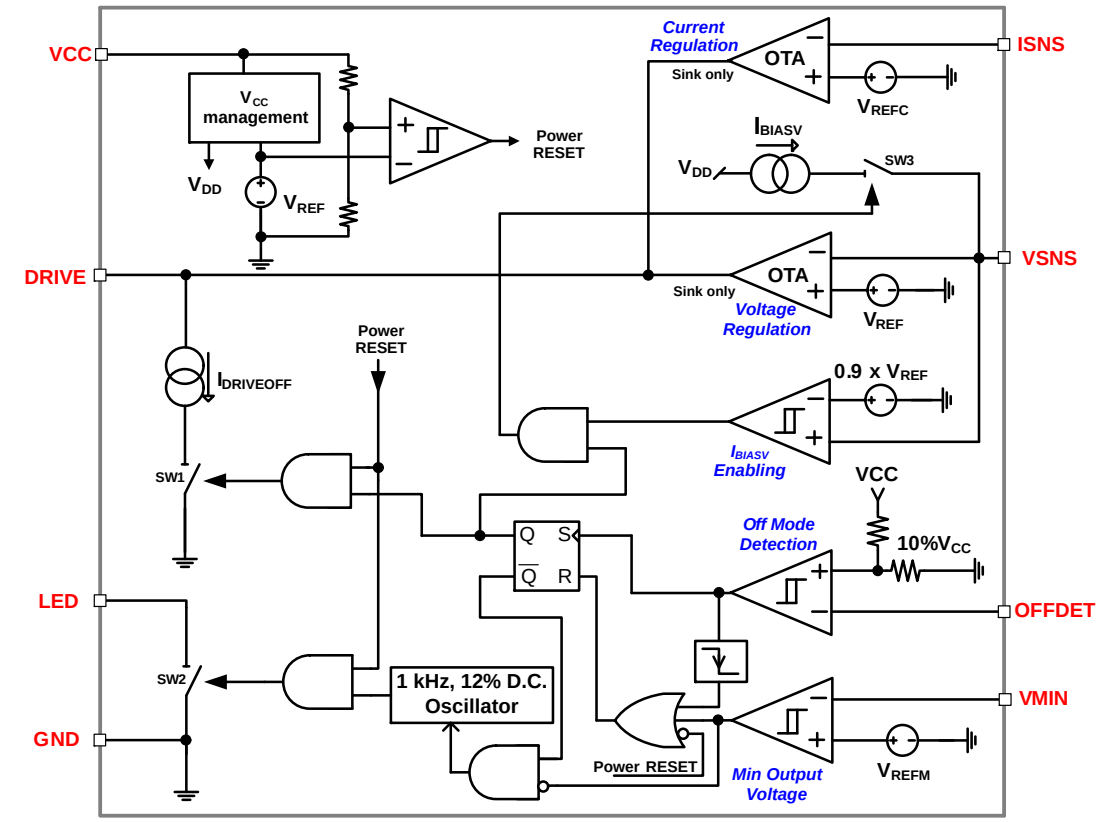


NCP4353A

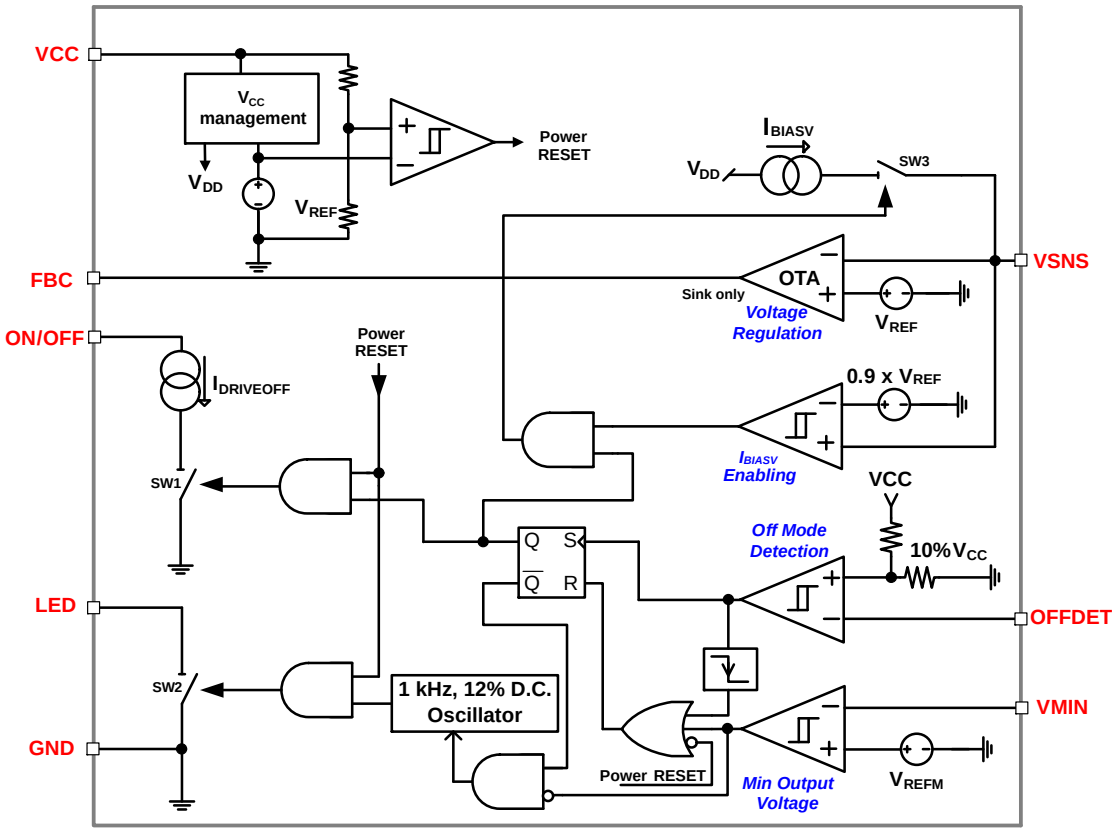


NCP4353B

Figure 1. Simplified Block Diagrams NCP4353A and NCP4353B



NCP4354A



NCP4354B

Figure 2. Simplified Block Diagrams NCP4354A and NCP4354B

PIN FUNCTION DESCRIPTION

NCP4353A	NCP4353B	NCP4354A	NCP4354B	Pin Name	Description
1	1	8	8	VCC	Supply voltage pin
2	2	7	7	GND	Ground
6	6	1	1	VSNS	Output voltage sensing pin, connected to output voltage divider
5	5	2	2	OFFDET	OFF mode detection input. Voltage divider provides adjustable off mode detection threshold
−	4	3	3	VMIN	Minimum output voltage adjustment
4	−	4	−	ISNS	Current sensing input for output current regulation, connect it to shunt resistor in ground branch.
−	−	5	4	LED	PWM LED driver output. Connected to LED cathode with current define by external serial resistance
−	−	−	6	FBC	Output of current sinking OTA amplifier or amplifiers driving feedback optocoupler's LED. Connect here compensation network (networks) as well.
−	−	−	5	ON/OFF	OFF mode current sink. This output keeps primary control pin at low level in off mode.
3	3	6	−	DRIVE	Combination of FBC and ON/OFF pins

ABSOLUTE MAXIMUM RATINGS

Rating		Symbol	Value	Unit
Input Voltage		V_{CC}	−0.3 to 40	V
DRIVE, ON/OFF, FBC, LED Voltage		V_{DRIVE}, V_{ONOFF}, V_{FBC}, V_{LED}	−0.3 to V_{CC} + 0.3	V
VSNS, ISNS, OFFDET, VMIN Voltage		V_{SNS}, V_{ISNS}, V_{OFFDET}, V_{MIN}	−0.3 to 10	V
LED Current		I_{LED}	10	mA
Thermal Resistance − Junction−to−Air (Note 1)	NCP4353A NCP4353B NCP4354A NCP4354B	$R_{\theta JA}$	315 324 260 277	°C/W
Junction Temperature		T_J	−40 to 150	°C
Storage Temperature		T_{STG}	−60 to 150	°C
ESD Capability, Human Body Model (Note 2)		ESD_{HBM}	2000	V
ESD Capability, Machine Model (Note 2)		ESD_{MM}	250	V
ESD Capability, Charged Device Model (Note 2)		ESD_{CDM}	1000	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. 50 mm^2, 1.0 oz. Copper spreader.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per JESD22−A114F
   ESD Machine Model tested per JESD22−A115C
   ESD Charged Device Model tested per JESD22−C101F
   Latchup Current Maximum Rating tested per JEDEC standard: JESD78D.

ELECTRICAL CHARACTERISTICS

$0°C \le T_J \le 125°C$; V_{CC} = 15 V; unless otherwise noted. Typical values are at T_J = +25°C.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Maximum Operating Input Voltage		V_{CC}			36.0	V
VCC UVLO	V_{CC} rising	V_{CCUVLO}	3.3	3.5	3.7	V
	V_{CC} falling		2.3	2.5	2.7	
VCC UVLO Hysteresis		$V_{CCUVLOHYS}$	0.8	1.0		V
Quiescent Current in Regulation	NCP4353A	I_{CC}		101	125	μA
	NCP4353B			82	105	
	NCP4354A			118	145	
	NCP4354B			95	120	
Quiescent Current in OFF Mode	V_{SNS} < 1.12 V	$I_{CC,OFFmode}$		90	110	μA
VOLTAGE CONTROL LOOP OTA						
Transconductance	Sink current only	gm_V		1		S
Reference Voltage	2.8 V ≤ V_{CC} ≤ 36.0 V, T_J = 25°C	V_{REF}	1.244	1.250	1.256	V
	2.8 V ≤ V_{CC} ≤ 36.0 V, T_J = 0 − 85°C		1.240	1.250	1.264	
	2.8 V ≤ V_{CC} ≤ 36.0 V, T_J = 0 − 125°C		1.230	1.250	1.270	
Sink Current Capability	In regulation, V_{DRIVE} or V_{FBC} > 1.5 V	I_{SINKV}	2.5			mA
	In OFF mode, V_{DRIVE} or V_{FBC} > 1.5 V		1.2	1.5	2.0	mA
Inverting Input Bias Current	In regulation, V_{SNS} = V_{REF}	I_{BIASV}	−100		100	nA
	In OFF mode, V_{SNS} > 1.12 V		−13	−11	−10	μA
Inverting Input Bias Current Threshold	In OFF mode	$V_{SNSBIASTH}$	1.07	1.12	1.17	V
CURRENT CONTROL LOOP OTA (NCP435xA only)						
Transconductance	Sink current only	gm_C		3		S
Reference Voltage		V_{REFC}	60	62.5	65	mV
Sink Current Capability	V_{DRIVE} or V_{FBC} > 1.5 V	I_{SINKC}	2.5			mA
Inverting Input Bias Current	I_{SNS} = V_{REFC}	I_{BIASC}	−100		100	nA
MINIMUM VOLTAGE COMPARATOR (except NCP4353A)						
Threshold Voltage		V_{REFM}	355	377	400	mV
Hysteresis	Output change from logic high to logic low	V_{MINH}		40		mV
OFF MODE DETECTION COMPARATOR						
Threshold Value	2.5 V ≤ V_{CC} ≤ 36.0 V	$V_{OFFDETTH}$		10% V_{CC}		V
	V_{CC} = 15 V		1.47	1.50	1.53	
Hysteresis	Output change from logic high to logic low	$V_{OFFDETH}$		40		mV
LED DRIVER (NCP4354x only)						
Switching Frequency		f_{SWLED}		1		kHz
Duty Cycle		D_{LED}	10.0	12.5	15.0	%
Switch Resistance	I_{LED} = 5 mA	R_{SW2}		50		Ω
OFF MODE CONTROL						
Sink Current	In OFF mode, V_{DRIVE} or V_{ONOFF} > 0.6 V	$I_{DRIVEOFF}$	140	160	180	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

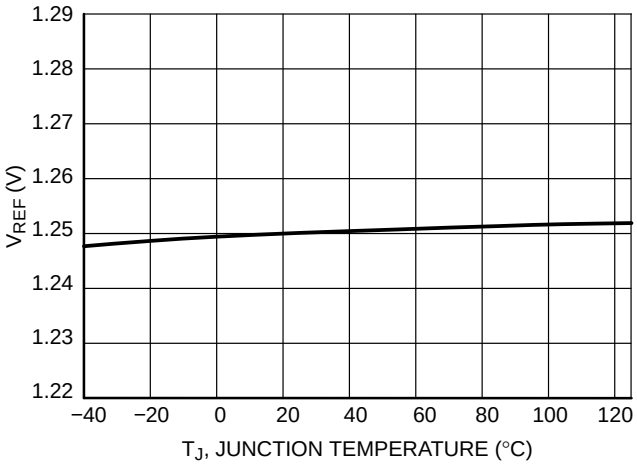


Figure 3. V_{REF} at V_{CC} = 15 V

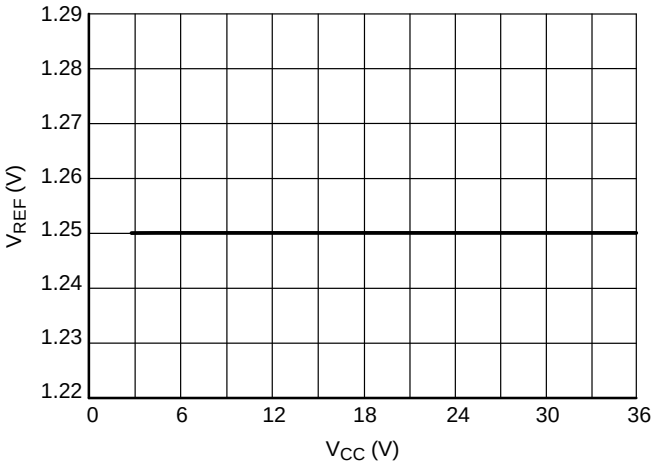


Figure 4. V_{REF} at T_J = 25°C

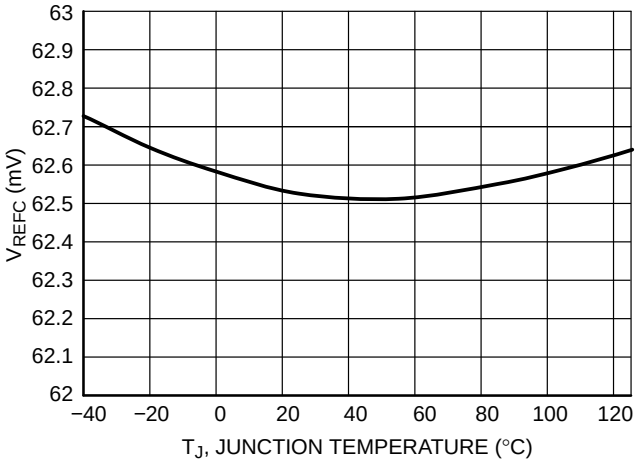


Figure 5. V_{REFC} at V_{CC} = 15 V

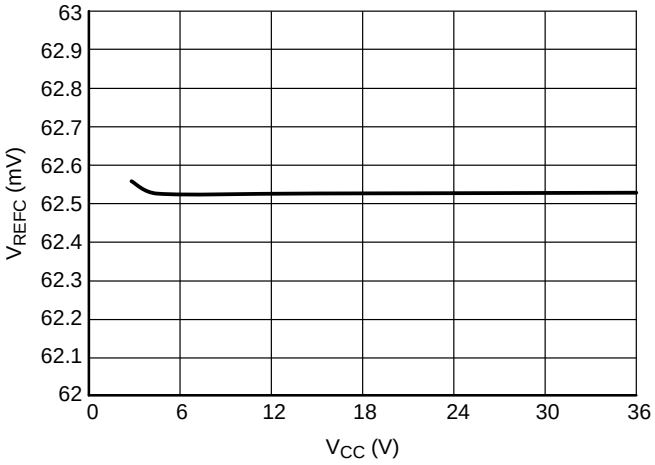


Figure 6. V_{REFC} at T_J = 25°C

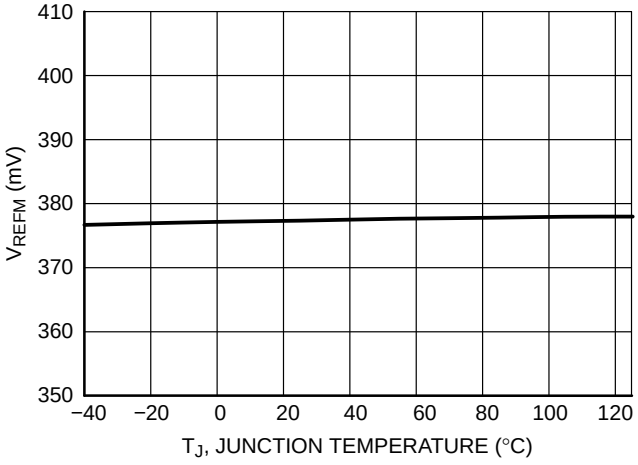


Figure 7. V_{REFM} at V_{CC} = 15 V

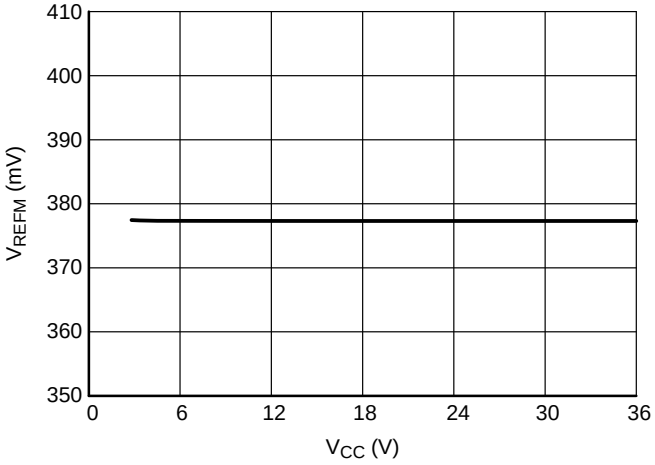


Figure 8. V_{REFM} at T_J = 25 °C

TYPICAL CHARACTERISTICS

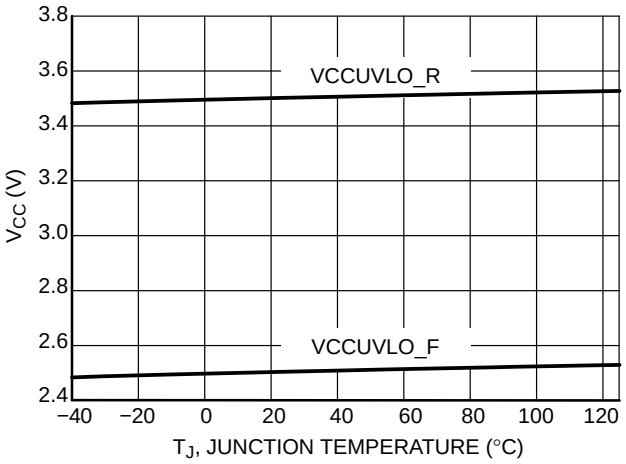


Figure 9. V_{CCUVLO}

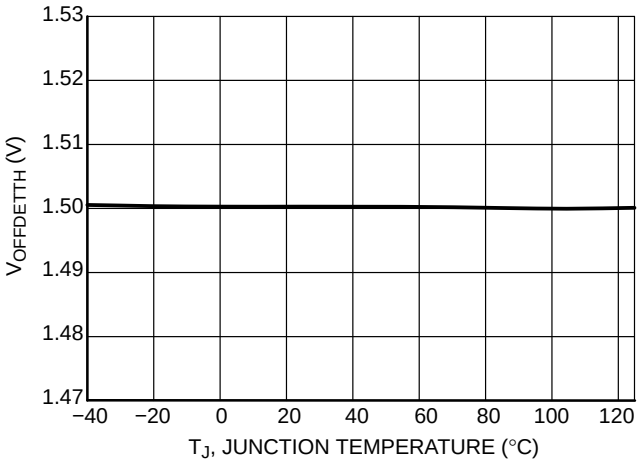


Figure 10. $V_{OFFDETTH}$ at V_{CC} = 15 V

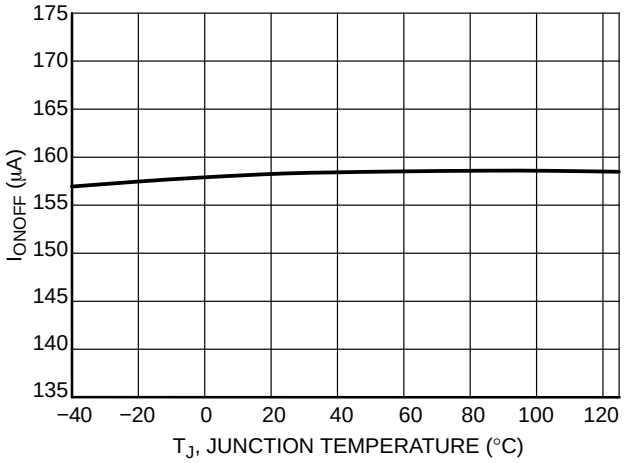


Figure 11. I_{ONOFF} at V_{CC} = 15 V

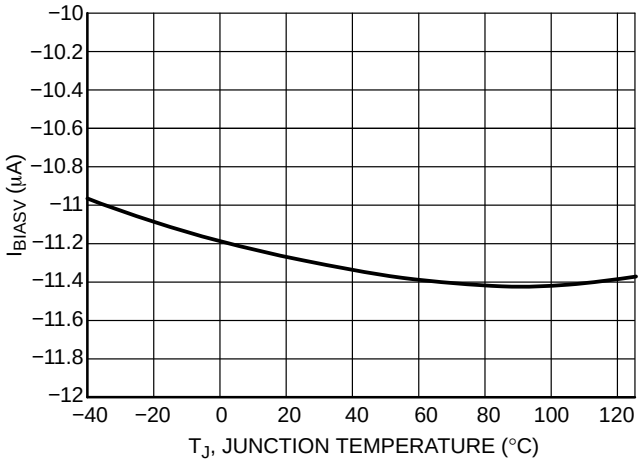


Figure 12. I_{BIASV} at V_{CC} = 15 V, V_{SNS} > $V_{SNSBIASTH}$

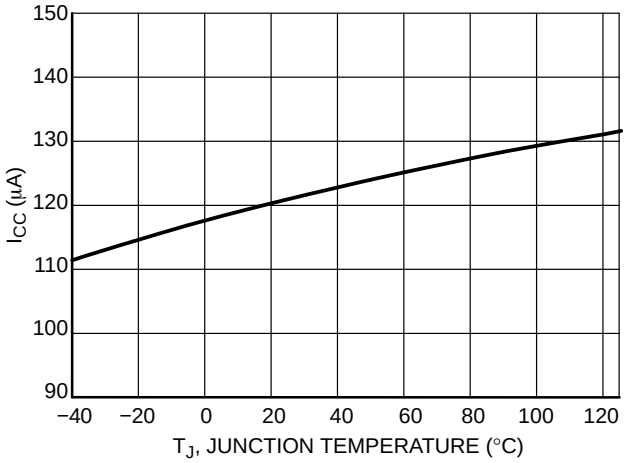


Figure 13. I_{CC} in Regulation at V_{CC} = 15 V for NCP4354A

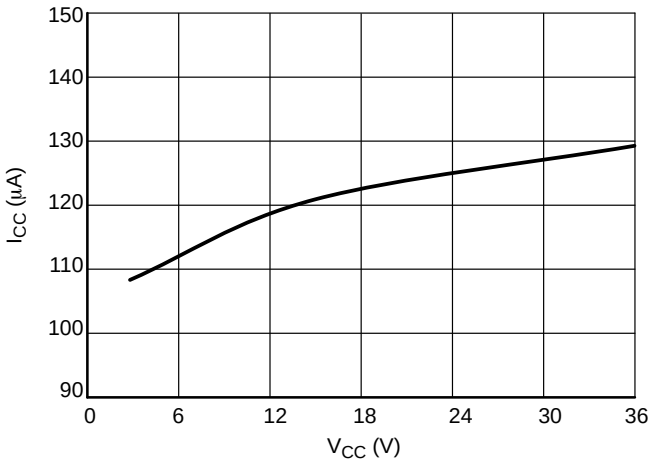


Figure 14. I_{CC} in Regulation at T_J = 25°C for NCP4354A

TYPICAL CHARACTERISTICS

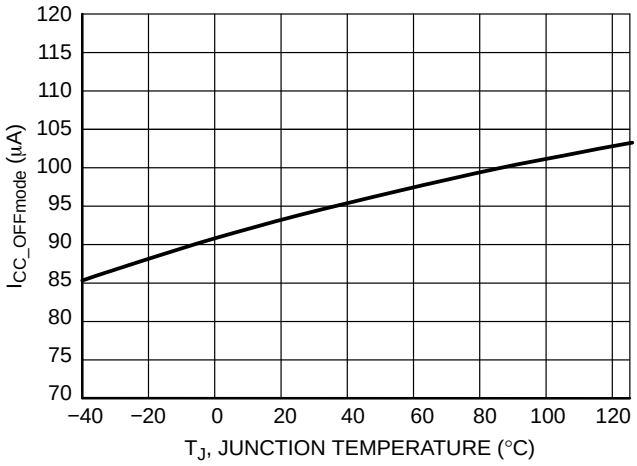


Figure 15. I_{CC} in OFF Mode at V_{CC} = 15 V, V_{SNS} < $V_{SNSBIASTH}$, for NCP4354A

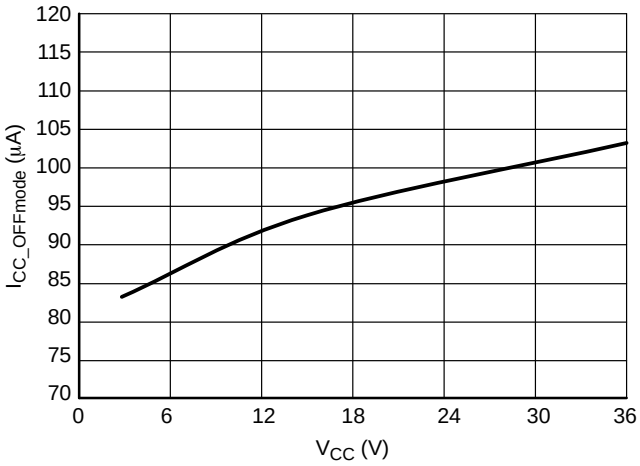


Figure 16. I_{CC} in OFF Mode at T_J = 25°C, V_{SNS} < $V_{SNSBIASTH}$, for NCP4354A

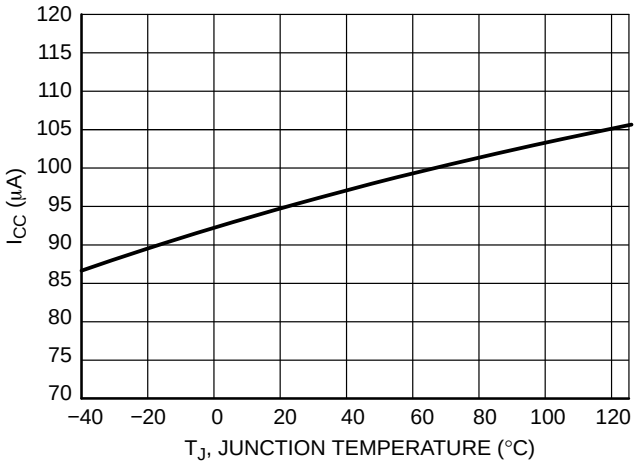


Figure 17. I_{CC} in Regulation at V_{CC} = 15 V for NCP4354B

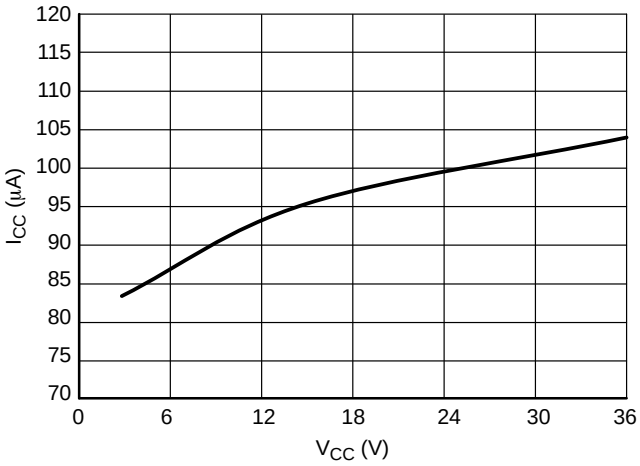


Figure 18. I_{CC} in Regulation at T_J = 25°C for NCP4354B

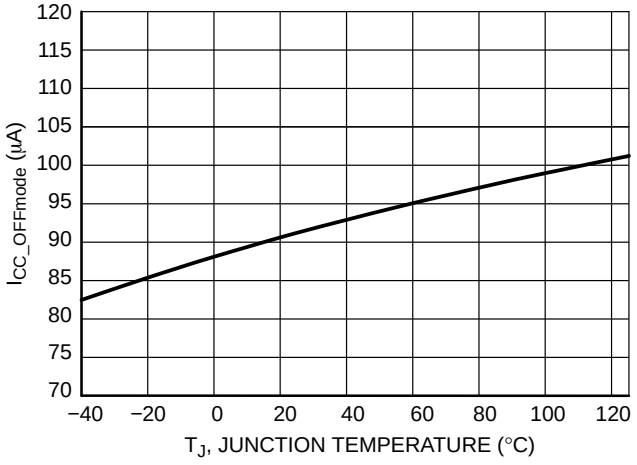


Figure 19. I_{CC} in OFF Mode at V_{CC} = 15 V, V_{SNS} < $V_{SNSBIASTH}$, for NCP4354B

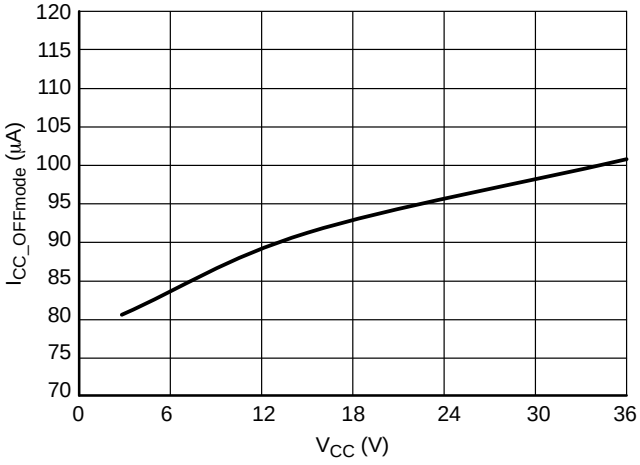


Figure 20. I_{CC} in OFF Mode at T_J = 25°C, V_{SNS} < $V_{SNSBIASTH}$, for NCP4354B

TYPICAL CHARACTERISTICS

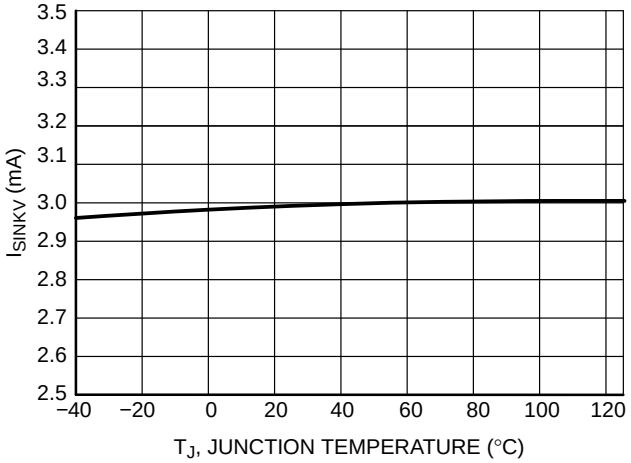


Figure 21. Voltage OTA Current Sink Capability in Regulation

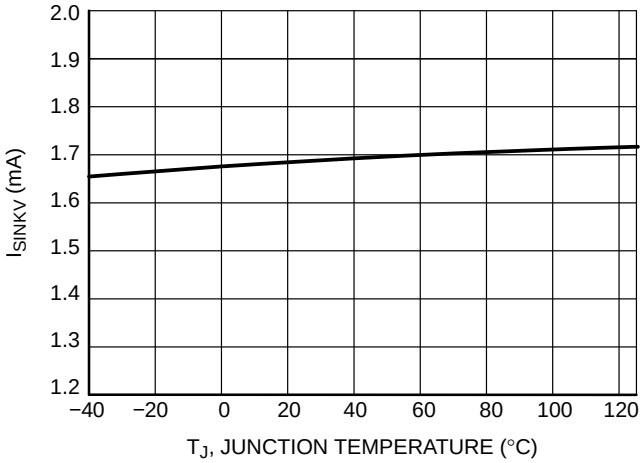


Figure 22. Voltage OTA Current Sink Capability in OFF Mode

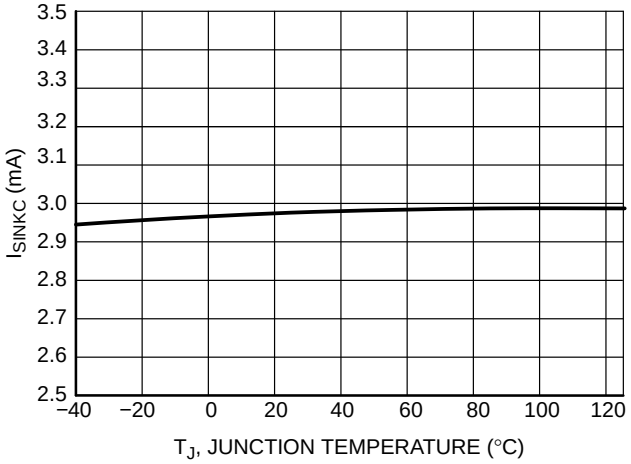


Figure 23. Current OTA Current Sink Capability

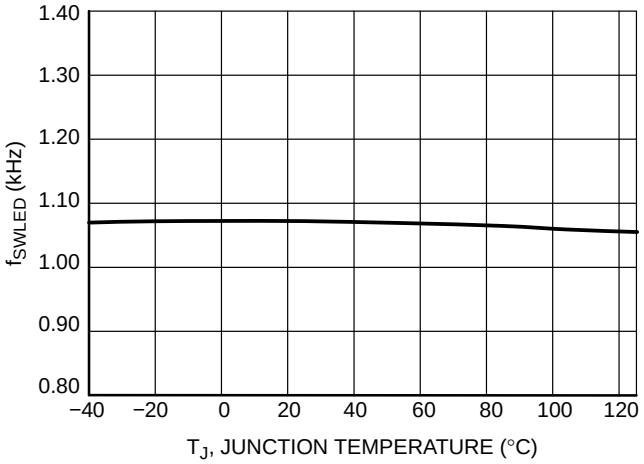


Figure 24. LED Switching Frequency at V_{CC} = 15 V

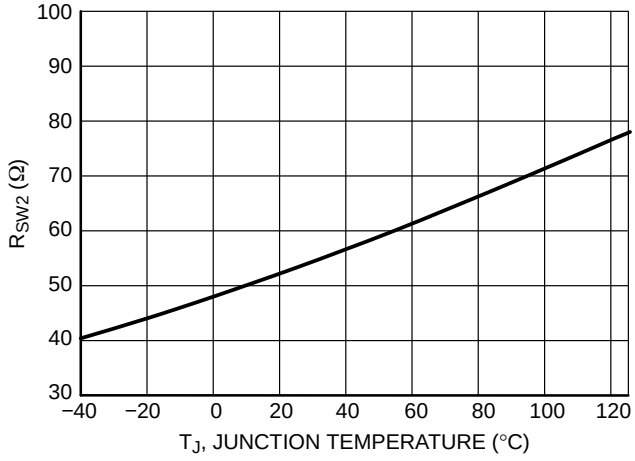


Figure 25. R_{SW2} at V_{CC} = 15 V

APPLICATION INFORMATION

A typical application circuit for NCP435x series is shown in Figure 28, done with an imaginary IC with all features in one. Pin functions are available in pin description table.

Simplified typical application circuit for NCP4353B that shows only available features in this IC is shown in Figure 27. Figure 29 shows possible connection of the NCP4353B to flyback primary controller.

IC will be derived in multiple versions with different features for each of them.

Power Supply

The NCP435x is designed to operate from a single supply up to 36 V. It starts to operate when VCC voltage reaches 3.5 V and stops when VCC voltage drops below 2.5 V. V_{CC} can be supplied by direct connection to the VOUT voltage of the power supply. It is highly recommended to add a RC filter (R1 and C3) in series from VOUT to VCC pin to reduce voltage spikes and drops that are produced at the converter's output capacitors. Recommended values for this filter are 220 Ω and 1 μF.

Voltage Regulation Path

The output voltage is detected on the VSNS pin by the R4, R5 and R6 voltage divider. This voltage is compared with the internal precise voltage reference. The voltage difference is amplified by gm_V of the transconductance amplifier. The amplifier output current is connected to the FBC or DRIVE pin. The compensation network is also connected to this pin to provide frequency compensation for the voltage regulation path. This FBC (DRIVE) pin drives regulation optocoupler that provides regulation of primary side. The optocoupler is supplied via direct connection to VOUT line through resistor R2.

Regulation information is transferred through the optocoupler to the primary side controller where its FB pin is usually pulled down to reduce energy transferred to secondary output.

The VSNS voltage divider is shared with VMIN voltage divider. The shared voltage divider can be connected in two ways as shown in Figure 26. The divider type is selected based on the ratio between V_{MIN} and V_{OUT}. When the condition of Equation 1 is true, divider type 1 should be used.

$$V_{MIN} > \frac{V_{OUT} \times V_{REFM}}{V_{REF}} \qquad \text{(eq. 1)}$$

Output voltage for divider type 1 can be computed by Equation 2

$$V_{OUT} = V_{REF} \times \frac{R4 + R5 + R6}{R5 + R6} \qquad \text{(eq. 2)}$$

and for type 2 by Equation 3.

$$V_{OUT} = V_{REF} \times \frac{R4 + R5 + R6}{R6} \qquad \text{(eq. 3)}$$

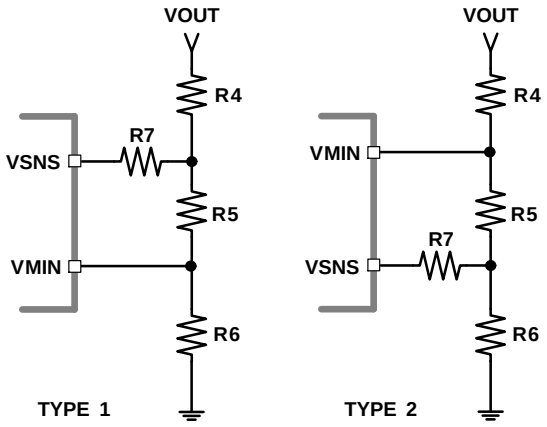


Figure 26. Shared Dividers Type

Current Regulation Path (A versions only)

The output current is sensed by the shunt resistor R12 in series with the load. Voltage drop on R12 is compared with internal precise voltage reference V_{REFC} at I_{SNS} transconductance amplifier input.

Voltage difference is amplified by gm_C to output current of amplifier, connected to FBC or DRIVE pin. Compensation network is connected between this pin and ISNS input to provide frequency compensation for current regulation path. Resistor R13 separates compensation network from sense resistor. Compensation network works into low impedance without this resistor that significantly decreases compensation network impact.

Current regulation point is set to current given by Equation 4.

$$I_{OUTLIM} = \frac{V_{REFC}}{R12} \qquad \text{(eq. 4)}$$

OFF Mode Detection

OFF mode operation is advantageous for ultra low or zero output current condition. The very long off time and the ultra low power mode of the whole regulation system greatly reduces the overall consumption.

The output voltage is varying between nominal and minimal in OFF mode. When output voltage decreases below set (except NCP4353A) minimum level, primary controller is switched on until output capacitor C1 is charged again to the nominal voltage.

The OFF mode detection is based on comparison of output voltage and voltage loaded with fixed resistances (D2, C2, R8 and R9). Figure 30 shows detection waveforms. When output voltage is loaded with very low current, primary controller goes into skip mode (primary controller stops switching for some time). While output capacitor C1 is discharged very slowly (no load condition), the capacitor C2

is discharged through a fixed load, by R8 and R9 faster than output voltage on C1.

Once OFFDET pin voltage is lower than $V_{OFFDETTH}$ (this threshold is derived from V_{OUT}), OFF mode is detected. In OFF mode SW1 is switched on to allow $I_{DRIVEOFF}$ current, going through ON/OFF pin (NCP4354B) or DRIVE pin, to keep switch off primary controller.

A higher sink current on primary FB pin is needed to keep primary controller FB below the skip level until the OFF mode is detected on primary side.

Despite output voltage on C1 may go down, the current I_{BIASV} injected into VSNS pin provides the requested offset (VSNS voltage is higher than V_{REF}). Primary IC should detect OFF mode before VSNS is lower than 90% of V_{REF} while I_{BIASV} is switched off to reduce consumption.

This offset, defined by R7 and the internal current source, should be large enough to secure off mode detection of the primary controller and avoid restart when $V_{SNS} < V_{REF}$.

Minimum Output Voltage Detection (Except NCP4353A)

Minimum output voltage level defines primary controller restart from OFF mode. It can be set by shared voltage divider with voltage regulation loop. When VMIN voltage drops below V_{REFM}, OFF mode is ended and primary controller restarts.

Minimum voltage level is given by Equation 5 for divider type 1

$$V_{MIN} = V_{REF} \times \frac{R4 + R5 + R6}{R6} \qquad \text{(eq. 5)}$$

and for type 2 by Equation 6.

$$V_{MIN} = V_{REF} \times \frac{R4 + R5 + R6}{R5 + R6} \qquad \text{(eq. 6)}$$

NCP4353A has no external adjustment and uses the internal minimum voltage level specified by minimum falling operation supply voltage.

LED Driver (NCP4354x only)

LED driver is active when VCC is higher than V_{CCMIN} and output voltage is in regulation (driver is off in OFF mode). LED driver consists of an internal power switch controlled by a PWM modulated logic signal and an external current limiting resistor R3. LED current can be computed by Equation 7.

$$I_{LED} = \frac{V_{OUT} - V_{F\_LED}}{R3} \qquad \text{(eq. 7)}$$

PWM modulation is used to increase efficiency of LED.

Operation in OFF Mode Description

Operation waveforms in off mode and transition into OFF mode with NCP1246 primary controller are shown in Figure 31.

Figure shows waveforms from the first start (1) of the convertor. At first, primary controller's DSS charges VCC capacitor over the UVLO level (2). When primary V_{CC} is over UVLO level (3), primary controller starts to operate. VCC capacitor is charged above DSS level from auxiliary winding, V_{OUT} is slowly rising according to primary controller start up ramp to nominal voltage (4).

Primary FB pin voltage is above regulation range until V_{OUT} is at set level. Once V_{OUT} is at set level, the secondary controller starts to sink current from optocoupler LED's and primary FB voltage is stabilized in regulation region. With nominal output power (without skip mode) OFFDET pin voltage is higher than $V_{OFFDETTH}$ (typically 10% of V_{CC}).

After some time, the load current decreases to low level (5) and primary convertor uses skip mode (6) to keep regulation of output voltage at set level. The skip mode consists of few switching cycles followed by missing ones to provide limited energy by light load. The number of missing cycles allows regulation for any output power.

While both C1 and C2 are discharged during the missing cycles, C2 discharge will be faster than C1 without output current, V_{OFFDET} drops below $V_{OFFDETTH}$ and OFF mode is detected (7). This situation is shown in Figure 30 in detail. When OFF mode is detected, internal pull−up current I_{BIASV} is switch on (7), VSNS voltage increases (due to I_{BIASV}) and voltage amplifier sinks full current to keep primary FB voltage below skip level until OFF mode is detected by the primary side controller (8). Current into ONOFF pin or DRIVE pin begins to flow at the same time, when entering into OFF mode (7). When OFF mode is detected by primary side controller (8a), primary FB injected current decreases to a lower level to reduce overall power consumption. Optocoupler current, can also be reduced from that time to keep the level below restart level. Secondary side controller decreases optocoupler current (voltage transconductance amplifier stops to sink current) when VSNS voltage drops below V_{REF} (9) and I_{BIASV} is also switch off when V_{SNS} is lower than 90% of V_{REF} to reduce overall consumption. This point is defined by I_{BIASV} current, R6, R4 and R5 resistors and discharging time of output capacitor C1. Discharging of C1 continues (10) until output voltage drops below level set by voltage divider at VMIN pin (except NCP4353A where minimum V_{OUT} is defined only by VCC UVLO) (11). ONOFF current stops and thanks to internal pull−up, the primary FB voltage rises above restart level (12) and primary controller starts switching (13). Output capacitor C1 is recharged (14) to set voltage. If there is still light load condition primary controller goes to skip mode (15) again and after some time secondary controller detects OFF mode by very light or no load condition (16) and whole cycle is repeated.

Fast Restart From OFF Mode

The IC ends OFF mode when a load is connected to the output and V_{OUT} is discharged to V_{MIN} level. There exists another connection that allows transition to normal mode faster without waiting some time for V_{OUT} to discharge to V_{MIN}. This schematic is shown at Figure 32. The basic idea is that C3 is discharged by the IC faster than C1 by output

load in OFF mode. When an output load is applied, capacitor C1 is discharged faster and this creates a voltage drop at D8. When there is enough voltage at D8, T2 is opened and current is injected into the OFFDET divider through R17. OFFDET voltage higher than 10% of V_{CC} ends OFF mode and ON/OFF current stops. Primary controller leaves OFF mode because voltage at its FB pin rises above OFF mode end level and switching resumes.

Normal operation waveforms for typical load detection connection and improved load detection waveforms are shown in Figure 33.

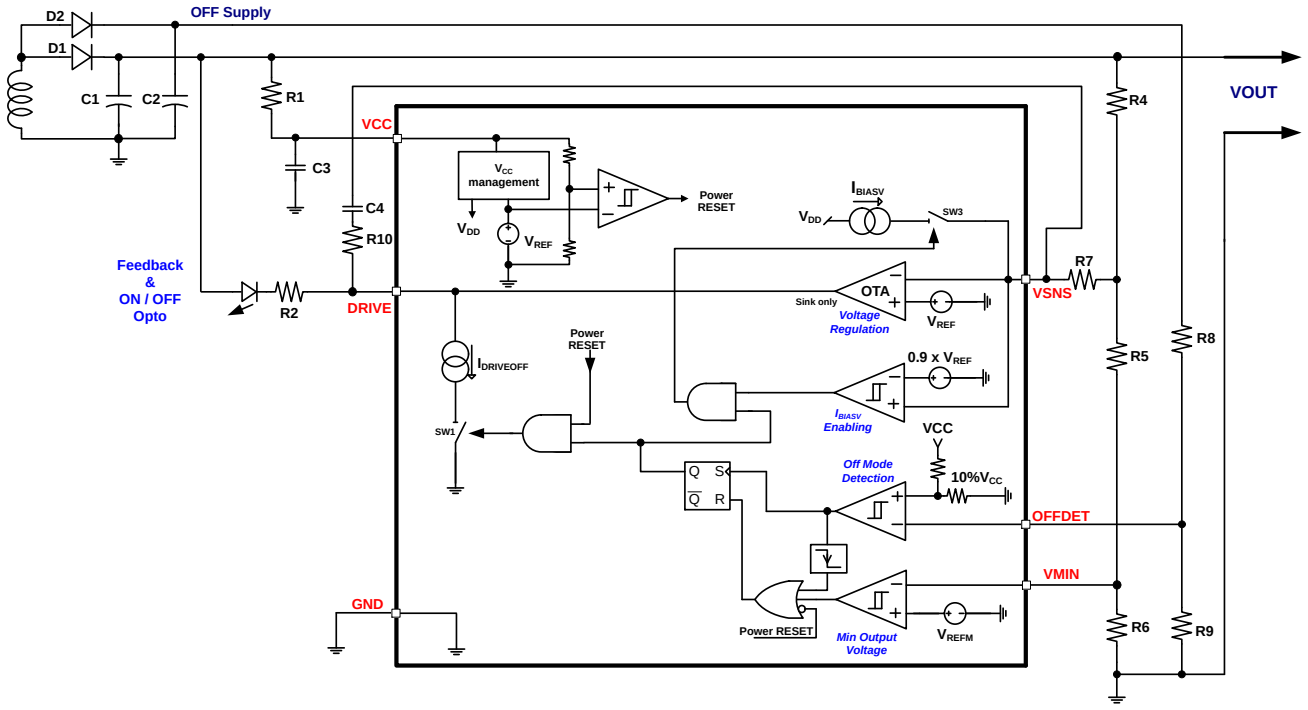


Figure 27. Typical Application Schematic for NCP4353B

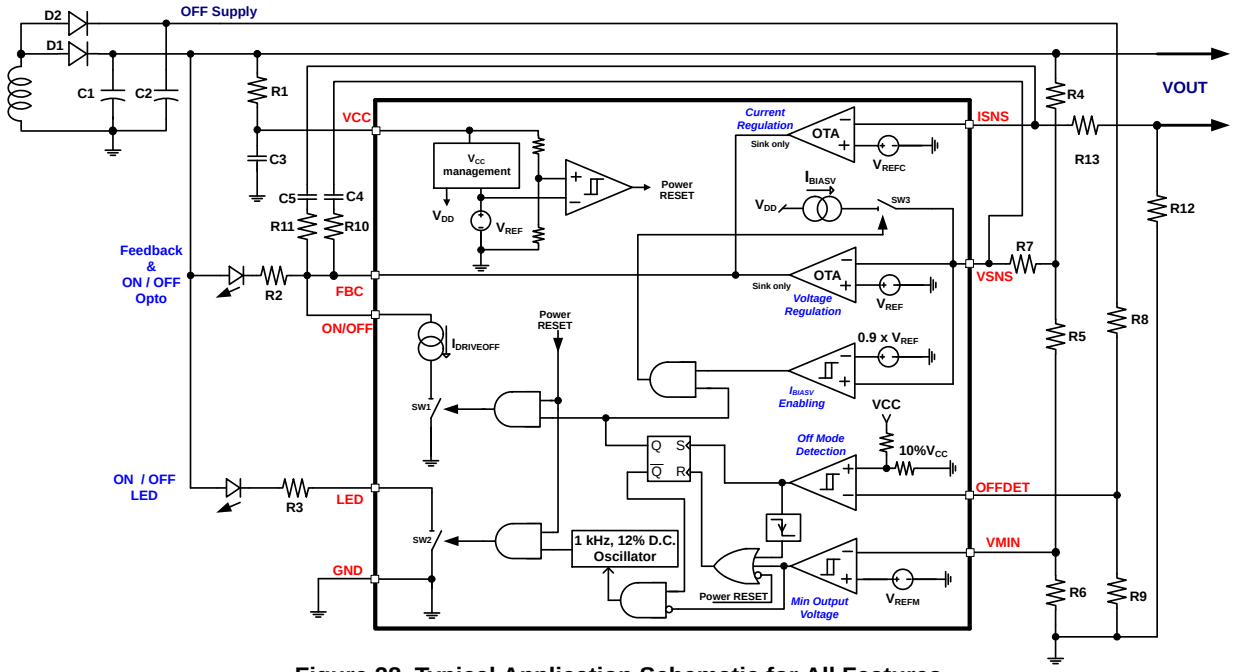


Figure 28. Typical Application Schematic for All Features

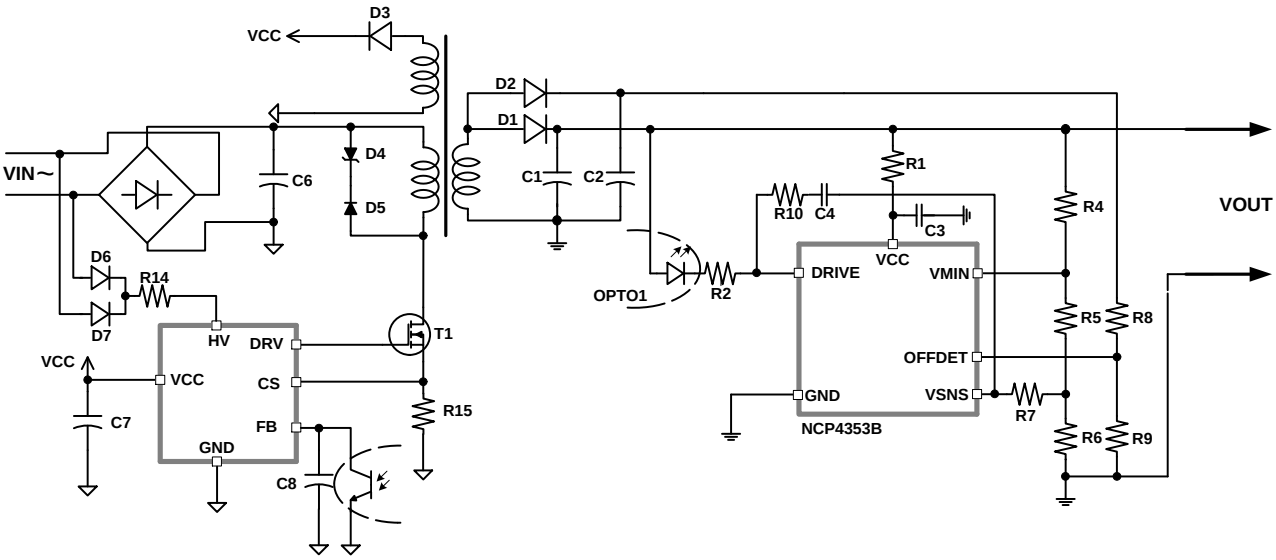


Figure 29. Typical Application Schematic for NCP4353B with Flyback

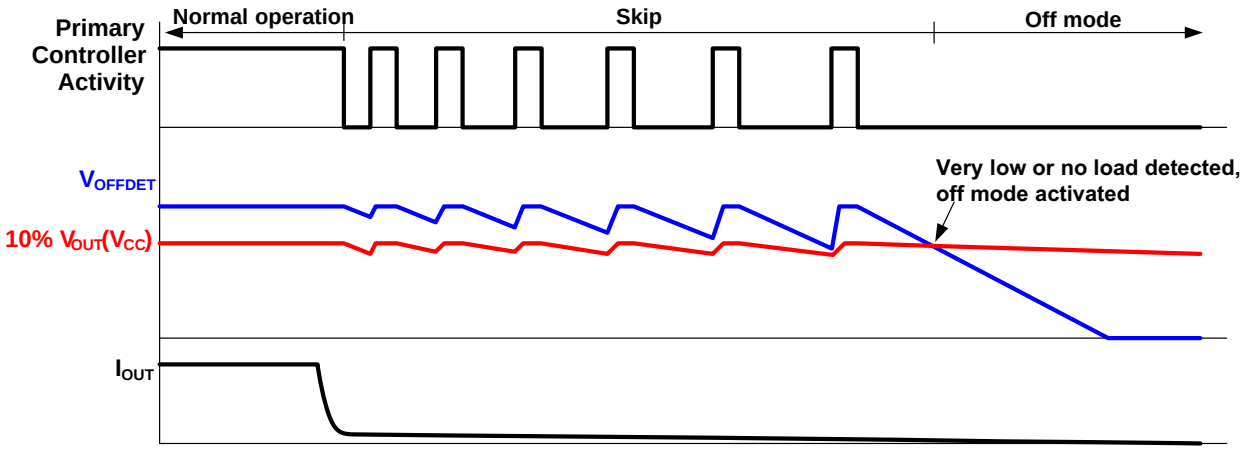


Figure 30. OFF Mode Detection

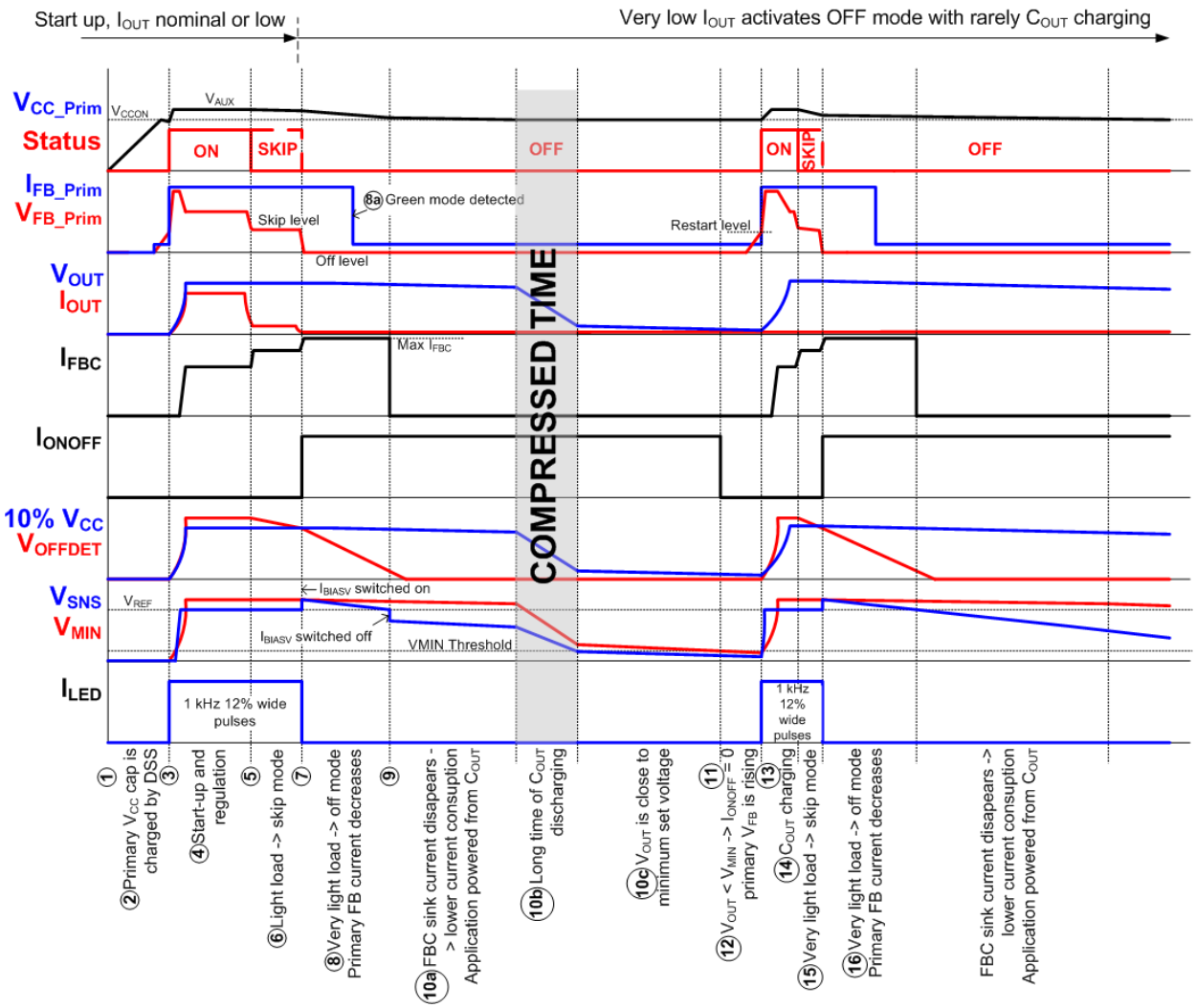


Figure 31. Typical Application States and Waveforms in OFF Mode with NCP1246 Primary Controller

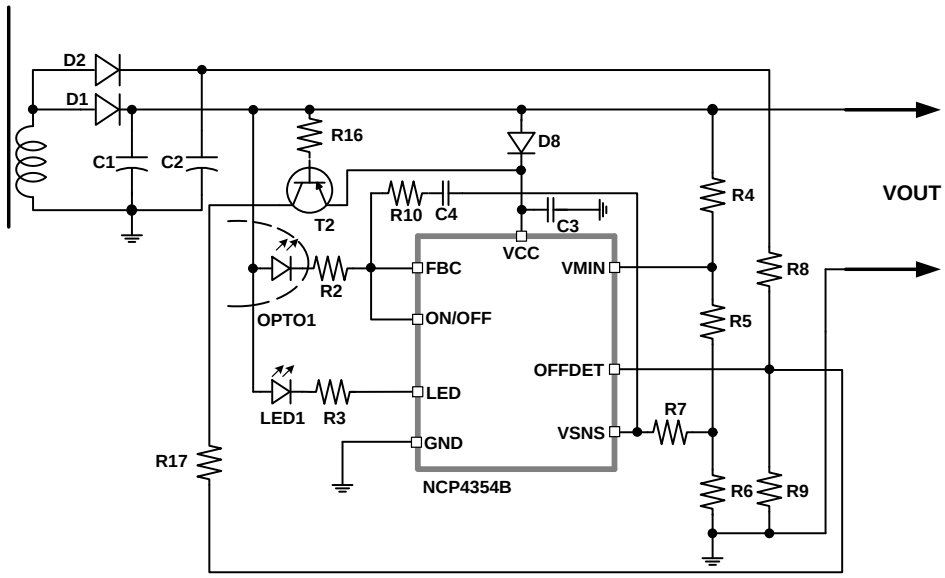


Figure 32. Improved Load Detection Connection

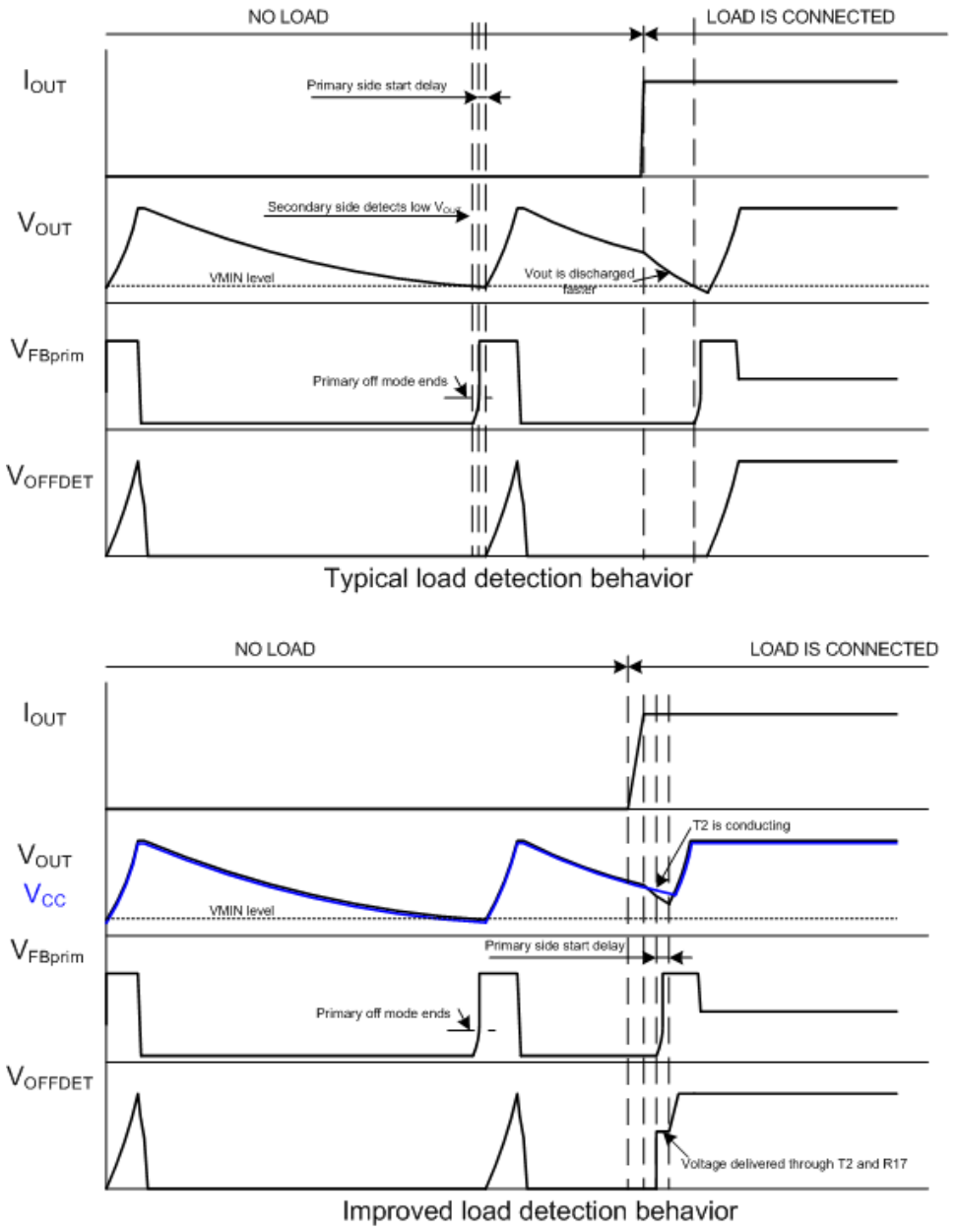


Figure 33. Typical and Improved Load Detection Comparison Waveforms

ORDERING INFORMATION

Device	Marking	Adjustable V_{min}	Current Regulation	LED Driver	Package	Shipping†
NCP4353ASNT1G	A53	No	Yes	No	TSOP−6 (Pb−Free)	3000 / Tape & Reel
NCP4353BSNT1G	B53	Yes	No	No	TSOP−6 (Pb−Free)	3000 / Tape & Reel
NCP4354ADR2G	NCP4354A	Yes	Yes	Yes	SOIC−8 (Pb−Free)	2500 / Tape & Reel
NCP4354BDR2G	NCP4354B	Yes	No	Yes	SOIC−8 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

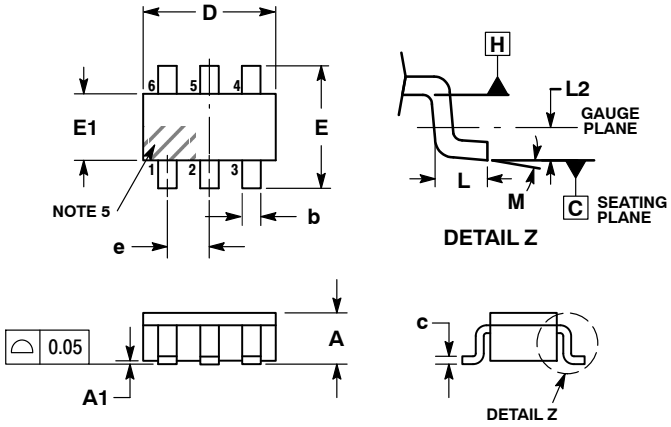
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

1

SCALE 2:1

TSOP−6
CASE 318G−02
ISSUE V

DATE 12 JUN 2012



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. PIN ONE INDICATOR MUST BE LOCATED IN THE INDICATED ZONE.

	MILLIMETERS		
DIM	**MIN**	**NOM**	**MAX**
A	0.90	1.00	1.10
A1	0.01	0.06	0.10
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.90	3.00	3.10
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e	0.85	0.95	1.05
L	0.20	0.40	0.60
L2	0.25 BSC		
M	0°	–	10°

STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 2:
PIN 1. EMITTER 2
2. BASE 1
3. COLLECTOR 1
4. EMITTER 1
5. BASE 2
6. COLLECTOR 2

STYLE 3:
PIN 1. ENABLE
2. N/C
3. R BOOST
4. Vz
5. V in
6. V out

STYLE 4:
PIN 1. N/C
2. V in
3. NOT USED
4. GROUND
5. ENABLE
6. LOAD

STYLE 5:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

STYLE 6:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 7:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. N/C
5. COLLECTOR
6. EMITTER

STYLE 8:
PIN 1. Vbus
2. D(in)
3. D(in)+
4. D(out)+
5. D(out)
6. GND

STYLE 9:
PIN 1. LOW VOLTAGE GATE
2. DRAIN
3. SOURCE
4. DRAIN
5. DRAIN
6. HIGH VOLTAGE GATE

STYLE 10:
PIN 1. D(OUT)+
2. GND
3. D(OUT)−
4. D(IN)−
5. VBUS
6. D(IN)+

STYLE 11:
PIN 1. SOURCE 1
2. DRAIN 2
3. DRAIN 2
4. SOURCE 2
5. GATE 1
6. DRAIN 1/GATE 2

STYLE 12:
PIN 1. I/O
2. GROUND
3. I/O
4. I/O
5. VCC
6. I/O

STYLE 13:
PIN 1. GATE 1
2. SOURCE 2
3. GATE 2
4. DRAIN 2
5. SOURCE 1
6. DRAIN 1

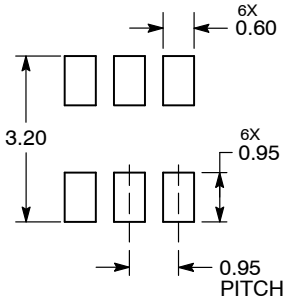
STYLE 14:
PIN 1. ANODE
2. SOURCE
3. GATE
4. CATHODE/DRAIN
5. CATHODE/DRAIN
6. CATHODE/DRAIN

STYLE 15:
PIN 1. ANODE
2. SOURCE
3. GATE
4. DRAIN
5. N/C
6. CATHODE

STYLE 16:
PIN 1. ANODE/CATHODE
2. BASE
3. EMITTER
4. COLLECTOR
5. ANODE
6. CATHODE

STYLE 17:
PIN 1. EMITTER
2. BASE
3. ANODE/CATHODE
4. ANODE
5. CATHODE
6. COLLECTOR

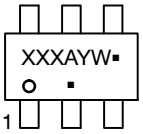
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

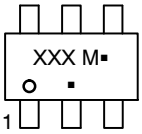
*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



IC

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package



STANDARD

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

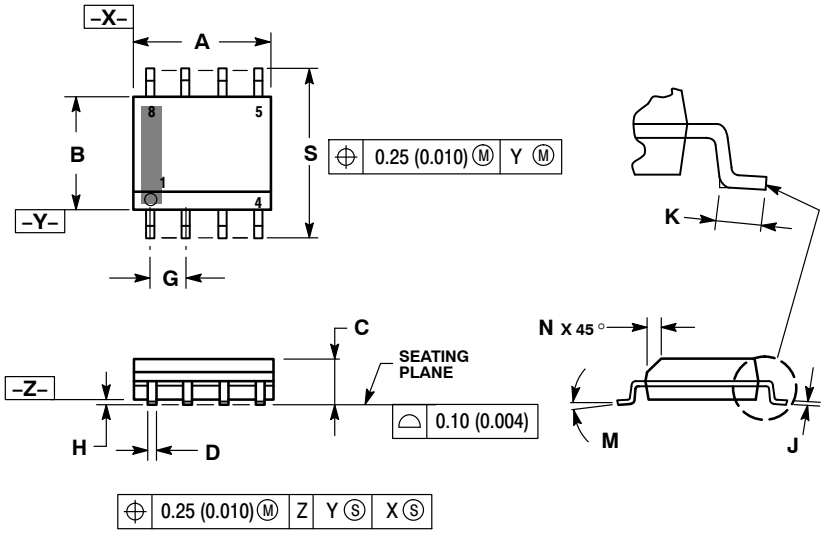
DOCUMENT NUMBER:	**98ASB14888C**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**TSOP−6**	**PAGE 1 OF 1**

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

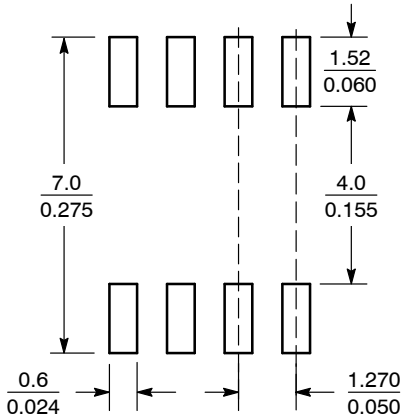
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

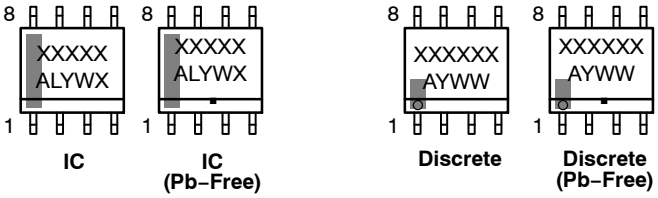
SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



IC | IC (Pb−Free) | Discrete | Discrete (Pb−Free)

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42564B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**SOIC−8 NB**	**PAGE 1 OF 2**

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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