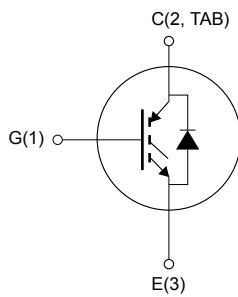


Trench gate field-stop, 650 V, 75 A, high-speed HB2 series IGBT in a TO-247 long leads package



TO-247 long leads



NG1E3C2T



Features

- Maximum junction temperature: $T_J = 175\text{ }^\circ\text{C}$
- Low $V_{CE(sat)} = 1.55\text{ V (typ.) @ } I_C = 75\text{ A}$
- Very fast and soft recovery co-packaged diode
- Minimized tail current
- Tight parameter distribution
- Low thermal resistance
- Positive $V_{CE(sat)}$ temperature coefficient

Applications

- Welding
- Power factor correction
- UPS
- Solar inverters
- Chargers

Description

The newest IGBT 650 V HB2 series represents an evolution of the advanced proprietary trench gate field-stop structure. The performance of the HB2 series is optimized in terms of conduction, thanks to a better $V_{CE(sat)}$ behavior at low current values, as well as in terms of reduced switching energy. A very fast soft recovery diode is co-packaged in antiparallel with the IGBT. The result is a product specifically designed to maximize efficiency for a wide range of fast applications.

Product status link

[STGWA75H65DFB2](#)

Product summary

Order code	STGWA75H65DFB2
Marking	G75H65DFB2
Package	TO-247 long leads
Packing	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CES}	Collector-emitter voltage ($V_{GE} = 0\text{ V}$)	650	V
I_C	Continuous collector current at $T_C = 25\text{ °C}$	115	A
	Continuous collector current at $T_C = 100\text{ °C}$	71	
$I_{CP}^{(1)}$	Pulsed collector current ($t_p \leq 1\text{ }\mu\text{s}$, $T_J < 175\text{ °C}$)	225	
V_{GE}	Gate-emitter voltage	± 20	V
	Transient gate-emitter voltage ($t_p \leq 10\text{ }\mu\text{s}$)	± 30	
I_F	Continuous forward current at $T_C = 25\text{ °C}$	110	A
	Continuous forward current at $T_C = 100\text{ °C}$	65	
$I_{FP}^{(1)}$	Pulsed forward current ($t_p \leq 1\text{ }\mu\text{s}$, $T_J < 175\text{ °C}$)	195	
P_{TOT}	Total power dissipation at $T_C = 25\text{ °C}$	357	W
T_{STG}	Storage temperature range	-55 to 150	°C
T_J	Operating junction temperature range	-55 to 175	

1. Defined by design, not subject to production test.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance junction-case IGBT	0.42	°C/W
	Thermal resistance junction-case diode	0.49	
R_{thJA}	Thermal resistance junction-ambient	50	

2 Electrical characteristics

$T_C = 25\text{ °C}$ unless otherwise specified

Table 3. Static characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)CES}$	Collector-emitter breakdown voltage	$V_{GE} = 0\text{ V}, I_C = 1\text{ mA}$	650			V
$V_{CE(sat)}$	Collector-emitter saturation voltage	$V_{GE} = 15\text{ V}, I_C = 75\text{ A}$		1.55	2	V
		$V_{GE} = 15\text{ V}, I_C = 75\text{ A}, T_J = 125\text{ °C}$		1.8		
		$V_{GE} = 15\text{ V}, I_C = 75\text{ A}, T_J = 175\text{ °C}$		1.9		
V_F	Forward on-voltage	$I_F = 75\text{ A}$		1.8	2.3	V
		$I_F = 75\text{ A}, T_J = 125\text{ °C}$		1.45		
		$I_F = 75\text{ A}, T_J = 175\text{ °C}$		1.35		
$V_{GE(th)}$	Gate threshold voltage	$V_{CE} = V_{GE}, I_C = 1\text{ mA}$	5	6	7	V
I_{CES}	Collector cut-off current	$V_{GE} = 0\text{ V}, V_{CE} = 650\text{ V}$			25	μA
I_{GES}	Gate-emitter leakage current	$V_{CE} = 0\text{ V}, V_{GE} = \pm 20\text{ V}$			± 250	nA

Table 4. Dynamic characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{ies}	Input capacitance	$V_{CE} = 25\text{ V}, f = 1\text{ MHz}, V_{GE} = 0\text{ V}$	-	4357	-	pF
C_{oes}	Output capacitance		-	264	-	
C_{res}	Reverse transfer capacitance		-	117	-	
Q_g	Total gate charge	$V_{CC} = 520\text{ V}, I_C = 75\text{ A},$	-	207	-	nC
Q_{ge}	Gate-emitter charge	$V_{GE} = 0\text{ to }15\text{ V}$	-	40	-	
Q_{gc}	Gate-collector charge	(see Figure 28. Gate charge test circuit)	-	85	-	

Table 5. Switching characteristics (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{CC} = 400\text{ V}$, $I_C = 75\text{ A}$, $V_{GE} = 15\text{ V}$, $R_G = 2.2\ \Omega$ (see Figure 27. Test circuit for inductive load switching)	-	28	-	ns
t_r	Current rise time		-	16	-	ns
$E_{on}^{(1)}$	Turn-on switching energy		-	1428	-	μJ
$t_{d(off)}$	Turn-off delay time		-	100	-	ns
t_f	Current fall time		-	36	-	ns
$E_{off}^{(2)}$	Turn-off switching energy		-	1050	-	μJ
$t_{d(on)}$	Turn-on delay time	$V_{CC} = 400\text{ V}$, $I_C = 75\text{ A}$, $V_{GE} = 15\text{ V}$, $R_G = 2.2\ \Omega$, $T_J = 175\text{ }^\circ\text{C}$ (see Figure 27. Test circuit for inductive load switching)	-	27	-	ns
t_r	Current rise time		-	17	-	ns
$E_{on}^{(1)}$	Turn-on switching energy		-	3090	-	μJ
$t_{d(off)}$	Turn-off delay time		-	123	-	ns
t_f	Current fall time		-	87	-	ns
$E_{off}^{(2)}$	Turn-off switching energy		-	1770	-	μJ

1. Including the reverse recovery of the diode.
2. Including the tail of the collector current.

Table 6. Diode switching characteristics (inductive load)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{rr}	Reverse recovery time	$I_F = 75\text{ A}$, $V_R = 400\text{ V}$, $V_{GE} = 15\text{ V}$, $di/dt = 1000\text{ A}/\mu\text{s}$ (see Figure 30. Diode reverse recovery waveform)	-	88	-	ns
Q_{rr}	Reverse recovery charge		-	923	-	nC
I_{rrm}	Reverse recovery current		-	26	-	A
di_{rr}/dt	Peak rate of fall of reverse recovery current during t_b		-	1166	-	$\text{A}/\mu\text{s}$
E_{rr}	Reverse recovery energy		-	144	-	μJ
t_{rr}	Reverse recovery time	$I_F = 75\text{ A}$, $V_R = 400\text{ V}$, $V_{GE} = 15\text{ V}$, $di/dt = 1000\text{ A}/\mu\text{s}$, $T_J = 175\text{ }^\circ\text{C}$ (see Figure 30. Diode reverse recovery waveform)	-	162	-	ns
Q_{rr}	Reverse recovery charge		-	5431	-	nC
I_{rrm}	Reverse recovery current		-	60	-	A
di_{rr}/dt	Peak rate of fall of reverse recovery current during t_b		-	800	-	$\text{A}/\mu\text{s}$
E_{rr}	Reverse recovery energy		-	1064	-	μJ

2.1 Electrical characteristics (curves)

Figure 1. Power dissipation vs case temperature

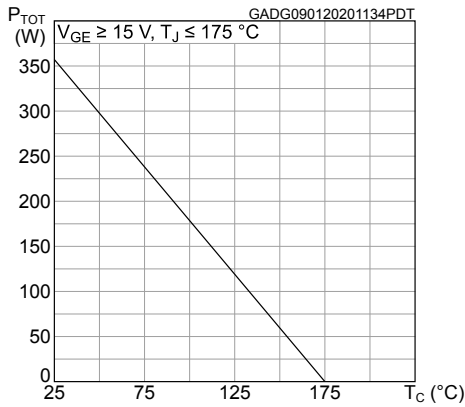


Figure 2. Collector current vs case temperature

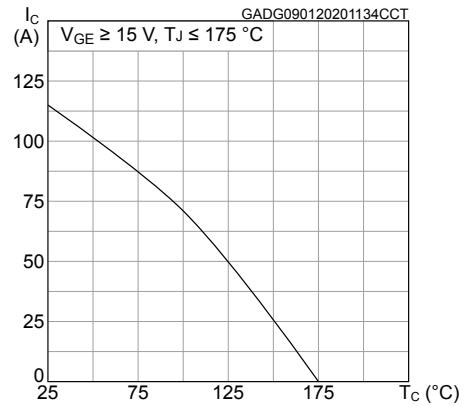


Figure 3. Output characteristics (T_J = 25 °C)

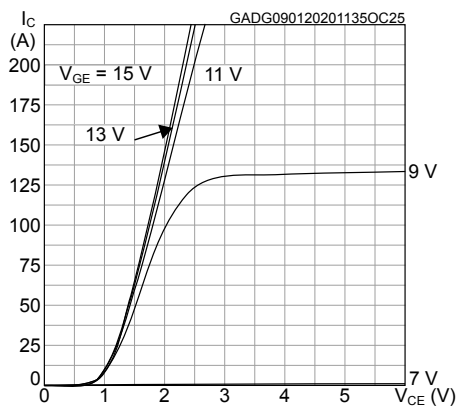


Figure 4. Output characteristics (T_J = 175 °C)

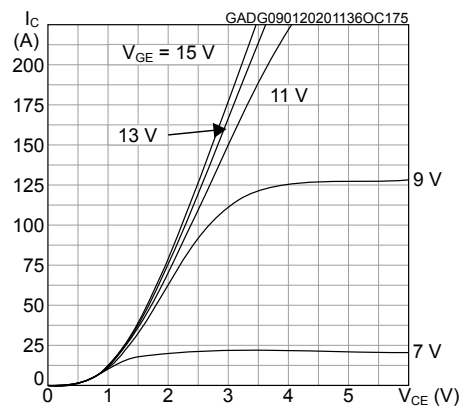


Figure 5. V_{CE(sat)} vs junction temperature

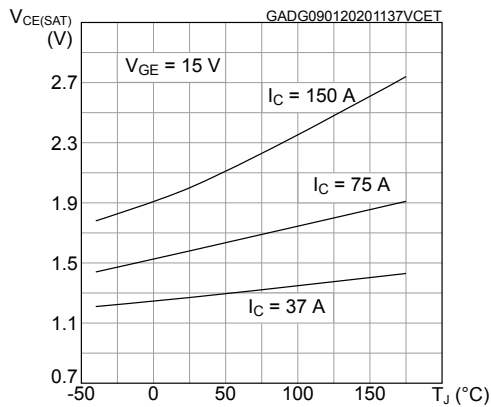


Figure 6. V_{CE(sat)} vs collector current

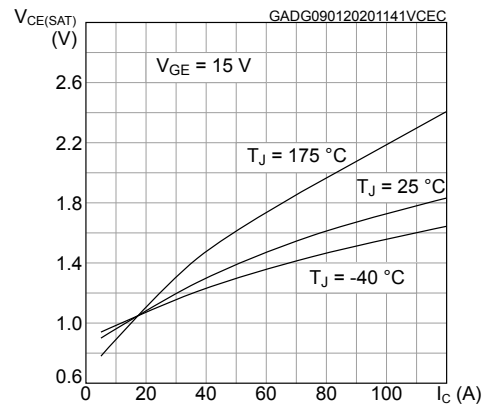


Figure 7. Collector current vs switching frequency

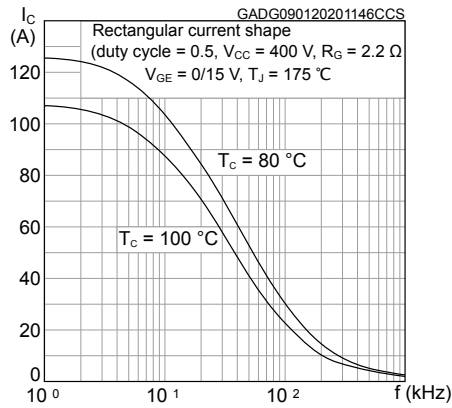


Figure 8. Forward bias safe operating area

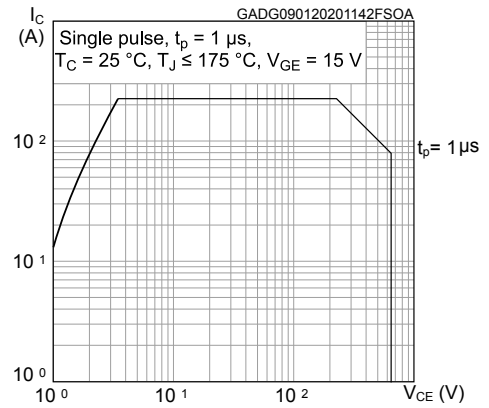


Figure 9. Transfer characteristics

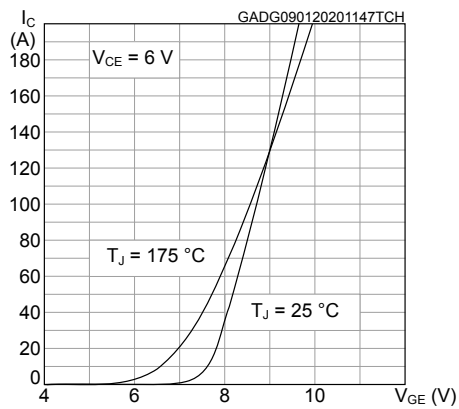


Figure 10. Diode V_f vs forward current

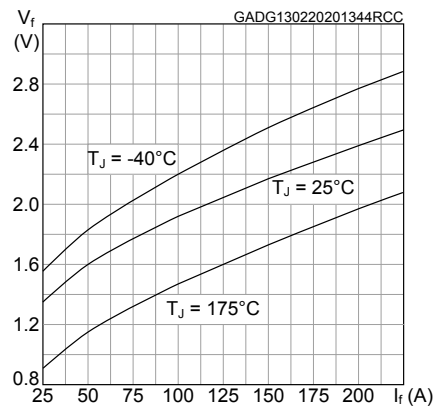


Figure 11. Normalized $V_{GE(th)}$ vs junction temperature

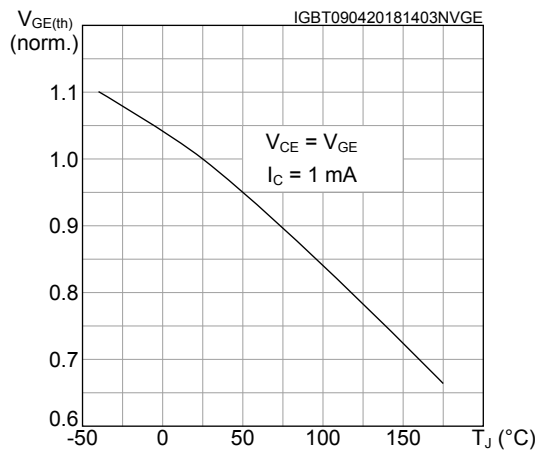


Figure 12. Normalized $V_{(BR)CES}$ vs junction temperature

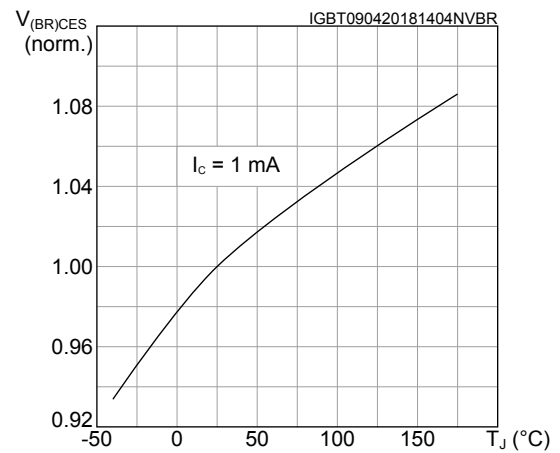


Figure 13. Capacitance variations

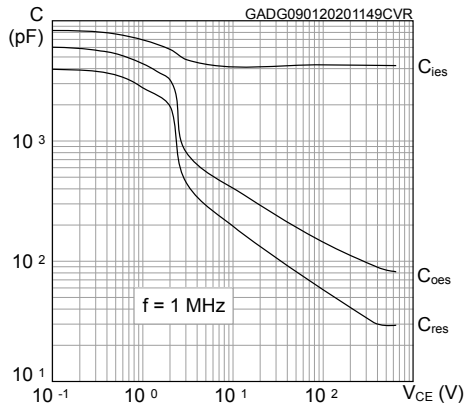


Figure 14. Gate charge vs gate-emitter voltage

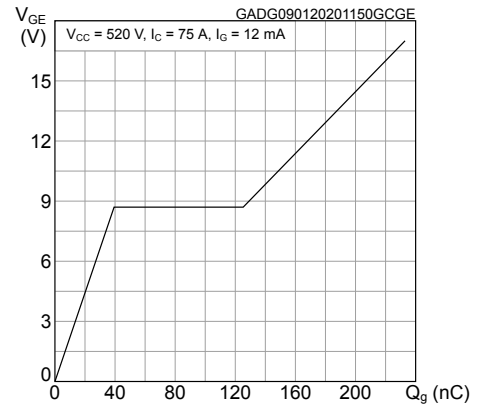


Figure 15. Switching energy vs collector current

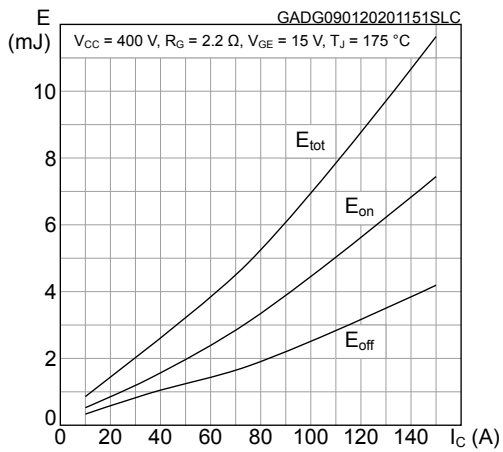


Figure 16. Switching energy vs temperature

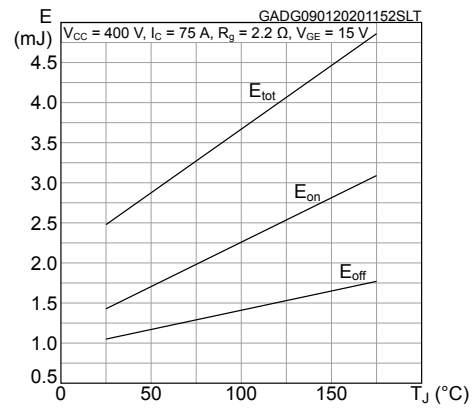


Figure 17. Switching energy vs collector emitter voltage

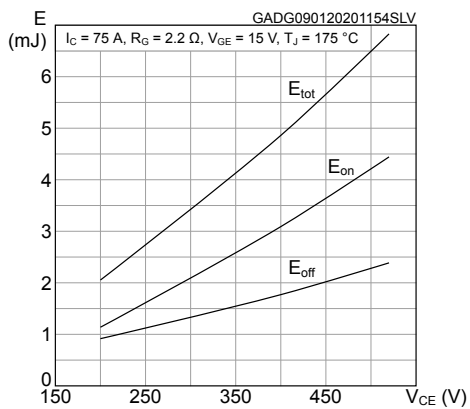


Figure 18. Switching energy vs gate resistance

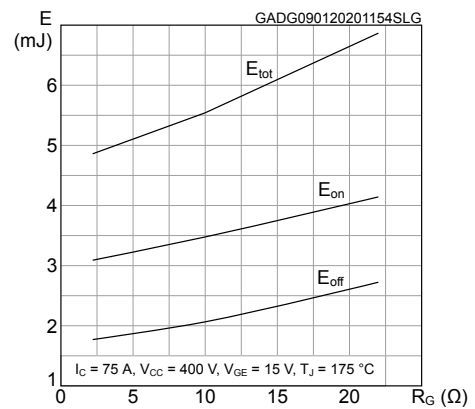


Figure 19. Switching times vs collector current

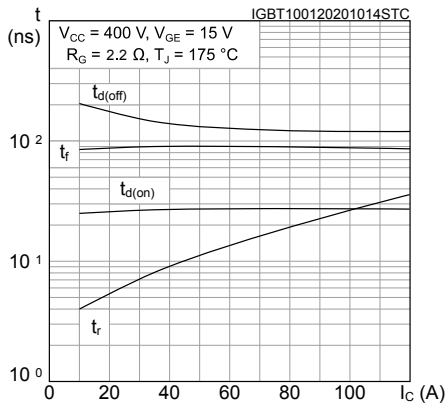


Figure 20. Switching times vs gate resistance

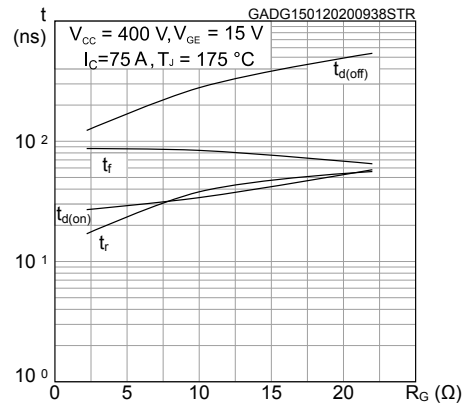


Figure 21. Reverse recovery current vs diode current slope

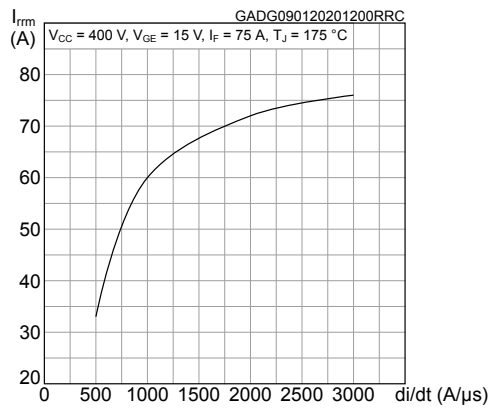


Figure 22. Reverse recovery time vs diode current slope

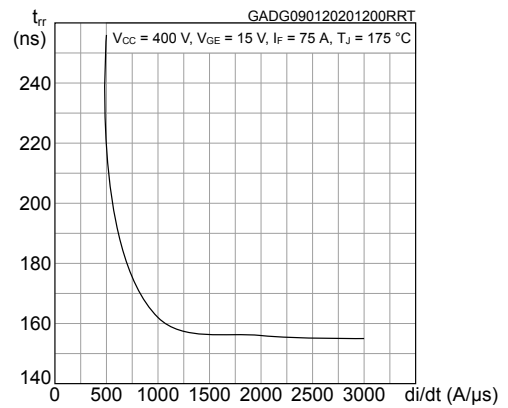


Figure 23. Reverse recovery charge vs diode current slope

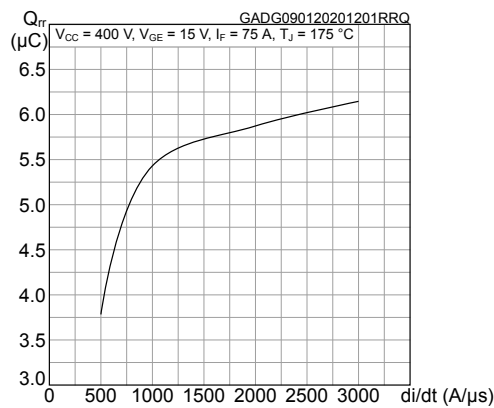


Figure 24. Reverse recovery energy vs diode current slope

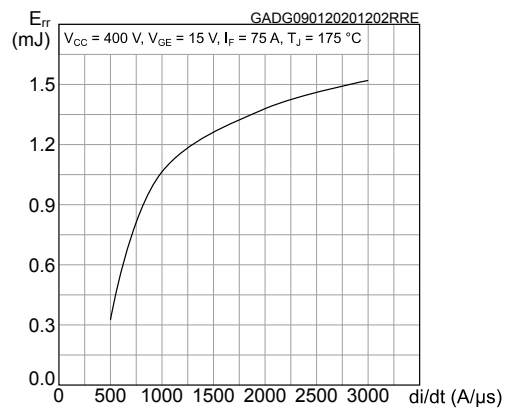


Figure 25. Thermal impedance for IGBT

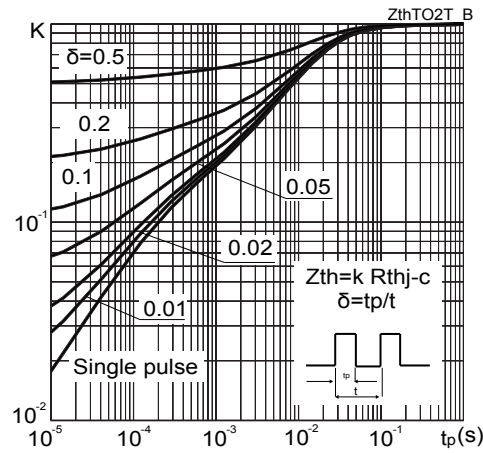
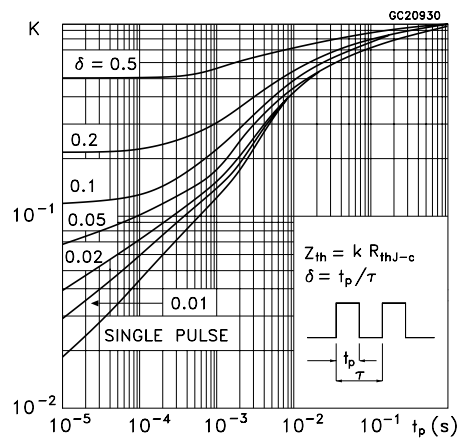
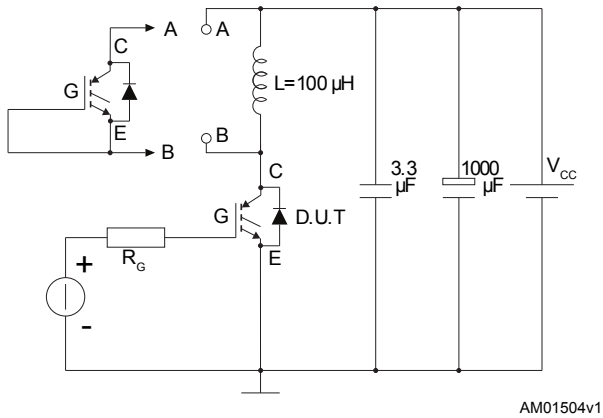
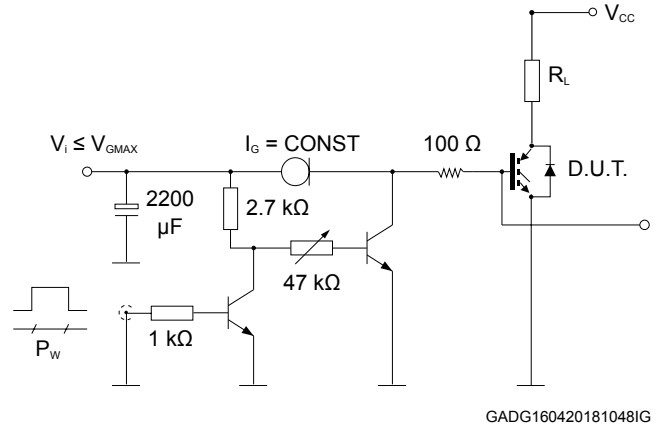
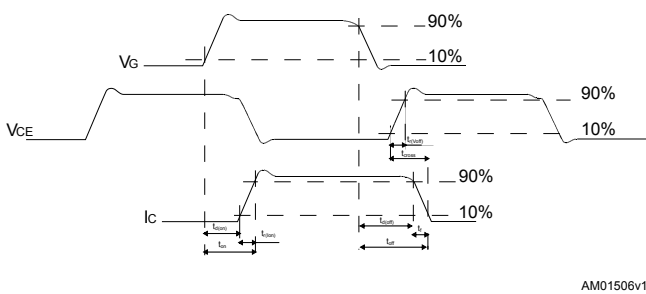
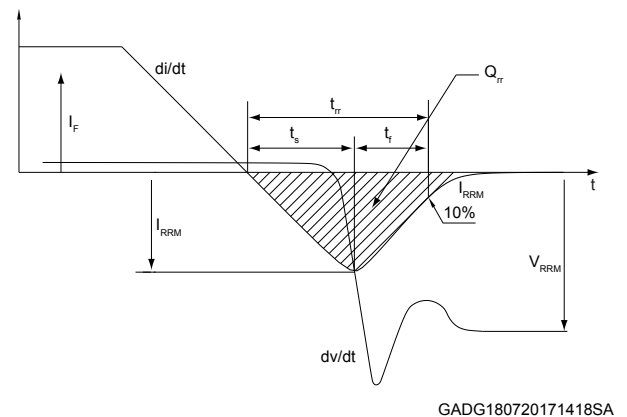


Figure 26. Thermal impedance for diode



3 Test circuits

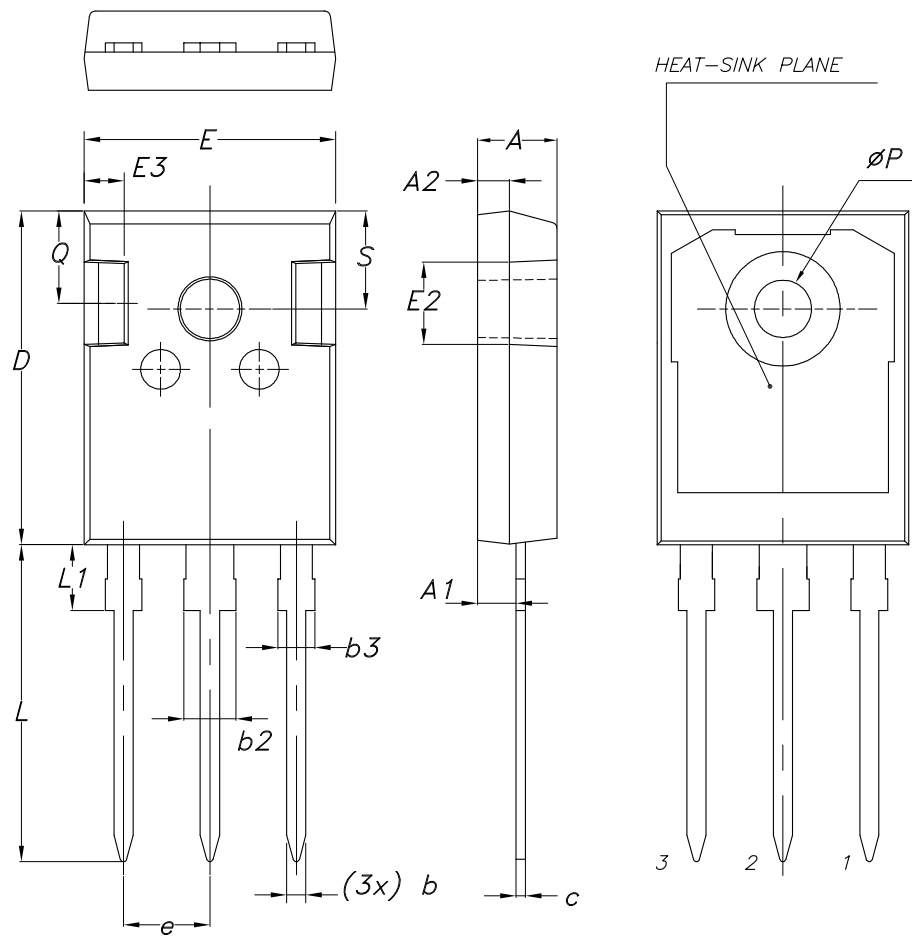
Figure 27. Test circuit for inductive load switching

Figure 28. Gate charge test circuit

Figure 29. Switching waveform

Figure 30. Diode reverse recovery waveform


4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO-247 long leads package information

Figure 31. TO-247 long leads package outline



8463846_2_F

Table 7. TO-247 long leads package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.90	5.00	5.10
A1	2.31	2.41	2.51
A2	1.90	2.00	2.10
b	1.16		1.26
b2			3.25
b3			2.25
c	0.59		0.66
D	20.90	21.00	21.10
E	15.70	15.80	15.90
E2	4.90	5.00	5.10
E3	2.40	2.50	2.60
e	5.34	5.44	5.54
L	19.80	19.92	20.10
L1			4.30
P	3.50	3.60	3.70
Q	5.60		6.00
S	6.05	6.15	6.25

Revision history

Table 8. Document revision history

Date	Version	Changes
09-Jan-2020	1	First release.
13-Feb-2020	2	Updated Table 3. Static characteristics and Figure 10. Diode V_F vs forward current . Minor text changes.

Contents

1	Electrical ratings	2
2	Electrical characteristics	3
2.1	Electrical characteristics (curves)	5
3	Test circuits	10
4	Package information	11
4.1	TO-247 long leads package information	11
	Revision history	13

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, please refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2020 STMicroelectronics – All rights reserved