PRODUCT/PROCESS CHANGE NOTIFICATION

PCN IPG-PWR/14/8304
Dated 27 Jan 2014

DPAK Matrix Large Die Pad Back-End Capacity Extension - Shenzhen (China) - Automotive

Table 1. Change Implementation Schedule

Forecasted implementation date for change	20-Jan-2014
Forecasted availability date of samples for customer	20-Jan-2014
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	20-Jan-2014
Estimated date of changed product first shipment	21-Jul-2014

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	see attached list
Type of change	Package assembly process change
Reason for change	Improve service to Customers
Description of the change	Continuing in the aim of a constant process improvement, please be informed that we're going to use Automatic Assembly/Testing DPAK Matrix & Large Die Pad line for Power MOSFET Transistors produced in Shenzhen (China). You already received products in DPAK Matrix or/and Large Die Pad Frame with separated processes, since long time, today we mix them together in order to maximize the productivity. DPAK device products, manufactured in Shenzhen (China), guarantee the same quality and electrical characteristics as reported in the relevant data sheets. Devices used for qualification are available as samples.
Change Product Identification	by data code
Manufacturing Location(s)	

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	

Customer Acknowledgement of Receipt	**PCN IPG-PWR/14/8304**
Please sign and return to STMicroelectronics Sales Office	**Dated 27 Jan 2014**
☐ Qualification Plan Denied	Name:
☐ Qualification Plan Approved	Title:
	Company:
☐ Change Denied	Date:
☐ Change Approved	Signature:

Remark

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DOCUMENT APPROVAL

Name	Function
Mottese, Anna	Marketing Manager
Aleo, Mario-Antonio	Product Manager
Falcone, Giuseppe	Q.A. Manager

Dear Customer,

Continuing in the aim of a constant process improvement, please be informed that we're going to use Automatic Assembly/Testing DPAK Matrix & Large Die Pad line for Power MOSFET Transistors produced in Shenzhen (China). You already received products in DPAK Matrix or/and Large Die Pad Frame with separated processes, since long time, today we mix them together in order to maximize the productivity. DPAK device products, manufactured in Shenzhen (China), guarantee the same quality and electrical characteristics as reported in the relevant data sheets. Devices used for qualification are available as samples.

The involved product series and affected packages are listed in the table below:

Product Family Description	Package	Commercial Product / Series
Power MOSFET Transistors	**DPAK**	**STDxxx**

Any other Product related to the above series, manufactured in DPAK package with Automatic Assembly/Testing DPAK Matrix & Large Die Pad line, even if not expressly included or partially mentioned in the attached table, is affected by this change.

Qualification program and results availability:

The reliability test report is provided in attachment to this document.

Samples availability:

Samples of the test vehicle devices will be available on request starting from week 04-2014.
Any other sample request will be processed and scheduled by Power Transistor Division upon request.

Product Family Description	Package	Part Number - Test Vehicle
Power MOSFET Transistors	**DPAK**	**STD45NF75T4** **STD96N3LLH6** **STD155N3H6**

Change implementation schedule:

The production start and first shipments will be implemented according to our work in progress and materials availability:

Product Family	1st Shipments
Power MOSFET Transistors	From Week 30-2014

Marking and traceability:

Unless otherwise stated by customer specific requirement, traceability of Power MOSFET Transistors form the Automatic Assembly/Testing DPAK Matrix & Large Die Pad line produced in Shenzhen (China), will be ensured by week code.

Sincerely Yours.

Reliability Report

DPAK Matrix Large Die Pad Back-End Capacity Extension - Shenzhen (China) - Automotive

General Information	
Product Lines:	ED7G / 6L34 / 6D3F
Product Families:	Power MOSFET
P/Ns:	STD45NF75T4 STD96N3LLH6 STD155N3H6
Product Group:	IPG
Product division:	Power Transistor Division
Package:	DPAK
Silicon Process techn.:	STripFET™ II Power MOSFET STripFET™ VI DeepGATE™ Power MOSFET

Locations	
Wafer Diffusion Plants:	*CATANIA (Italy)*
EWS Plants:	*CATANIA (Italy)*
Assembly plant:	*ST SHENZHEN (China)*
Reliability Lab:	*IPG-PTD Catania Reliability Lab.*

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	January 2014	8	C. Cappello	G. Falcone	First issue

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.
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TABLE OF CONTENTS

1 APPLICABLE AND REFERENCE DOCUMENTS 3
2 GLOSSARY 3
3 RELIABILITY EVALUATION OVERVIEW 3
3.1 OBJECTIVES 3
3.2 CONCLUSION 3
4 DEVICE CHARACTERISTICS 4
4.1 DEVICE DESCRIPTION 4
4.2 CONSTRUCTION NOTE 4
5 TESTS RESULTS SUMMARY 7
5.1 TEST VEHICLE 7
5.2 RELIABILITY TEST PLAN SUMMARY 7
6 ANNEXES 6.0 8
6.1 TESTS DESCRIPTION 8

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
AEC-Q101	Stress test qualification for automotive grade discrete semiconductors

2 GLOSSARY

DUT	Device Under Test
SS	Sample Size

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

Qualification of the Automatic Assembly/Testing DPAK Matrix & Large Die Pad line for Power MOSFET Transistors produced in Shenzhen (China).

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. It is stressed that reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description

N-channel Power MOSFET

4.2 Construction note

D.U.T.: STD45NF75T4 LINE: ED7G PACKAGE: DPAK

Wafer/Die fab. information	
Wafer fab manufacturing location	Catania (Italy)
Technology	STripFET™ II Power MOSFET
Die finishing back side	Ti/Ni/Au
Die size	3960 x 2910 μm^2
Metal	Al/Si
Passivation type	NITRIDE

Wafer Testing (EWS) information	
Electrical testing manufacturing location	Catania (Italy)
Test program	WPIS

Assembly information	
Assembly site	ST Shenzhen (China)
Package description	DPAK
Molding compound	Epoxy Resin
Frame material	Copper
Die attach process	Soft Solder
Die attach material	Pb/Sn/Ag
Wire bonding process	Ultrasonic
Wires bonding materials	Gate: Wire Al/Mg 5 mils Source: Wire Al 15 mils
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	ST Shenzhen (China)
Tester	IP TEST

D.U.T.: STD96N3LLH6 LINE: 6L34 PACKAGE: DPAK

Wafer/Die fab. information	
Wafer fab manufacturing location	Catania (Italy)
Technology	STripFET™ VI DeepGATE™ Power MOSFET
Die finishing back side	Ti/NiV/Au
Die size	2500 x 2200 μm^2
Metal	AlCu
Passivation type	TEOS/NITRIDE

Wafer Testing (EWS) information	
Electrical testing manufacturing location	Catania (Italy)
Test program	WPIS

Assembly information	
Assembly site	ST Shenzhen (China)
Package description	DPAK
Molding compound	Epoxy Resin
Frame material	Copper
Die attach process	Soft Solder
Die attach material	Pb/Sn/Ag
Wire bonding process	Ultrasonic
Wires bonding materials	Gate: Wire Al/Mg 5 mils Source: Wire Al 15 mils
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	ST Shenzhen (China)
Tester	IP TEST

D.U.T.: STD155N3H6 LINE: 6D3F PACKAGE: DPAK

Wafer/Die fab. information	
Wafer fab manufacturing location	Catania (Italy)
Technology	STripFET™ VI DeepGATE™ Power MOSFET
Die finishing back side	Ti/NiV/Au
Die size	2640 x 3860 μm^2
Metal	AlCu
Passivation type	TEOS/NITRIDE

Wafer Testing (EWS) information	
Electrical testing manufacturing location	Catania (Italy)
Test program	WPIS

Assembly information	
Assembly site	ST Shenzhen (China)
Package description	DPAK
Molding compound	Epoxy Resin
Frame material	Copper
Die attach process	Soft Solder
Die attach material	Pb/Sn/Ag
Wire bonding process	Ultrasonic
Wires bonding materials	Gate: Wire Al/Mg 5 mils Source: Wire Al 15 mils
Lead finishing/bump solder material	Pure Tin

Final testing information	
Testing location	ST Shenzhen (China)
Tester	IP TEST

5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Lot #	Process/ Package	Product Line	Comments
1	STD45NF75T4	ED7G	Power MOSFET
2	STD96N3LLH6	6L34	Power MOSFET
3	STD155N3H6	6D3F	Power MOSFET

5.2 Reliability test plan summary

Lot. 1 - D.U.T.: STD45NF75T4 LINE: ED7G PACKAGE: DPAK
Lot. 2 - D.U.T.: STD96N3LLH6 LINE: 6L34 PACKAGE: DPAK
Lot. 3 - D.U.T.: STD155N3H6 LINE: 6D3F PACKAGE: DPAK

#	Stress (Abrv)	PC	Std ref.	Conditions	Sample Size (S.S.)	Steps	Failure/SS		
							Lot 1	Lot 2	Lot 3
1	TEST		User specification	All qualification parts tested per the requirements of the appropriate device specification.			0/308	0/308	0/308
2	External visual		JESD22 B-101	All devices submitted for testing			0/308	0/308	0/308
3	PC		JESD22 A-113	Dryng 24H @ 125°C Store 168H @ TA=85°C RH=85% IR Reflow @ 260°C 3 times	All devices to be subjected to H3TRB, TC, AC, IOL		0/308	0/308	0/308
4	TC	Y	JESD22 A-104	TA=-55°C TO 150°C 1 HOURS / CYCLE TIME=1000CYCLES	231	100cy	0/77	0/77	0/77
						200cy	0/77	0/77	0/77
						500cy	0/77	0/77	0/77
						1000cy	0/77	0/77	0/77
5	AC	Y	JESD22 A-102	TA=121°C ; PA=2ATM TIME=96H	231	96H	0/77	0/77	0/77
6	H3TRB	Y	JESD22 A-101	TA=85°C ; RH=85% BIAS=50V (ED7G) BIAS=30V (6L34) BIAS=30V (6D3F) TIME=1000 HOURS	231	168H	0/77	0/77	0/77
						500H	0/77	0/77	0/77
						1000H	0/77	0/77	0/77
7	IOL / TF	Y	MIL-STD-750 Method 1037	ΔTC=105°C Ton / Toff = 2min	231	15Kcy	0/77	0/77	0/77
8	Thermal Resistance		JESD24-3, 24-4, 24-6 as appropriate		10 pre & post change		0/10		
9	Physical Dimension		JESD22 B-100		30		0/30		
10	Die Shear		MIL-STD-750 Method 2017		5		0/5		

6 ANNEXES 6.0

6.1Tests Description

Test name	Description	Purpose
Package Oriented Tests		
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
TF / IOL Thermal Fatigue / Intermittent Operating Life	The device is submitted to cycled temperature excursions generated by power cycles (ON/OFF) at T ambient.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
H3TRB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	To verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.

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