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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

May 2015

FQD2P40

P-Channel QFET® MOSFET

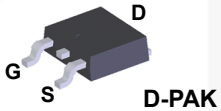
-400 V, -1.56 A, 6.5 Ω

Description

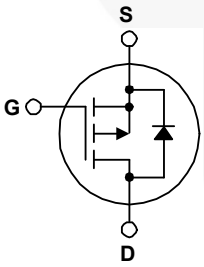
This P-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, audio amplifier, DC motor control, and variable switching power applications..

Features

- -1.56 A, -400 V, $R_{DS(on)}$ = 6.5 Ω (Max.) @ V_{GS} = -10 V, I_D = -0.78 A
- Low Gate Charge (Typ. 10 nC)
- Low Crss (Typ. 6.5 pF)
- 100% Avalanche Tested
- RoHS Compliant



D-PAK



Absolute Maximum Ratings

T_C = 25°C unless otherwise noted.

Symbol	Parameter		FQD2P40TM	Unit
V_{DSS}	Drain-Source Voltage		-400	V
I_D	Drain Current - Continuous (T_C = 25°C)		-1.56	A
	- Continuous (T_C = 100°C)		-0.98	A
I_{DM}	Drain Current - Pulsed	(Note 1)	-6.24	A
V_{GSS}	Gate-Source Voltage		± 30	V
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	120	mJ
I_{AR}	Avalanche Current	(Note 1)	-1.56	A
E_{AR}	Repetitive Avalanche Energy	(Note 1)	3.8	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	-4.5	V/ns
P_D	Power Dissipation (T_A = 25°C) *		2.5	W
	Power Dissipation (T_C = 25°C)		38	W
	- Derate above 25°C		0.3	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	°C
T_L	Maximum lead temperature for soldering, 1/8" from case for 5 seconds		300	°C

Thermal Characteristics

Symbol	Parameter	FQD2P40TM	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	3.29	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Minimum Pad of 2-oz Copper), Max.	110	
	Thermal Resistance, Junction to Ambient (*1 in^2 Pad of 2-oz Copper), Max.	50	

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQD2P40TM	FQD2P40	D-PAK	Tape and Reel	330 mm	16 mm	2500 units

Electrical Characteristics

T_C = 25°C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = -250 μA	-400	--	--	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = -250 μA, Referenced to 25°C	--	-	--	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -400 V, V_{GS} = 0 V	--	--	-1	μA
		V_{DS} = -320 V, T_C = 125°C	--	--	-10	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = -30 V, V_{DS} = 0 V	--	--	-100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = 30 V, V_{DS} = 0 V	--	--	100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -250 μA	-3.0	--	-5.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = -10 V, I_D = -0.78 A	--	5.0	6.5	Ω
g_{FS}	Forward Transconductance	V_{DS} = -50 V, I_D = -0.78 A	--	1.26	--	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = -25 V, V_{GS} = 0 V, f = 1.0 MHz	--	270	350	pF
C_{oss}	Output Capacitance		--	45	60	pF
C_{rss}	Reverse Transfer Capacitance		--	6.5	8.5	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = -200 V, I_D = -2.0 A, R_G = 25 Ω (Note 4)	--	9	30	ns
t_r	Turn-On Rise Time		--	33	75	ns
$t_{d(off)}$	Turn-Off Delay Time		--	22	55	ns
t_f	Turn-Off Fall Time		--	25	60	ns
Q_g	Total Gate Charge	V_{DS} = -320 V, I_D = -2.0 A, V_{GS} = -10 V (Note 4)	--	10	13	nC
Q_{gs}	Gate-Source Charge		--	2.1	--	nC
Q_{gd}	Gate-Drain Charge		--	5.5	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	-1.56	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	-6.24	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = -1.56 A	--	--	-5.0	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S = -2.0 A, dI_F / dt = 100 A/μs	--	250	--	ns
Q_{rr}	Reverse Recovery Charge		--	0.85	--	μC

Notes:
1. Repetitive rating : pulse-width limited by maximum junction temperature.
2. L = 86 mH, I_{AS} = -1.56 A, V_{DD} = -50 V, R_G = 25 Ω, starting T_J = 25°C.
3. I_{SD} ≤ -2.0 A, di/dt ≤ 200 A/μs, V_{DD} ≤ BV_{DSS}, starting T_J = 25°C.
4. Essentially independent of operating temperature.

Typical Characteristics

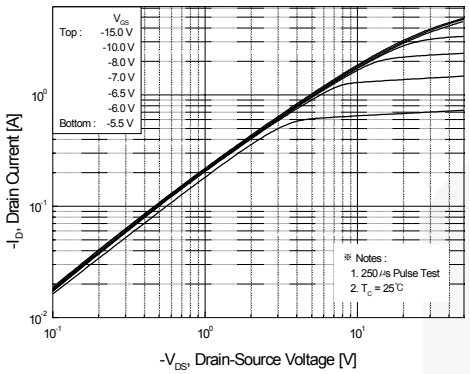


Figure 1. On-Region Characteristics

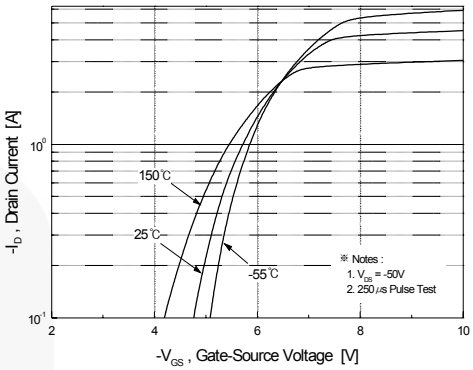


Figure 2. Transfer Characteristics

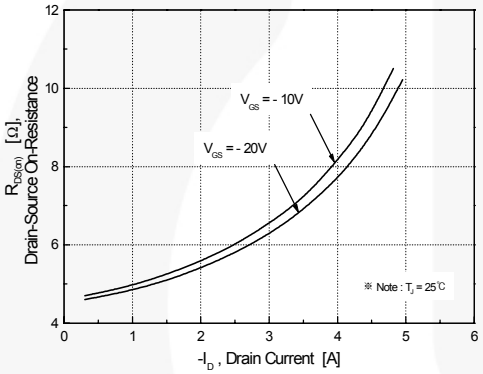


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

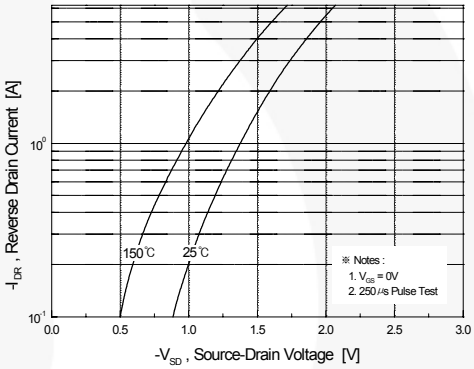


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

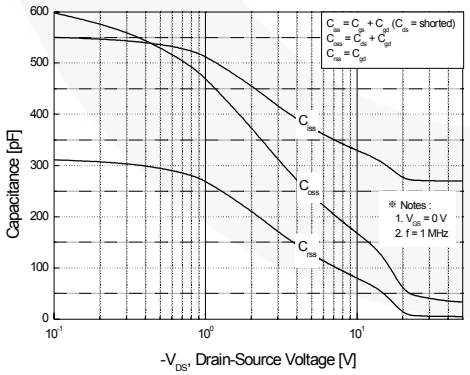


Figure 5. Capacitance Characteristics

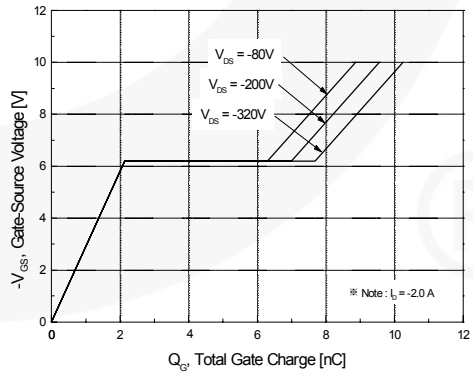


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

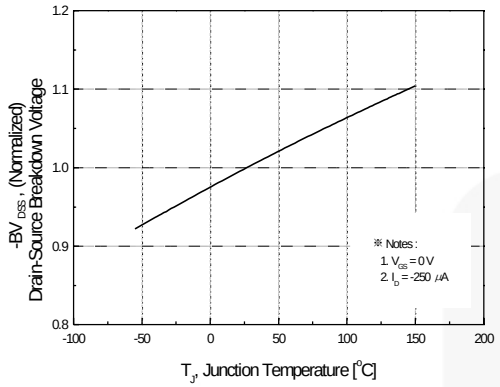


Figure 7. Breakdown Voltage Variation vs. Temperature

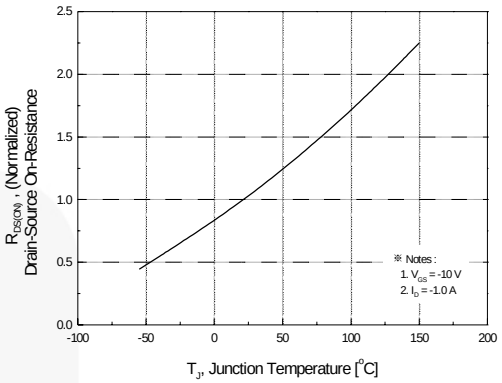


Figure 8. On-Resistance Variation vs. Temperature

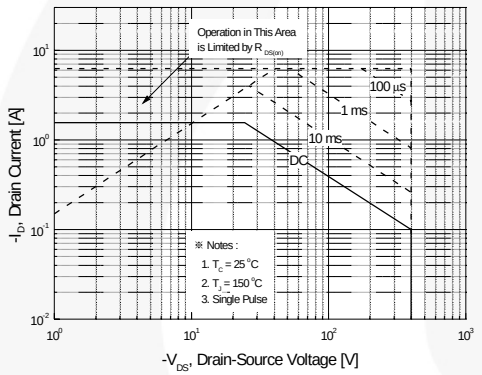


Figure 9. Maximum Safe Operating Area

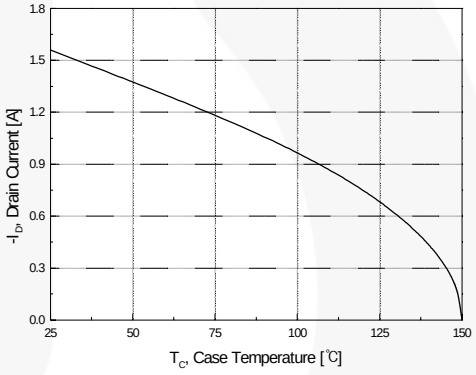


Figure 10. Maximum Drain Current vs. Case Temperature

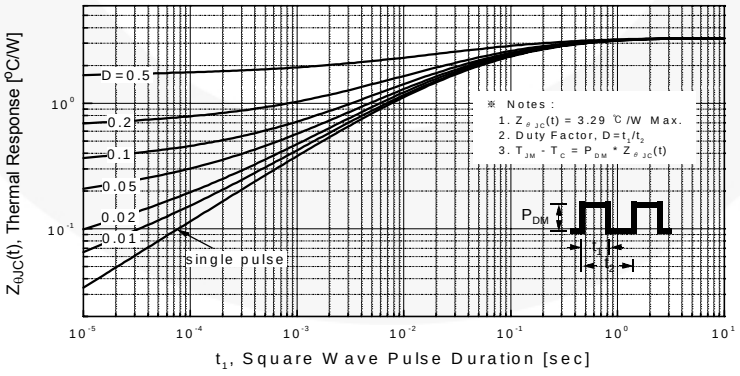


Figure 11. Transient Thermal Response Curve

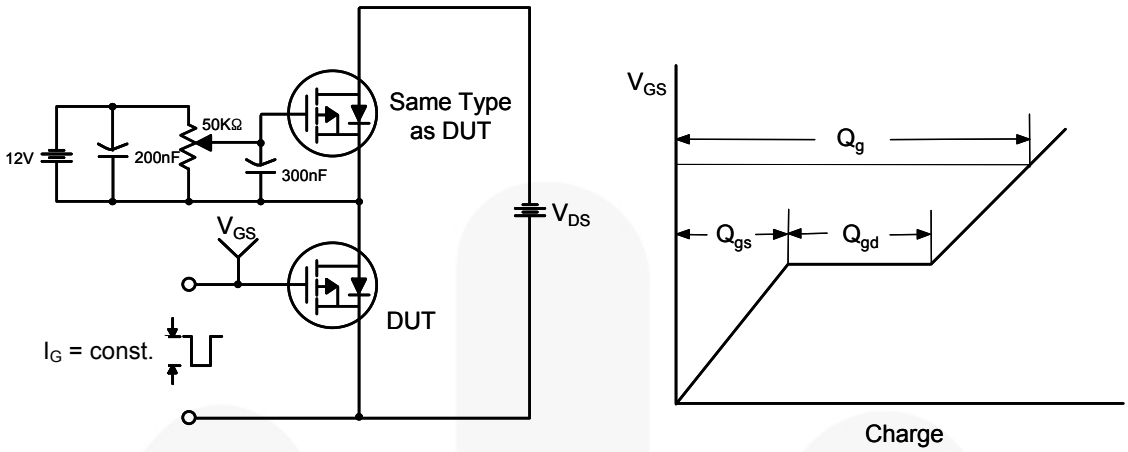


Figure 12. Gate Charge Test Circuit & Waveform

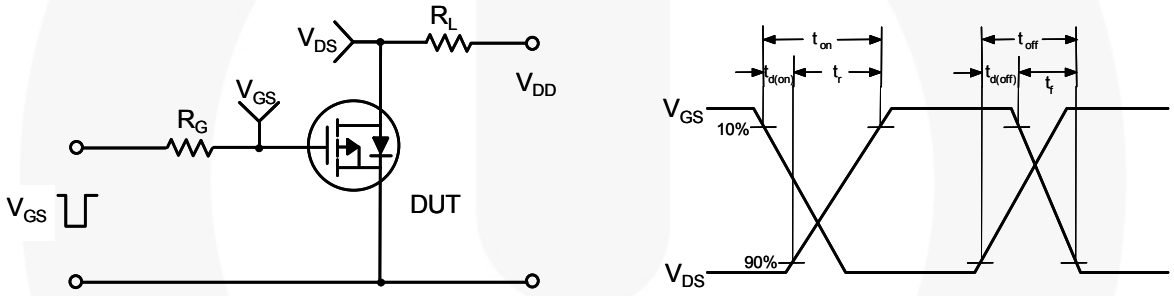


Figure 13. Resistive Switching Test Circuit & Waveforms

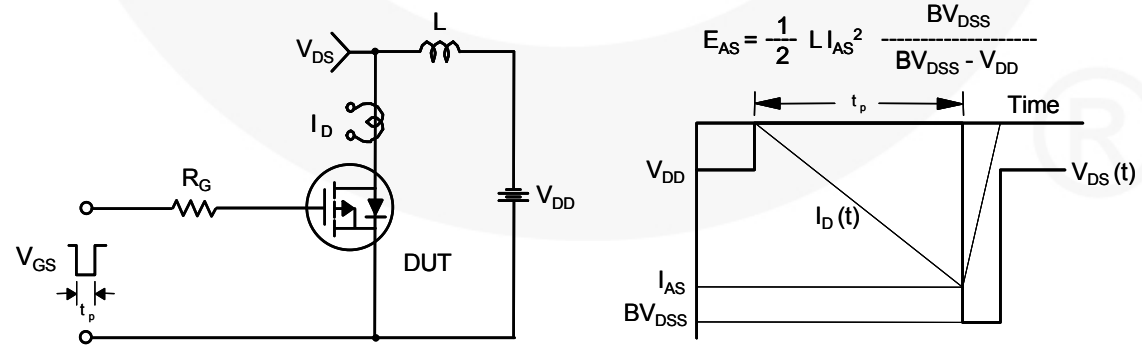


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

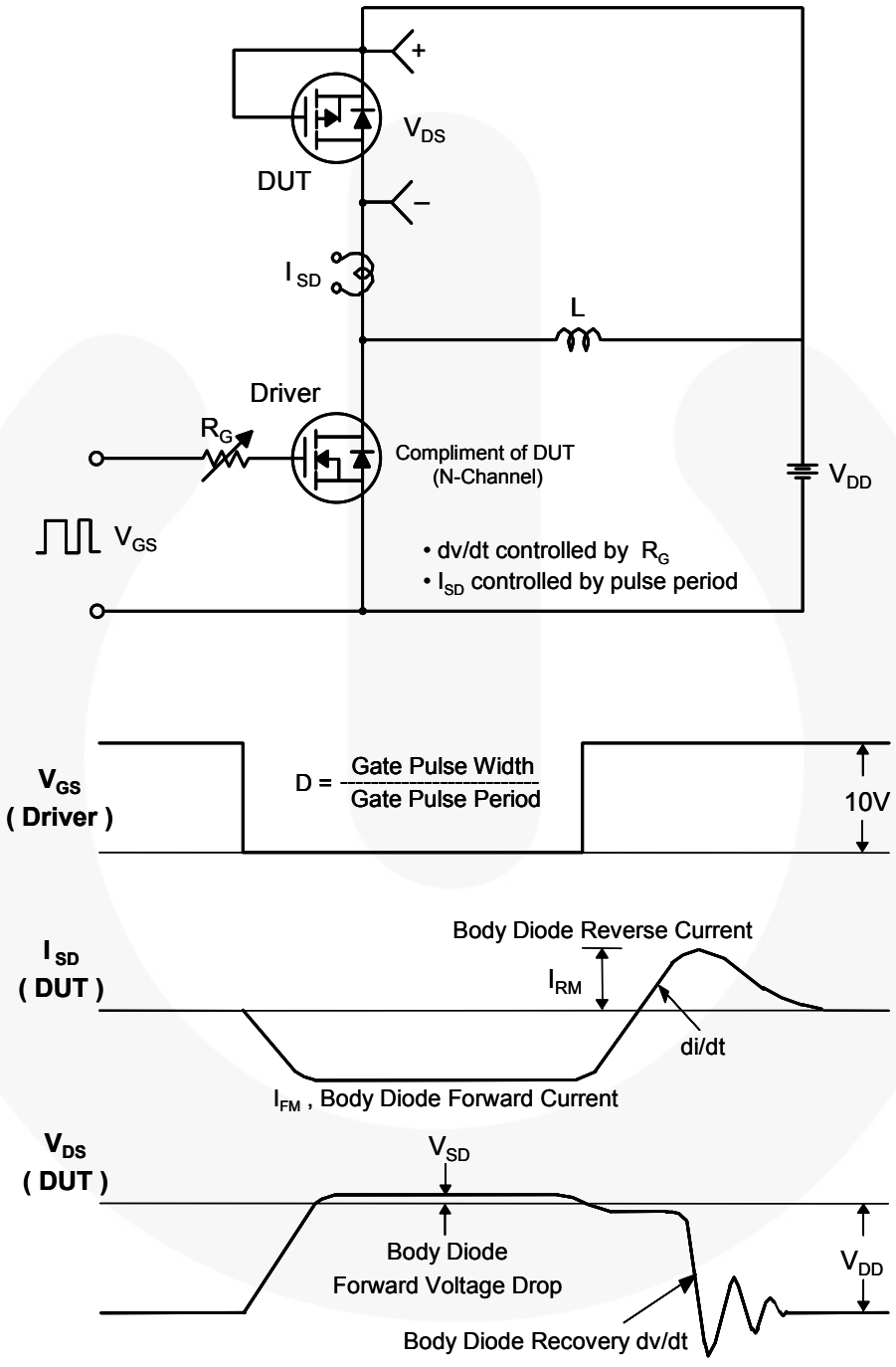
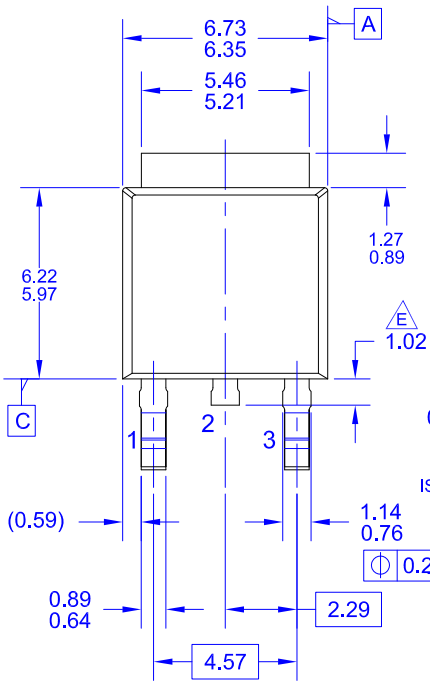
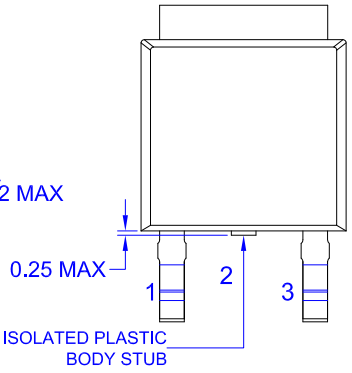


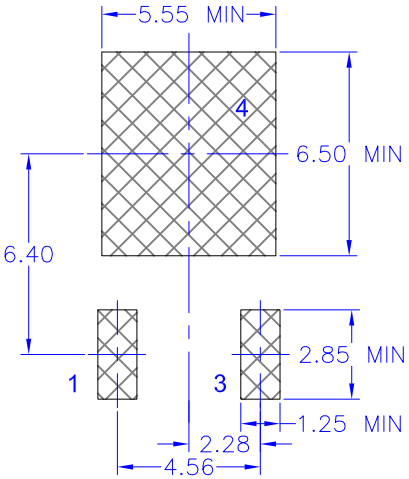
Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms



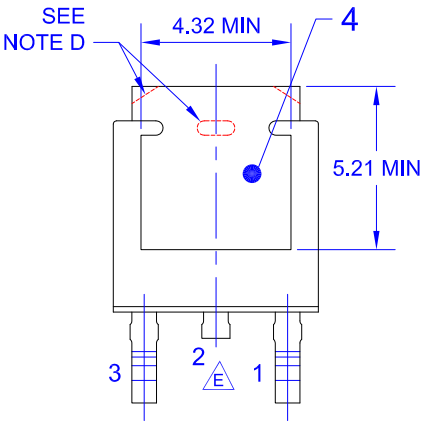
NON-DIODE PRODUCTS VERSION



DIODE PRODUCTS VERSION



LAND PATTERN RECOMMENDATION



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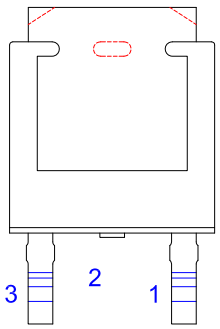

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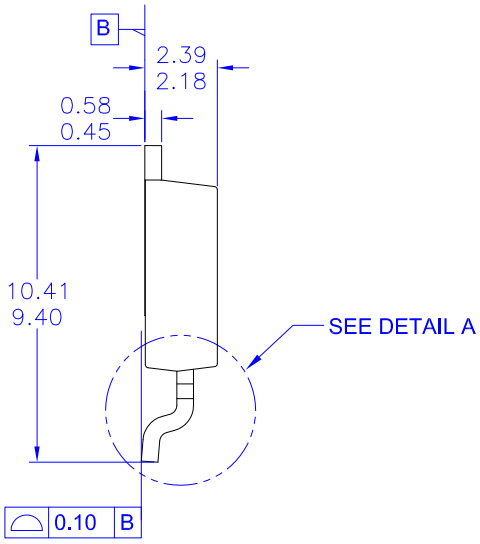
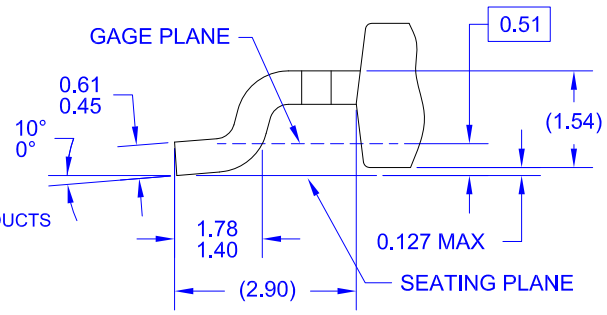


NOTES: UNLESS OTHERWISE SPECIFIED

A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
E) TRIMMED METAL CENTER LEAD IS PRESENT ON FOR NON-DIODE PRODUCTS
F) DIMENSIONS ARE EXCLUSIVE OF BURS, MOLD FLASH AND TIE BAR EXTRUSIONS.
G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.
H) DRAWING NUMBER AND REVISION: MKT-TO252A03REV11



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