8-String, White LED Driver with SMBus and PWM Input for LCD Backlight Applications

ADD5203

FEATURES

- **White LED driver based on inductive boost converter**
  - **Integrated 50 V MOSFET with 2.9 A peak current limit**
  - **Input voltage range: 6 V to 21 V**
  - **Maximum output adjustable up to 45 V**
  - **350 kHz to 1 MHz adjustable operating frequency**
  - **Overvoltage protection (OVP) up to typical 47.5 V**
  - **Built-in soft start for boost converter**
- **Drives up to eight LED current strings**
  - **LED current adjustable up to 30 mA for each channel**
  - **Headroom control to maximize efficiency**
  - **Adjustable dimming frequency: 200 Hz to 10 kHz**
  - **LED open and short fault protection**
- **Selectable dimming control interface methods**
  - **PWM input**
  - **SMBus serial input**
- **Selectable dimming modes**
  - **Fixed delay PWM dimming control with 8-bit resolution**
  - **No delay PWM dimming control with 8-bit resolution**
  - **Direct PWM dimming control**
  - **DC current dimming control with 8-bit resolution**
- **General**
  - **Thermal shutdown**
  - **Undervoltage lockout**
  - **28-lead, 4 mm × 4 mm × 0.75 mm LFCSP_WQ**

APPLICATIONS

Notebook PCs, UMPCs, and monitor displays

FUNCTIONAL BLOCK DIAGRAM

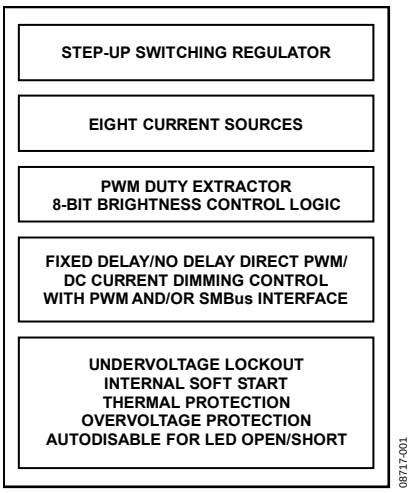

Figure 1.

GENERAL DESCRIPTION

The ADD5203 is a white LED driver for backlight applications based on high efficiency, current-mode, step-up converter technology. It is designed with a 0.15 Ω, 2.9 A internal switch and a pin-adjustable operating frequency between 350 kHz and 1 MHz.

The ADD5203 contains eight regulated current sources for uniform brightness intensity. Each current source can be driven up to 30 mA, and the LED driving current is pin adjustable by an external resistor. The ADD5203 drives up to eight parallel strings of multiple series connected LEDs with a ±1.5% current matching between strings.

The ADD5203 provides various dimming modes. Each dimming mode is selectable with an external dimming mode selection pin. The LED dimming control interface can be achieved through PWM input and/or SMBus. The device provides adjustable output dimming frequency range from 200 Hz to 10 kHz by an external resistor and capacitor. The ADD5203 operates over an input voltage range of 6 V to 21 V, but the device can function with a voltage as low as 5.6 V.

The ADD5203 also has multiple safety protection features to prevent damage during fault conditions. If any LED is open or short, the device automatically disables the faulty current source. The internal soft start prevents inrush current during startup. Thermal shutdown protection prevents thermal damage.

The ADD5203 is available in a low profile, thermally enhanced, 4 mm × 4 mm × 0.75 mm, 28-lead, RoHS-compliant lead frame chip scale package (LFCSP_WQ) and is specified over the industrial temperature range of −25°C to +85°C.

Rev. 0

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REVISION HISTORY

5/10—Revision 0: Initial Version

CIRCUIT DIAGRAM

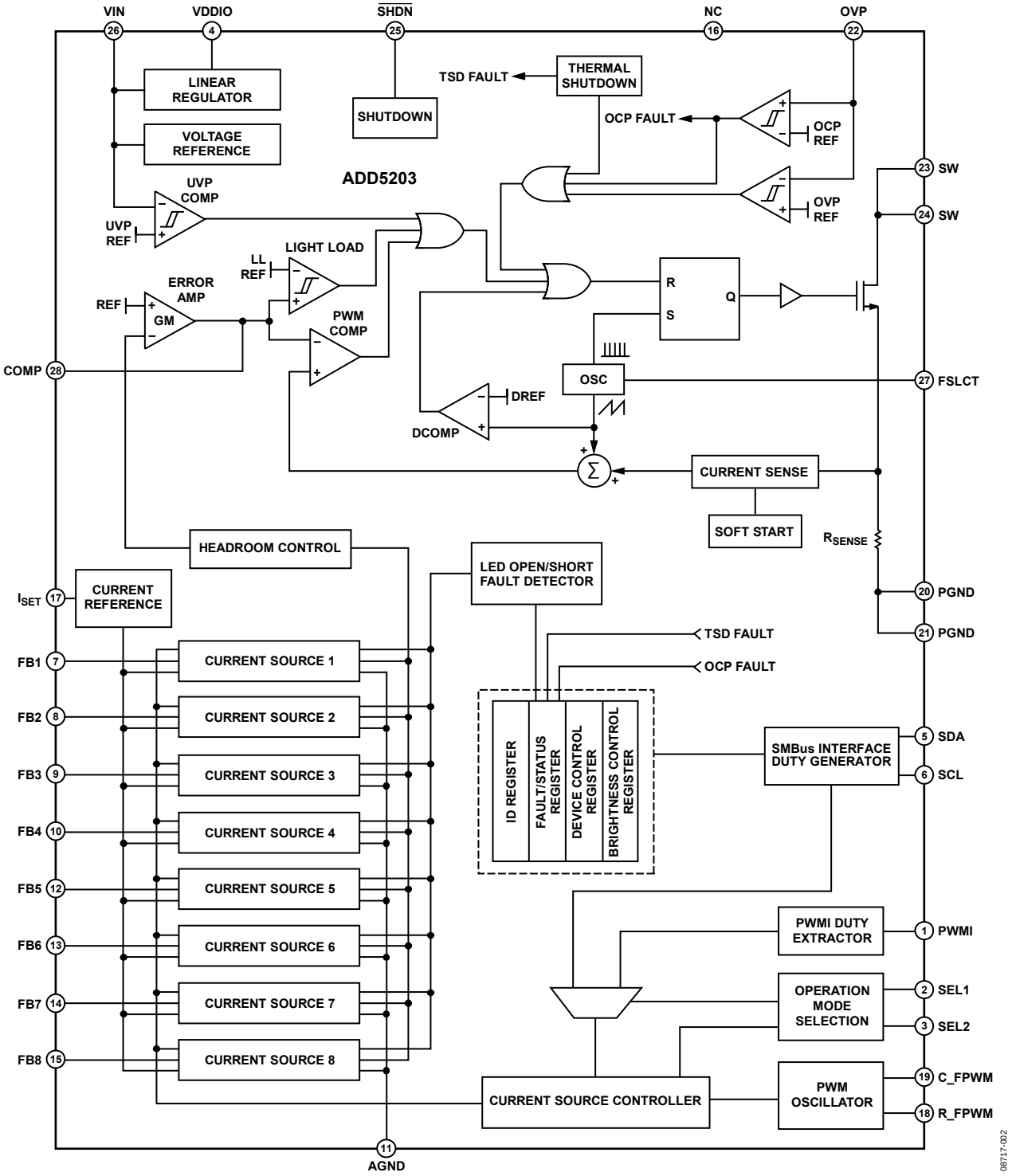


Figure 2. Circuit Diagram

SPECIFICATIONS

STEP-UP SWITCHING REGULATOR SPECIFICATIONS

V_{IN} = 12 V, $\overline{SHDN}$ = high, T_A = −25°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.

Table 1.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SUPPLY						
Input Voltage Range	V_{IN}		6		21	V
BOOST OUTPUT						
Output Voltage	V_{OUT}				45	V
SWITCH						
On Resistance	$R_{DS(ON)}$	V_{IN} = 12 V, I_{SW} = 100 mA		150	210	mΩ
Leakage Current	I_{LKG}			44	70	µA
Peak Current Limit	I_{CL}	Duty cycle (D) = D_{MAX}	2.9			A
OSCILLATOR						
Switching Frequency	f_{SW}	R_F = 150 kΩ	800	1000	1200	kHz
	f_{SW}	R_F = 470 kΩ		350		kHz
Maximum Duty Cycle	D_{MAX}	R_F = 470 kΩ	85	92		%
SOFT START						
Soft Start Time	t_{SS}			1.5		ms
OVERVOLTAGE PROTECTION						
Overvoltage Rising Threshold on OVP Pin	V_{OVPR}		1.154	1.20	1.267	V
Overvoltage Falling Threshold on OVP Pin	V_{OVPF}		1.050	1.12	1.188	V

LED CURRENT REGULATION SPECIFICATIONS

V_{IN} = 12 V, $\overline{SHDN}$ = high, T_A = −25°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.

Table 2.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
CURRENT SOURCE						
I_{SET} Pin Voltage	V_{SET}	6 V ≤ V_{IN} ≤ 21 V	1.16	1.2	1.24	V
Adjustable LED Current[1]	I_{LED}		0		30	mA
Constant Current Sink of 20 mA[2]	I_{LED20}	R_{SET} = 141.56 kΩ	19.4	20	20.6	mA
Minimum Headroom Voltage[2]	V_{HR20}	R_{SET} = 141.56 kΩ		0.65	0.85	V
Current Matching Between Strings[2]		R_{SET} = 141.56 kΩ	−1.5		+1.5	%
LED Current Accuracy[2]		R_{SET} = 141.56 kΩ	−3		+3	%
Current Source Leakage Current					1	µA
FPWM GENERATOR						
Dimming Frequency Range		6 V ≤ V_{IN} ≤ 21 V	200		10,000	Hz
Dimming Frequency	f_{PWM}	R_{FPWM} = 50 kΩ, C_{FPWM} = 150 pF	820	1000	1180	Hz
LED FAULT DETECTION						
Open Fault Delay[1]	$T_{D\_OPENFAULT}$				6.5	µs

[1] These electrical specifications are guaranteed by design.
[2] Tested at T_A = +25°C.

SMBUS SPECIFICATIONS

V_{IN} = 12 V, $\overline{SHDN}$ = high, T_A = −25°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.

Table 3.

Parameter[1]	Symbol	Test Conditions	Min	Typ	Max	Unit
SMBus INTERFACE						
Data, Clock Input Low Level	V_{IL}				0.8	V
Data, Clock Input High Level	V_{IH}		2.1		5.5	V
Data, Clock Output Low Level	V_{OL}				0.4	V
SMBus TIMING SPECIFICATIONS						
Clock Frequency	f_{SMB}		10		100	kHz
Bus-Free Time Between Stop and Start Condition	t_{BUF}		4.7			µs
Hold Time After Start Condition[2]	$t_{HD:STA}$		4.0			µs
Repeated Start Condition Setup Time	$t_{SU:STA}$		4.7			µs
Stop Condition Setup Time	$t_{SU:STO}$		4.0			µs
Data Hold Time	$t_{HD:DAT}$		300			ns
Data Setup Time	$t_{SU:DAT}$		250			ns
Clock Low Period	t_{LOW}		4.7			µs
Clock High Period	t_{HIGH}		4.0		50	µs
Clock/Data Fall Time	t_F				300	ns
Clock/Data Rise Time	t_R				1	us

[1] These electrical specifications are guaranteed by design.
[2] After this period, the first clock is generated.

GENERAL SPECIFICATIONS

V_{IN} = 12 V, $\overline{SHDN}$ = high, T_A = −25°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.

Table 4.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SUPPLY						
Input Voltage Range	V_{IN}		6		21	V
Quiescent Current	I_Q	6 V ≤ V_{IN} ≤ 21 V, $\overline{SHDN}$ = high		4.2	6.5	mA
Shutdown Supply Current	I_{SD}	6 V ≤ V_{IN} ≤ 21 V, $\overline{SHDN}$ = low		40	160	µA
VDD REGULATOR						
VDD Regulated Output	V_{VDD_REG}	6 V ≤ V_{IN} ≤ 21 V	3.18	3.3	3.42	V
PWM INPUT						
PWM Voltage High	V_{PWM_HIGH}		2.2		5.5	V
PWM Voltage Low	V_{PWM_LOW}				0.8	V
PWM Input Range			200		10,000	Hz
THERMAL SHUTDOWN						
Thermal Shutdown Threshold[1]	T_{SD}			160		°C
Thermal Shutdown Hysteresis[1]	T_{SDHYS}			30		°C
UVLO						
V_{IN} Falling Threshold	V_{UVLOF}	V_{IN} falling	4.2	4.6		V
V_{IN} Rising Threshold	V_{UVLOR}	V_{IN} rising		5.0	5.6	V
$\overline{SHDN}$ CONTROL						
Input Voltage High	V_{IH}		2.0			V
Input Voltage Low	V_{IL}				1.0	V
$\overline{SHDN}$ Pin Input Current	$I_{\overline{SHDN}}$	$\overline{SHDN}$ = 3.3 V		6		µA

[1] These electrical specifications are guaranteed by design.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 5.

Parameter	Rating
VIN	−0.3 V to +23 V
SW	−0.3 V to +50 V
$\overline{SHDN}$, SDA, SCL, PWMI, SEL1, and SEL2	−0.3 V to +6 V
I_{SET}, FSLCT, COMP, R_FPWM, and C_FPWM	−0.3 V to +3.6 V
VDDIO	−0.3 V to +3.7 V
FB1, FB2, FB3, FB4, FB5, FB6, FB7, and FB8	−0.3 V to +50 V
OVP	−0.3 V to +3 V
Maximum Junction Temperature (T_J max)	150°C
Operating Temperature Range (T_A)	−25°C to +85°C
Storage Temperature Range (T_S)	−65°C to +150°C
Reflow Peak Temperature (20 sec to 40 sec)	260°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 6. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
28-Lead LFCSP_WQ	32.6	1.4	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

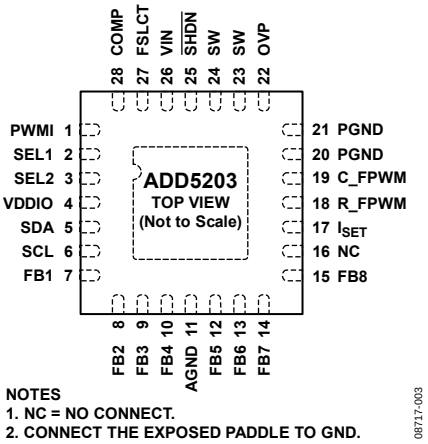


Figure 3. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	PWMI	PWM Signal Input.
2	SEL1	Dimming Mode Selection 1.
3	SEL2	Dimming Mode Selection 2.
4	VDDIO	Internal Linear Regulator Output. This regulator provides power to the ADD5203.
5	SDA	Serial Data Input/Output.
6	SCL	Serial Clock Input.
7	FB1	Regulated Current Sink. Connect the bottom cathode of the LED string to this pin.
8	FB2	Regulated Current Sink. Connect the bottom cathode of the LED string to this pin.
9	FB3	Regulated Current Sink. Connect the bottom cathode of the LED string to this pin.
10	FB4	Regulated Current Sink. Connect the bottom cathode of the LED string to this pin.
11	AGND	Analog Ground.
12	FB5	Regulated Current Sink. Connect the bottom cathode of the LED string to this pin. If unused, connect to GND.
13	FB6	Regulated Current Sink. Connect the bottom cathode of the LED string to this pin. If unused, connect to GND.
14	FB7	Regulated Current Sink. Connect the bottom cathode of the LED string to this pin. If unused, connect to GND.
15	FB8	Regulated Current Sink. Connect the bottom cathode of the LED string to this pin. If unused, connect to GND.
16	NC	No Connection.
17	I_{SET}	Full-Scale LED Current Set. A resistor from this pin to ground sets the LED current up to 30 mA.
18	R_FPWM	Dimming frequency adjustment pin with an external resistor.
19	C_FPWM	Dimming frequency adjustment pin with an external capacitor.
20	PGND	Power Ground.
21	PGND	Power Ground.
22	OVP	Overvoltage Protection.
23	SW	Drain Connection of the Internal Power FET.
24	SW	Drain Connection of the Internal Power FET.
25	$\overline{SHDN}$	Shutdown Control for PWM Input Operation Mode. Active low.
26	VIN	Supply Input. Must be locally bypassed with a capacitor to ground.
27	FSLCT	Frequency Select. A resistor from this pin to ground sets the boost switching frequency from 350 kHz to 1 MHz.
28	COMP	Compensation for Boost Converter. A capacitor and a resistor are connected in series between ground and this pin for stable operation and an optional capacitor can be connected from this pin to ground.
	EP	Exposed Paddle. Connect the exposed paddle to ground.

TYPICAL PERFORMANCE CHARACTERISTICS

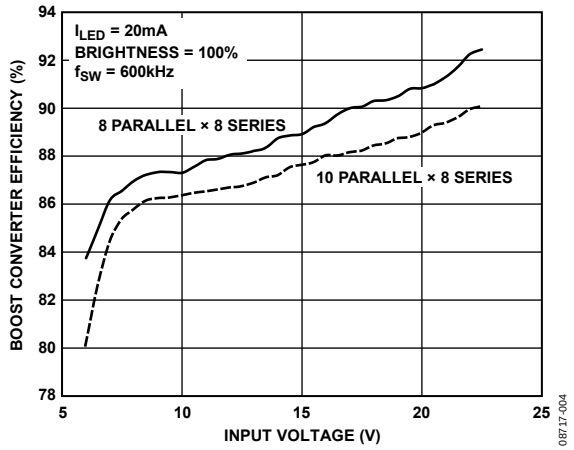


Figure 4. Boost Converter Efficiency vs. Input Voltage

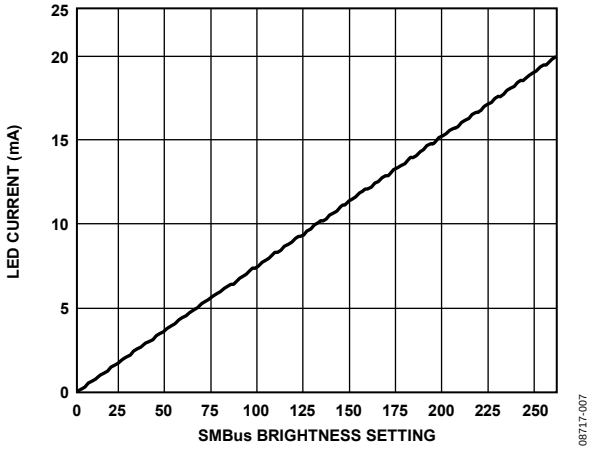


Figure 7. LED Current vs. SMBus Brightness Setting

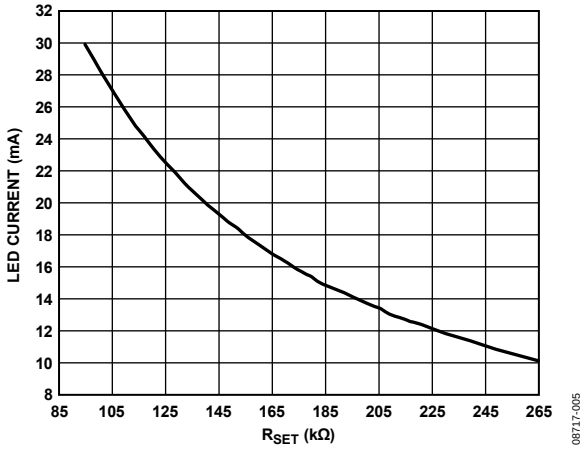


Figure 5. LED Current vs. R_{SET}

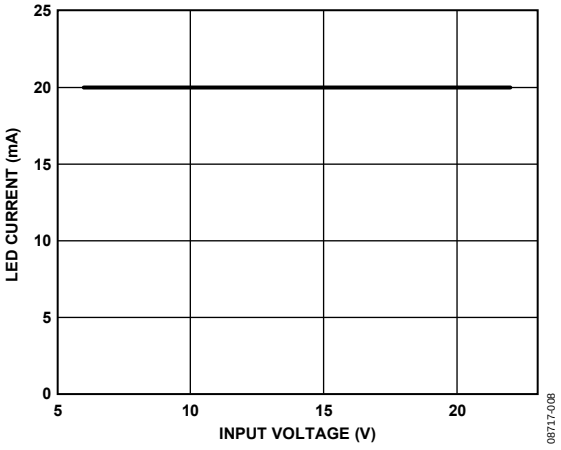


Figure 8. LED Current vs. Input Voltage (I_{LED} = 20 mA)

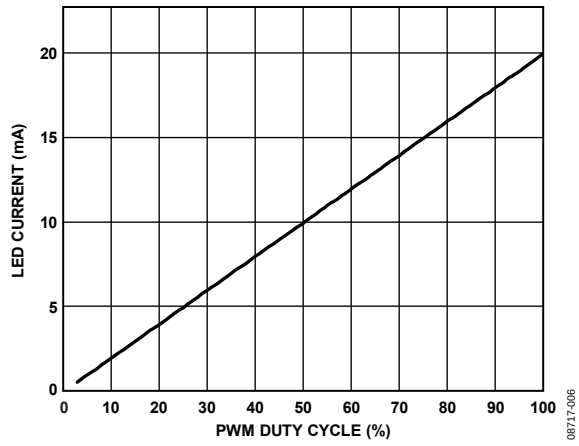


Figure 6. LED Current vs. PWM Input Duty Cycle

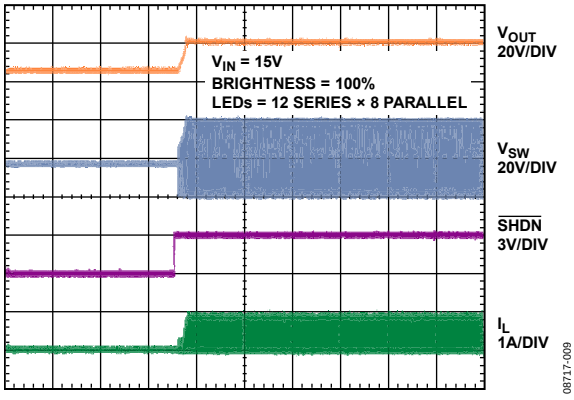


Figure 9. Start-Up Waveforms (Brightness = 100%)

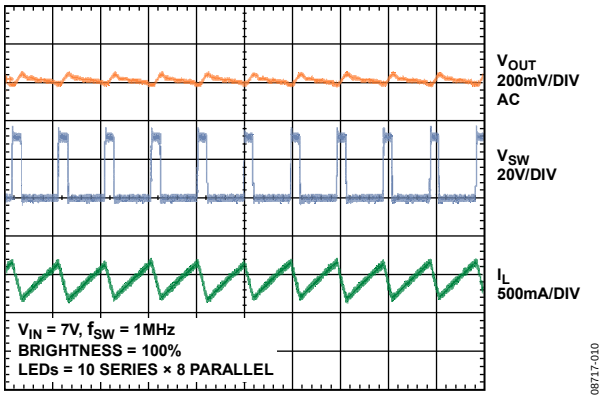


Figure 10. Switching Waveforms (V_{IN} = 7 V)

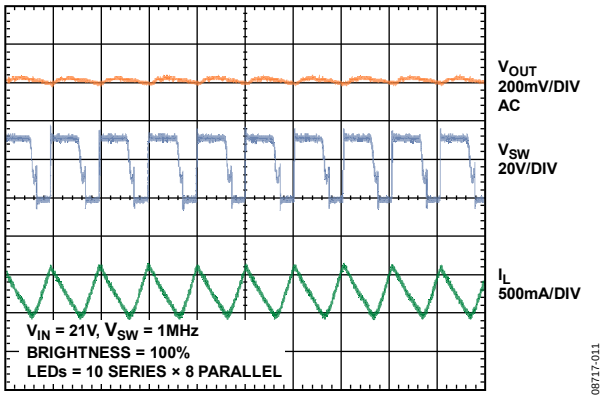


Figure 11. Switching Waveforms (V_{IN} = 21 V)

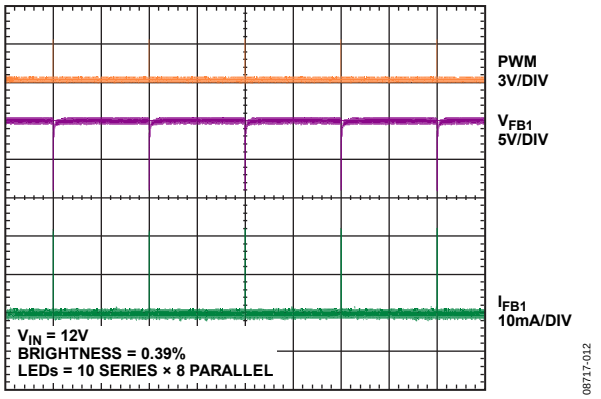


Figure 12. LED Current Waveforms (Brightness = 0.39%)

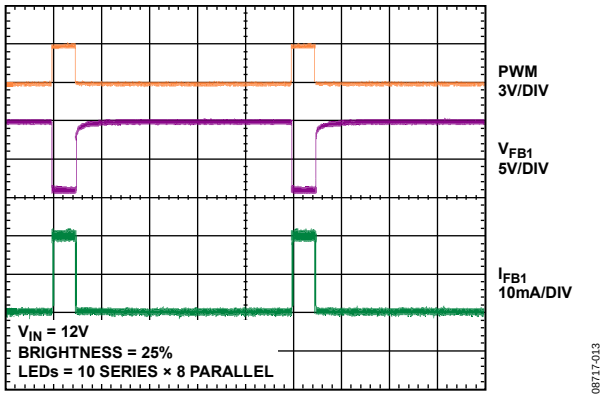


Figure 13. LED FBx Waveforms (Brightness = 10%)

THEORY OF OPERATION

CURRENT-MODE, STEP-UP SWITCHING REGULATOR OPERATION

The ADD5203 uses a current-mode PWM boost regulator to provide the minimal voltage needed to enable the LED string at the programmed LED current. The current-mode regulation system allows fast transient response while maintaining a stable output voltage. By selecting the proper resistor-capacitor network from COMP to GND, the regulator response can be optimized for a wide range of input voltages, output voltages, and load conditions. The ADD5203 can provide a 45 V maximum output voltage and drive up to 13 LEDs (3.4 V/30 mA type of LEDs) for each channel.

INTERNAL 3.3 V REGULATOR

The ADD5203 contains a 3.3 V linear regulator. The regulator is used for biasing internal circuitry. The internal regulator requires a 1 µF bypass capacitor. Place this bypass capacitor between VDDIO (Pin 4) and GND, as close as possible to Pin VDDIO.

BOOST CONVERTER SWITCHING FREQUENCY

The ADD5203 boost converter switching frequency is user adjustable, between 350 kHz to 1 MHz, by using an external resistor, R_F. A frequency of 350 kHz is recommended to optimize the regulator for high efficiency, and a frequency of 1 MHz is recommended for small external components.

See Figure 14 for considerations when selecting a switching frequency and an adjustment resistor (R_F).

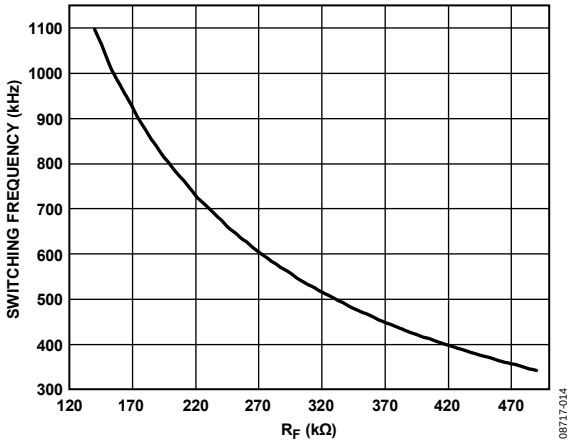


Figure 14. Switching Frequency vs. R_F

DIMMING FREQUENCY (f_{PWM})

The ADD5203 contains an internal oscillator to generate the PWM dimming signal for LED brightness control. The LED dimming frequency (f_{PWM}) is adjustable, in the f_{PWM} range of 200 Hz to 10 kHz, by using an external resistor (R_{FPWM}) and capacitor (C_{FPWM}). The R_{FPWM} should be in the range of 13 kΩ to 110 kΩ, and the C_{FPWM} should be in the range of 20 pF to 390 pF.

Table 8. R_{FPWM} and C_{FPWM} Recommendation

Dimming Freq (f_{PWM})	R_{FPWM} (kΩ)	C_{FPWM} (pF)
200 Hz	110	390
500 Hz	75	200
1 kHz	50	150
5 kHz	18	47
10 kHz	13	20

CURRENT SOURCE

The ADD5203 contains eight current sources to provide accurate current sinking for each LED string. String-to-string tolerance is kept within ±1.5% at 20 mA. Each LED string current is adjusted up to 30 mA by an external resistor.

The ADD5203 contains an LED open and short fault protection circuit for each channel. If the headroom voltage of the current source remains below 200 mV while the boost converter output reaches the OVP level, the ADD5203 recognizes that the current source has an open load fault for the current source, and the current source is disabled. If the headroom voltage of the current source goes above 7.2 V, the current source is disabled for short protection.

If an application requires four LED strings, each LED string should be connected using FB1 to FB4. Tie the unused FB pins (FB5 to FB8) to GND.

The ADD5203 contains hysteresis to prevent the LED current change that is caused by a ±0.195% jitter of the PWM input.

Programming the LED Current

As shown in Figure 2, the ADD5203 has an LED current set pin (I_{SET}). A resistor (R_{SET}) from this pin to ground adjusts the LED current up to 30 mA. LED current level can be set with the following equation:

$$I_{LED} = \frac{2831}{R_{SET}}(A)$$

DIMMING CONTROL INTERFACE

The ADD5203 dimming control interface method is selectable between the SMBus serial input and/or the external PWM input. The LED dimming modes supported by ADD5203 can be controlled externally through these dimming control interfaces. The SEL1 and SEL2 pins should be set based on the application conditions (see Table 9).

Table 9. Brightness Control Mode Selection

SEL1	SEL2	Dimming Mode	Interface
High	High	Fixed delay PWM	SMBus
	Low	No delay PWM	SMBus
Open	High	Fixed delay PWM	PWM
	Low	No delay PWM	PWM
Low	High	DC current	SMBus
	Open	DC current	PWM
	Low	Direct PWM	PWM

PWM DIMMING MODE

The ADD5203 supports an 8-bit resolution to control brightness; therefore, the LED dimming duty is generated with 256 steps through the PWM input duty value in the range of 0% to 100%. In addition, if the PWM input duty cycle is 0% longer than 10 ms, the ADD5203 is disabled.

Note that the ADD5203 has immunity when the PWM input duty cycle is converted to 256 steps. Even the PWM input has ±0.195% jitter.

Fixed Delay PWM Dimming

Fixed delay PWM mode is selected when SEL1 is open and SEL2 is high for a PWM application, or when SEL1 is high and SEL2 is high for an SMBus application. In this mode, each current source has a fixed turn-on time delay between adjacent strings. The fixed delay time is set by the FPWM frequency. Each channel delay time is set by the following equation:

$$t_D = \frac{2 \times t_{FPWM}}{256}$$

where $t_{FPWM} = 1/f_{PWM}$, and f_{PWM} is the LED dimming frequency.

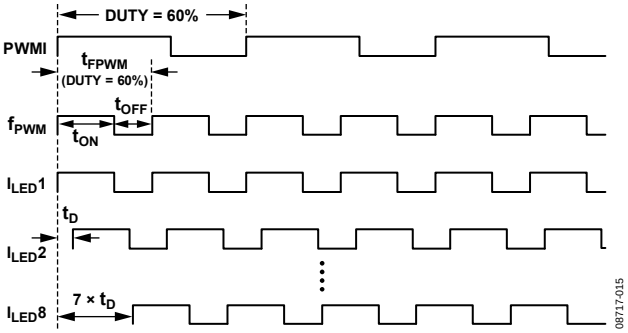


Figure 15. Fixed-Delay PWM Dimming Timing

No Delay PWM Dimming

No-delay PWM mode is selected when SEL1 is open and SEL2 is low for a PWM application or when SEL1 is high and SEL2 is low for an SMBus application. In this mode, each current source turns on and off at the same time without any phase delay.

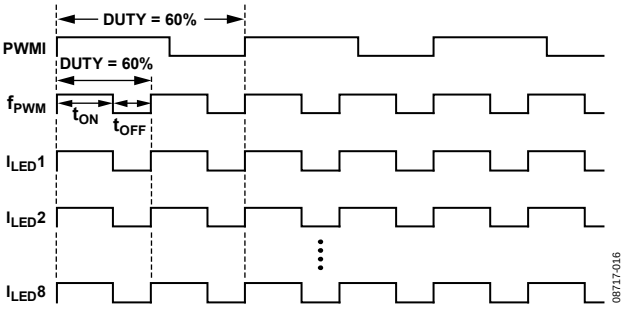


Figure 16. No Delay PWM Dimming Timing

Direct PWM Dimming

Direct PWM mode is selected when SEL1 is low and SEL2 is low for a PWM application. In this mode, the PWM input controls the ADD5203 LED dimming logic. It turns the current sources on and off without any duty extraction. In addition, each current source has no phase delay in this mode. The LED brightness is changed by the PWM input duty ratio.

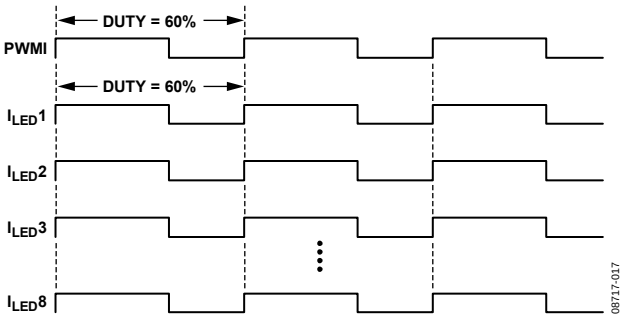


Figure 17. Direct PWM Dimming Timing

DC Current Dimming

DC current mode is selected when SEL1 is low and SEL2 is open for a PWM application, or when SEL1 is low and SEL2 is high for an SMBus application. In this mode, the maximum LED current is set by the value of R_{SET}. Once the maximum LED current is set, the LED current can be changed with 256 steps through PWM input or SMBus.

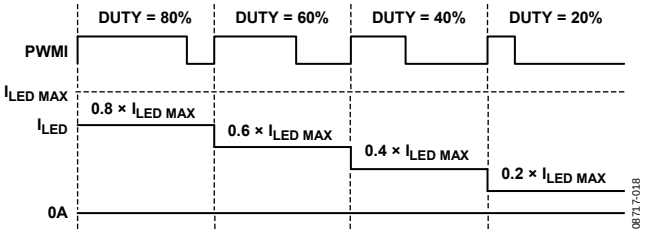


Figure 18. DC Current Dimming Timing

SAFETY FEATURES

The ADD5203 contains several safety features to provide stable operation.

Soft Start

The ADD5203 contains an internal soft start function to reduce inrush current at startup. The soft start time is typically 1.5 ms.

Overvoltage Protection (OVP)

The ADD5203 contains OVP circuits to prevent boost converter damage if the output voltage becomes excessive for any reason. To keep a safe output level, the integrated OVP circuit monitors the output voltage. When the OVP pin voltage is reached by the OVP rising threshold, the boost converter stops switching, causing the output voltage to drop. When the OVP pin voltage goes lower than the OVP falling threshold, the boot converter begins switching, causing the output to rise. There is about 7.5% hysteresis between the rising and falling thresholds. The OVP level can be calculated with the following equation:

$$V_{OVP} = \frac{1.2\,V}{R1} \times (R1 + R2)$$

In general, the suitable OVP level is 5 V higher than the nominal boost switching regulator output. Large resistors, up to 1 MΩ, can be used for R2 to minimize power loss. In addition, some applications require C1 to prevent noise interference at the OVP pin in the range of 10 pF to 30 pF.

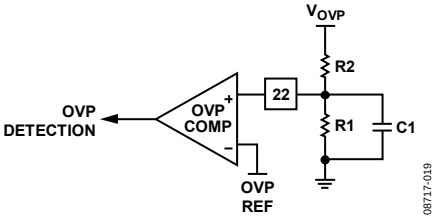


Figure 19. Overvoltage Protection Circuit

Open Load Protection (OLP)

The ADD5203 contains a headroom control circuit to minimize power loss at each current source. Therefore, the minimum feedback voltage is achieved by regulating the output voltage of the boost converter. If any LED string is opened during normal operation, the current source headroom voltage (V_{HR}) is pulled to GND. In this condition, open load protection (OLP) is activated if V_{HR} is less than 200 mV until the boost converter output voltage rises up to the OVP level.

Short-Circuit Protection (SCP)

The ADD5203 contains the short circuit protection (SCP). If a few LEDs at any strings are shorted during normal operation, the current source headroom voltage (V_{HR}) is increasing. In this condition, SCP is activated if V_{HR} is higher than 7.2 V; therefore, the string that includes short LEDs is disabled.

Undervoltage Lockout (UVLO)

An undervoltage lockout circuit is included with built-in hysteresis. The ADD5203 turns on when VIN rises above 5 V (typical) and shuts down when VIN falls below 4.6 V (typical).

Thermal Overload Protection

Thermal overload protection prevents excessive power dissipation from overheating the ADD5203. When the junction temperature (T_J) exceeds 160°C, a thermal sensor immediately activates the fault protection, which shuts down the device, allowing the IC to cool. The device self-starts when the junction temperature (T_J) of the die falls below 130°C.

SMBUS INTERFACE

SMBus mode can be selected using the SEL1 and SEL2 mode selection pins. When in SMBus mode, the ADD5203 can be controlled with an SMBus serial interface.

Read Byte

As shown in Figure 21, the read byte protocol is four bytes long and starts with the slave address followed by the command code, which translates to the register index. Then, the bus direction turns around with the rebroadcast of the slave address, with Bit 0 indicating a read cycle. The fourth byte contains the data being returned by the backlight controller. The byte value in the data byte should reflect the value of the register being queried at the command code index. Note the bus directions, which are shaded in Figure 21 and are used on cycles where the slaved backlight controller drives the data line. All other cycles are driven by the host master.

Write Byte

The write byte protocol is only three bytes long. The first byte starts with the slave address followed by the command code, which translates to the register index being written. The third byte contains the data byte that must be written into the register selected by the command code. Note the bus directions, which are shaded in Figure 22 and are used on cycles where the slaved backlight controller drives the data line. All other cycles are driven by the host master.

Slave Device Address

As shown in Figure 23, the ADD5203 address consists of seven address bits plus one read/write (R/$\overline{W}$) bit. If the device is in write mode, the LSB is set to 0 and the slave address byte is 0x58. If the device is in read mode, the LSB is set to 1 and the slave address byte is 0x59.

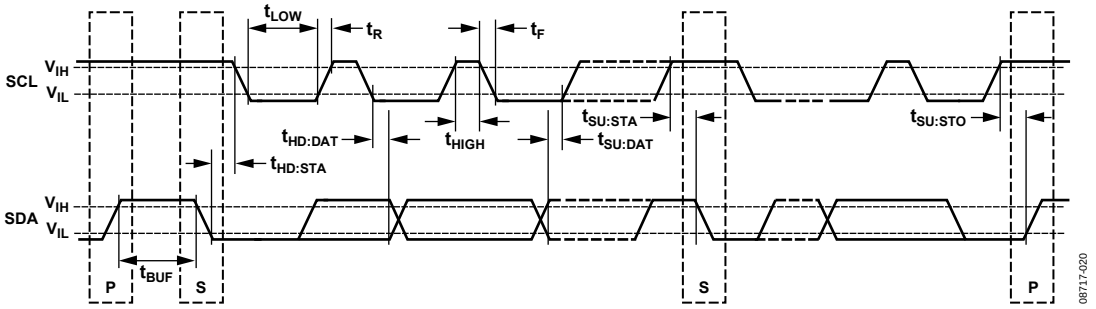


Figure 20. SMBus Interface

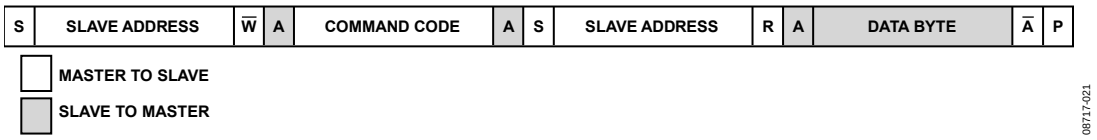


Figure 21. Read Byte Protocol

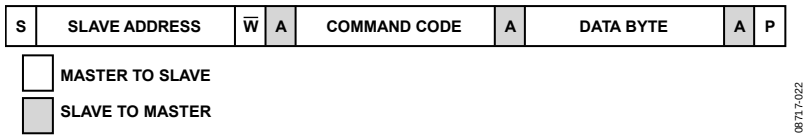


Figure 22. Write Byte Protocol

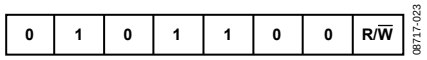


Figure 23. Slave Address Definition

SMBUS REGISTER DESCRIPTION

The ADD5203 has four registers to control and monitor brightness, fault status, identifications, and operating mode. Those registers are one byte wide and accessible via the SMBus read/write byte protocols.

Brightness Control Register (Address 0x00)

This register consists of eight bits, BRT7 to BRT0, which are used to control the LED brightness level in 256 steps. An SMBus write byte cycle to this register sets the brightness level if the device is in SMBus mode. In addition, a write byte cycle to this register sets the brightness level if the device is in SMBus mode. Furthermore, a write byte cycle to this register has no effect when the device is in a mode other than SMBus mode. The operating mode is selected by the device control register (Address 0x01).

An SMBus read byte cycle to this register returns the current brightness level, regardless of the value of PWM_SEL. An SMBus setting of 0xFF for this register sets the device to the maximum brightness output, and a setting of 0x00 sets the device to the minimum brightness output.

This register is both readable and writable for all bits. The default value is 0xFF.

Device Control Register (Address 0x01)

This register has three bits. Two bits control the operation mode of the device, and a single bit controls the backlight on/off state. This register is both readable and writable for Bit 0 to Bit 2. Bit 0, named BL_CTL, is used as on/off control for the output LEDs. Bit 1 and Bit 2, named PWM_SEL and PWM_MD, control the operating mode of the device, respectively. If the BL_CRT bit is set to 1, the device turns on the backlight within 10 ms after the write cycle. If the BL_CRT bit is set to 0, the device turns off the backlight immediately. The ADD5203 output operating mode is selected by the combination of Bit 1 and Bit 2 (see Table 10).

The PWM_MD bit selects the manner in which the PWM input is to be interpreted. When this bit is 0, the PWM input reflects a percent change in the current brightness (that is, DPST mode) and should be as follows:

$$DPST\ Brightness = C_{BT} \times (PWM)$$

where:
C_{BT} is the current brightness setting from SMBus without influence from the PWM.

PWM is the percent duty cycle.

The PWM signal starts from 100% when operating in DPST mode.

When PWM_MD is 1, the PWM input has no effect on the brightness setting, unless the ADD5203 is in PWM mode. In addition, when operating in PWM mode, this bit is a do not care (see Table 10). The PWM_SEL bit determines whether the SMBus or PWM input should drive brightness.

The relationship between these two control bits can be thought of as specifying an operating mode for the ADD5203. The defined modes are shown in Table 10. Note that depending on the setting of some bits, other bits have no effect and are do not cares, shown as X in Table 10.

Table 10. Operating Modes Selected by Device Control Register Bit 1 and Bit 2

PWM_SEL (Bit 1)	PWM_MD[1] (Bit 2)	Mode
1	X	PWM mode
0	1	SMBus mode
0	0	SMBus mode with DPST

[1] X is don't care.

All reserved bits return to 0 when read, and the bits are ignored when written. This default value of the register is 0x00.

Table 11. Brightness Control Register (Address 0x00) Bit Map

MSB								LSB
Bit 7 (R/$\overline{W}$)	**Bit 6 (R/$\overline{W}$)**	**Bit 5 (R/$\overline{W}$)**	**Bit 4 (R/$\overline{W}$)**	**Bit 3 (R/$\overline{W}$)**	**Bit 2 (R/$\overline{W}$)**	**Bit 1 (R/$\overline{W}$)**	**Bit 0 (R/$\overline{W}$)**	**Default Value**
BRT7	BRT6	BRT5	BRT4	BRT3	BRT2	BRT1	BRT0	0xFF

Table 12. Brightness Control Register (Address 0x00) Bit Description

Bit Name	Description
BRT[7:0]	256 steps of brightness levels

Table 13. Device Control Register (Address 0x01) Bit Map

MSB								LSB
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2 (R/$\overline{W}$)**	**Bit 1 (R/$\overline{W}$)**	**Bit 0 (R/$\overline{W}$)**	**Default Value**
Reserved	Reserved	Reserved	Reserved	Reserved	PWM_MD	PWM_SEL	BL_CTL	0x00

Table 14. Device Control Register (Address 0x01) Bit Description

Bit Name	Description
PWM_MD	PWM mode select 1 = absolute brightness, 0 = percent change (default)
PWM_SEL	Brightness control select 1 = control by PWM, 0 = control by SMBus (default)
BL_CTL	Backlight on/off 1 = on, 0 = off (default)

Fault/Status Register (Address 0x02)

This register has six status bits that allow monitoring of the ADD5203 operating state. Bit 0, named fault, is a logical OR of all fault codes to simplify error detection. In the operation of the ADD5203, Bit 1, named THRM_SHDN, is set to 1 when a thermal shutdown event occurs. Bit 3, named BL_STAT, is the backlight status indicator. This bit is set to 1 whenever the backlight is on and is set to 0 whenever the backlight is off. Bit 4, named 1_CH_SD, is set to 1 if one or more current sources are disabled. In addition, Bit 5, named 2_CH_SD, is set to 1 if two or more current sources are disabled due to an LED open event during normal operation. All reserved bits return to 0 when read and ignore the bit value when written. All of the bits in this register are read only. The default value for Register 0x02 is 0x00.

Identification Register (Address 0x03)

The ID register contains two bit fields to denote the manufacturer and silicon revision of the ADD5203. The bit field widths were chosen to allow up to 16 vendors with up to eight silicon revisions each. To ensure that the number of silicon revisions remains low, the revision field should not be updated until the part is sent to the factory of the end-customer. Therefore, if during the engineering development process, three silicon spins are needed before the device is released to the factory of the end-customer, the next available revision ID is used for these three spins. The manufacturer ID of Analog Devices, Inc., is 6 (Bit[6:3] = 0110b). In addition, the initial value of REVx is 0, and subsequent REVx values are incremented by 1. This register is read only.

Table 15. Fault/Status Register (Address 0x02) Bit Map

MSB								LSB
Bit 7	**Bit 6**	**Bit 5 (R)**	**Bit 4 (R)**	**Bit 3 (R)**	**Bit 2 (R)**	**Bit 1 (R)**	**Bit 0 (R)**	**Default Value**
Reserved	Reserved	2_CH_SD	1_CH_SDS	BL_STAT	OV_CURR	THRM_SHDN	Fault	0x00

Table 16. Fault/Status Register (Address 0x01) Bit Description

Bit Name	Description
2_CH_SD_, 1_CH_SD	The number of faulted strings is reported in these bits. 00 = no faults, 01 = one string fault, 11 = two or more strings faulted.
BL_STAT	Backlight status. 1 = backlight on, 0 = backlight off (default).
OV_CURR	Input overcurrent. 1 = overcurrent condition, 0 = current ok (default).
THRM_SHDN	Thermal shutdown. 1 = thermal fault, 0 = thermal ok (default).
Fault	Fault occurred. Logic OR of all the fault conditions.

Table 17. Identification Register (Address 0x03) Bit Map

MSB								LSB
Bit 7	**Bit 6**	**Bit 5 (R)**	**Bit 4 (R)**	**Bit 3 (R)**	**Bit 2 (R)**	**Bit 1 (R)**	**Bit 0 (R)**	**Default Value**
LED panel	MFG3	MFG2	MFG1	MFG0	REV2	REV1	REV0	0xB0

Table 18. Identification Register (Address 0x03) Bit Description

Bit Name	Description
LED Panel	Display panel using LED backlight, Bit 7 = 1.
MFG[3:0]	Manufacturer ID (Analog Devices ID is 6).
REV[2:0]	Silicon revision (Revision 0 to Revision 7 are allowed for silicon spins).

EXTERNAL COMPONENT SELECTION GUIDE

Inductor Selection

The inductor is an integral part of the step-up converter. It stores energy during the switch-on time and transfers that energy to the output through the output diode during the switch-off time. An inductor in the range of 4.7 µH to 22 µH is recommended. In general, lower inductance values result in higher saturation current and lower series resistance for a given physical size. However, lower inductance results in higher peak current, which can lead to reduced efficiency and greater input and/or output ripple and noise. Peak-to-peak inductor ripple current at close to 30% of the maximum dc input current typically yields an optimal compromise.

The input (V_{IN}) and output (V_{OUT}) voltages determine the switch duty cycle (D), which in turn can be used to determine the inductor ripple current.

$$D = \frac{V_{OUT} - V_{IN}}{V_{OUT}}$$

Use the duty cycle and switching frequency (f_{SW}) to determine the on time.

$$t_{ON} = \frac{D}{f_{SW}}$$

The inductor ripple current (ΔI_L) in a steady state is

$$\Delta I_L = \frac{V_{IN} \times t_{ON}}{L}$$

Solve for the inductance value (L).

$$L = \frac{V_{IN} \times t_{ON}}{\Delta I_L}$$

Make sure that the peak inductor current (that is, the maximum input current plus half of the inductor ripple current) is less than the rated saturation current of the inductor. In addition, ensure that the maximum rated rms current of the inductor is greater than the maximum dc input current to the regulator.

For duty cycles greater than 50% that occur with input voltages greater than half the output voltage, slope compensation is required to maintain stability of the current-mode regulator. The inherent open-loop stability causes subharmonic instability when the duty ratio is greater than 50%. To avoid subharmonic instability, the slope of the inductor current should be less than half of the compensation slope.

Inductor manufacturers include Coilcraft, Inc., Sumida Corporation, and Toko.

Input and Output Capacitors Selection

The ADD5203 requires input and output bypass capacitors to supply transient currents while maintaining a constant input and output voltage. Use a low effective series resistance (ESR) 10 µF or greater capacitor for the input capacitor to prevent noise at the ADD5203 input. Place the input between the VIN and GND, as close as possible to the ADD5203. Ceramic capacitors are preferred because of their low ESR characteristics. Alternatively, use a high value, medium ESR capacitor in parallel with a 0.1 µF low ESR capacitor as close as possible to the ADD5203.

The output capacitor maintains the output voltage and supplies current to the load while the ADD5203 switch is on. The value and characteristics of the output capacitor greatly affect the output voltage ripple and stability of the regulator. Use a low ESR output capacitor; ceramic dielectric capacitors are preferred.

For very low ESR capacitors, such as ceramic capacitors, the ripple current due to the capacitance is calculated as follows. Because the capacitor discharges during the on time (t_{ON}), the charge removed from the capacitor (Q_C) is the load current multiplied by the on time. Therefore, the output voltage ripple (ΔV_{OUT}) is

$$\Delta V_{OUT} = \frac{Q_C}{C_{OUT}} = \frac{I_L \times t_{ON}}{C_{OUT}}$$

where:
C_{OUT} is the output capacitance.
I_L is the average inductor current.

Using the duty cycle and switching frequency (f_{SW}), users can determine the on time with the following equation:

$$t_{ON} = \frac{D}{f_{SW}}$$

The input (V_{IN}) and output (V_{OUT}) voltages determine the switch duty cycle (D) with the following equation:

$$D = \frac{V_{OUT} - V_{IN}}{V_{OUT}}$$

Choose the output capacitor based on the following equation:

$$C_{OUT} \geq \frac{I_L \times (V_{OUT} - V_{IN})}{f_{SW} \times V_{OUT} \times \Delta V_{OUT}}$$

Capacitor manufacturers include Murata Manufacturing Co., Ltd., AVX, Sanyo, and Taiyo Yuden Co., Ltd.

Diode Selection

The output diode conducts the inductor current to the output capacitor and loads while the switch is off. For high efficiency, minimize the forward voltage drop of the diode. Schottky diodes are recommended. However, for high voltage, high temperature applications, where the Schottky diode reverse leakage current becomes significant and can degrade efficiency, use an ultrafast junction diode. The output diode for a boost regulator must be chosen depending on the output voltage and the output current. The diode must be rated for a reverse voltage equal to or greater than the output voltage used. The average current rating must be greater than the maximum load current expected, and the peak current rating must be greater than the peak inductor current. Using Schottky diodes with lower forward voltage drop decreases power dissipation and increases efficiency. The diode must be rated to handle the average output load current. Many diode

manufacturers derate the current capability of the diode as a function of the duty cycle. Verify that the output diode is rated to handle the average output load current with the minimum duty cycle.

The minimum duty cycle of the ADD5203 is

$$D_{MIN} = \frac{V_{OUT} - V_{IN\_MAX}}{V_{OUT}}$$

where V_{IN_MAX} is the maximum input voltage.

For example, D_{MIN} is 0.5 when V_{OUT} is 30 V and V_{IN_MAX} is 15 V.

Schottky diode manufacturers include ON Semiconductor, Diodes Incorporated, Central Semiconductor Corp., and Sanyo.

Loop Compensation

The external inductor, output capacitor, and the compensation resistor and capacitor determine the loop stability. The inductor and output capacitor are chosen based on performance, size, and cost. The compensation resistor (R_C) and compensation capacitor (C_C) at the COMP pin are selected to optimize control loop stability.

For most applications, the compensation resistor should be in the range of 500 Ω to 30 kΩ , and the compensation capacitor should be in the range of 100 pF to 330 nF.

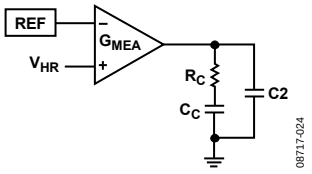


Figure 24. Compensation Components

A step-up converter produces an undesirable right-half plane zero in the regulation feedback loop. Capacitor C2 is chosen to cancel the zero introduced by output capacitance ESR. Solving for C2

$$C2 = \frac{ESR \times C_{OUT}}{R_C}$$

For low ESR output capacitance, such as with a ceramic capacitor, C2 is optional.

LAYOUT GUIDELINES

When designing a high frequency, switching, regulated power supply, layout is very important. Using a good layout can solve many problems associated with these types of supplies. The main problems are loss of regulation at high output current and/or large input-to-output voltage differentials, excessive noise on the output and switch waveforms, and instability. Using the following guidelines can help minimize these problems.

Make all power (high current) traces as short, direct, and thick as possible. It is good practice on a standard printed circuit board (PCB) to make the traces an absolute minimum of 15 mil (0.381 mm) per ampere. Place the inductor, output capacitors, and output diode as close to each other as possible. This helps reduce the EMI radiated by the power traces that are due to the high switching currents through them. This also reduces lead inductance and resistance, which, in turn, reduce noise spikes, ringing, and resistive losses that produce voltage errors. The grounds of the IC, input capacitors, output capacitors, and output diode (if applicable), should be connected close together, directly to a ground plane. It is also a good idea to have a ground plane on both sides of the PCB. This reduces noise by reducing ground loop errors and by absorbing more of the EMI radiated by the inductor.

For multilayer boards of more than two layers, a ground plane can be used to separate the power plane (power traces and components) and the signal plane (feedback, compensation, and components) for improved performance. On multilayer boards, the use of vias is required to connect traces and different planes. If a trace needs to conduct a significant amount of current from one plane to the other, it is good practice to use one standard via per 200 mA of current. Arrange the components so that the switching current loops curl in the same direction.

Due to how switching regulators operate, there are two power states: one state when the switch is on, and one when the switch is off. During each state, there is a current loop made by the power components currently conducting. Place the power components so that the current loop is conducting in the same direction during each of the two states. This prevents magnetic field reversal caused by the traces between the two half cycles and reduces radiated EMI.

Layout Procedure

To achieve high efficiency, good regulation, and stability, a good PCB layout is required. It is recommended that the reference board layout be followed as closely as possible because it is already optimized for high efficiency and low noise.

Use the following general guidelines when designing PCBs:

- Keep C_{IN} close to the V_{IN} and GND leads of the ADD5203.
- Keep the high current path from C_{IN} (through L1) to the SW and GND leads as short as possible.
- Keep the high current path from C_{IN} (through L1), D1, and C_{OUT} as short as possible.
- Keep high current traces as short and wide as possible.
- Keep nodes connected to SW away from sensitive traces, such as COMP, to prevent coupling of the traces. If such traces need to be run near each other, place a ground trace between the two as a shield.
- Place the compensation components as close as possible to the COMP pin.
- Place the LED current setting resistors as close as possible to each pin to prevent noise pickup.
- Avoid routing noise sensitive traces near high current traces and components, especially the LED current setting node (I_{SET}).
- Use a thermal pad size that is the same dimension as the exposed pad on the bottom of the package.

Heat Sinking

When using a surface-mount power IC or external power switches, the PCB can often be used as the heat sink. This is accomplished by using the copper area of the PCB to transfer heat from the device. Users should maximize this area to optimize thermal performance.

TYPICAL APPLICATION CIRCUITS

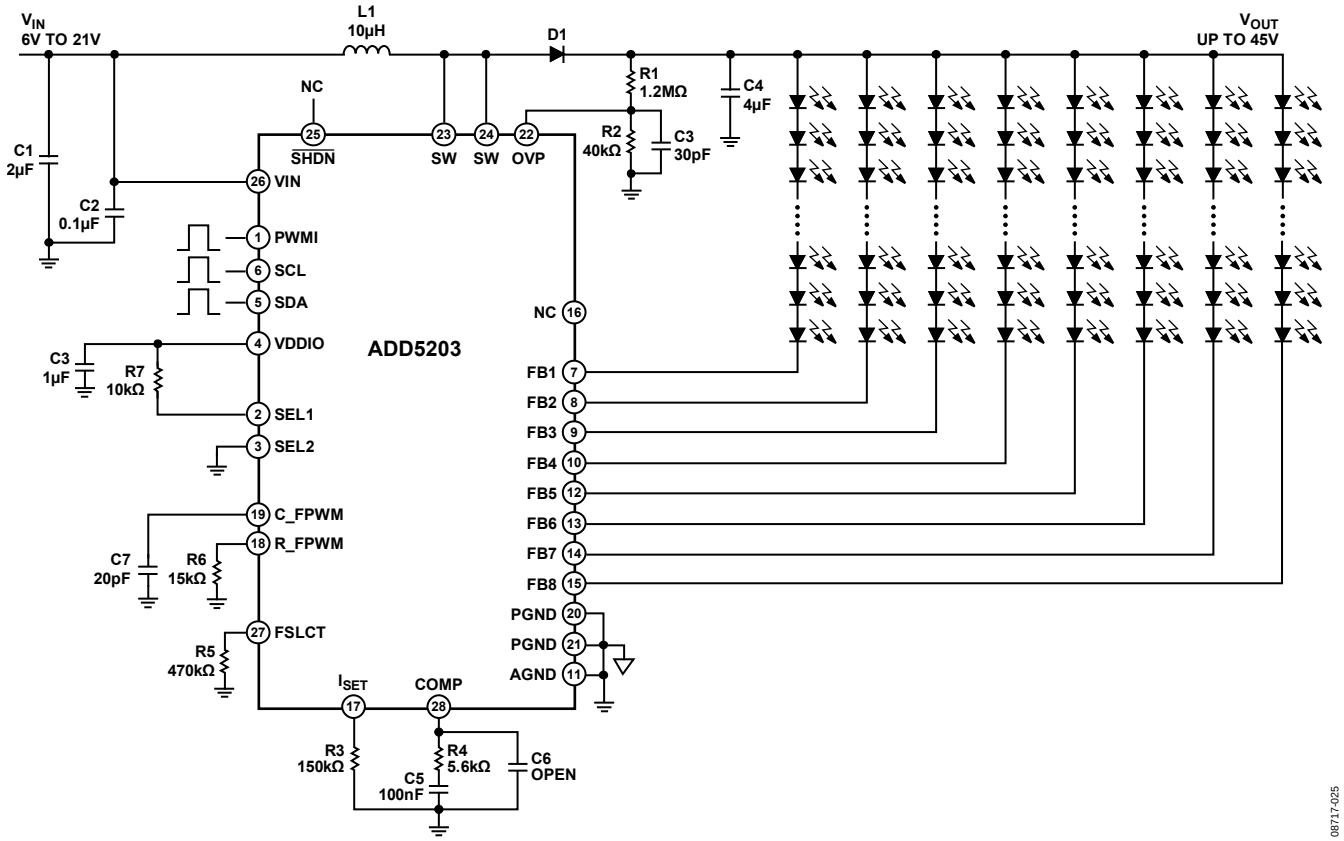


Figure 25. Typical Application Circuit for SMBus Interface with No Delay Dimming Mode

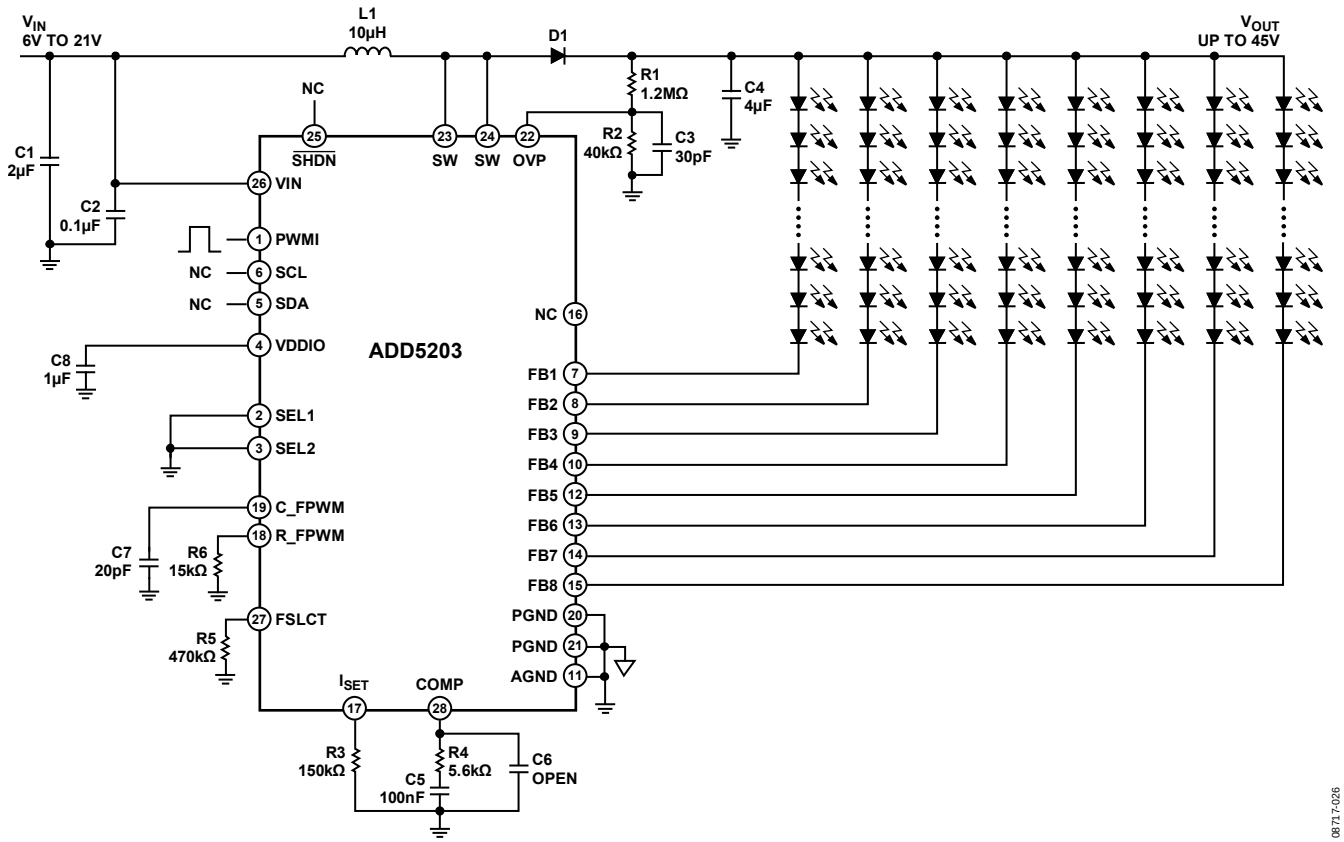


Figure 26. Typical Application Circuit for PWM Interface with DPWM Dimming Mode

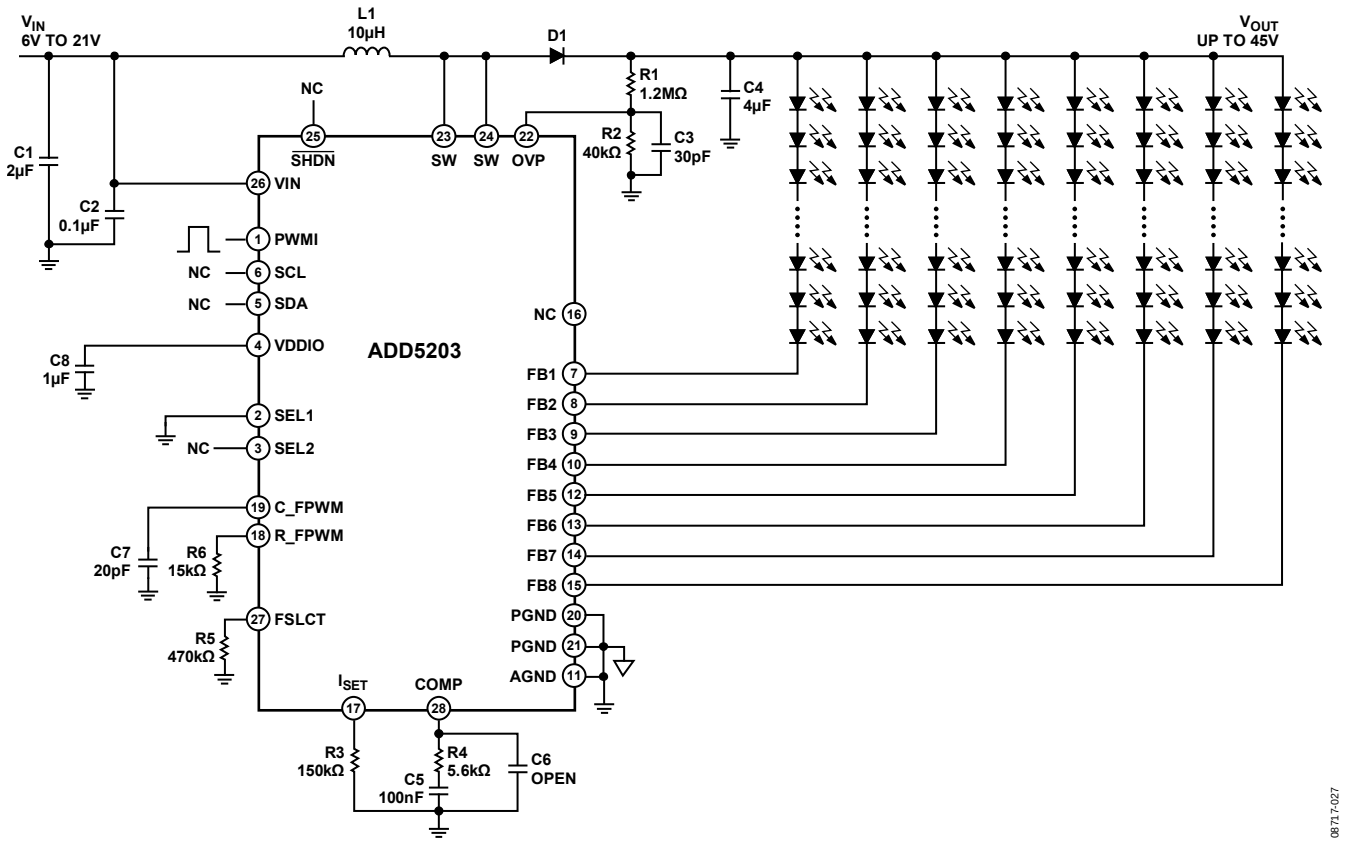
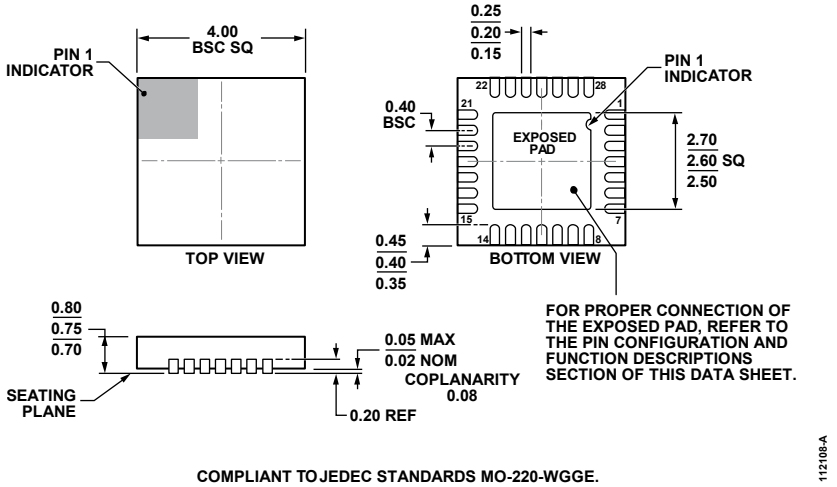


Figure 27. Typical Application Circuit for PWM Interface with DC Current Dimming Mode

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WGGE.

Figure 28. 28-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
4 mm × 4 mm × 0.75 mm Body, Very Very Thin Dual
(CP-28-5)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADD5203ACPZ-RL	−25°C to +85°C	28-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-28-5

[1] Z = RoHS Compliant Part.

NOTES

D08717-0-5/10(0)