IM69D130

High performance digital XENSIV^{TM} MEMS microphone

Description

The IM69D130 is designed for applications where low self-noise (high SNR), wide dynamic range, low distortions and a high acoustic overload point is required.

Infineon's Dual Backplate MEMS technology is based on a miniaturized symmetrical microphone design, similar as utilized in studio condenser microphones, and results in high linearity of the output signal within a dynamic range of 105dB. The microphone distortion does not exceed 1% even at sound pressure levels of 128dBSPL. The flat frequency response (28Hz low-frequency roll-off) and tight manufacturing tolerance result in close phase matching of the microphones, which is important for multi-microphone (array) applications.

With its low equivalent noise floor of 25dBSPL (SNR 69dB(A)) the microphone is no longer the limiting factor in the audio signal chain and enables higher performance of voice recognition algorithms.

The digital microphone ASIC contains an extremely low-noise preamplifier and a high-performance sigma-delta ADC. Different power modes can be selected in order to suit specific current consumption requirements.

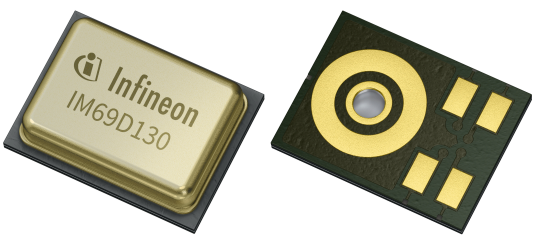
Each IM69D130 microphone is calibrated with an advanced Infineon calibration algorithm, resulting in small sensitivity tolerances (± 1dB). The phase response is tightly matched (± 2°) between microphones, in order to support beamforming applications.

Features

- Dynamic range of 105dB
  - Signal to noise ratio of 69dB(A) SNR
  - <1% total harmonic distortions up to 128dBSPL
  - Acoustic overload point at 130dBSPL
- Sensitivity (± 1dB) and phase (± 2° @1kHz) matched
- Flat frequency response with low frequency roll off at 28Hz
- Very fast analog to digital conversion speed (6µs latency @1kHz
- Power optimized modes determined by PDM clock frequency
- Package dimensions: 4mm x 3mm x 1.2mm
- PDM output
- Omnidirectional pickup pattern

Typical applications

- Devices with Voice User Interface (VUI)
  - Smart speakers
  - Home automation
  - IOT devices
- Active Noise Cancellation (ANC) headphones and earphones
- High quality audio capturing
  - Conference systems
  - Cameras and camcorders
- Industrial or home monitoring with audio pattern detection



Use cases

- Below 1% total harmonic distortion
  - Voice command during music from the loud speaker
  - Effective active noise cancellation even close to loud noise source
  - Recordings in a discotheque or at a rock concert
- High Signal to noise ratio
  - Far field audio signal pick-up
  - Low volume audio and whispered voice capturing
  - Microphone noise is no longer limiting the audio chain
- Sensitivity and phase matching
  - Full utilization of voice algorithms capability
  - Audio beam forming
  - High and precise attenuation of background noise
- Power optimized modes
  - Low current consumption for always on applications
  - Long operating time of battery powered devices

Block diagram

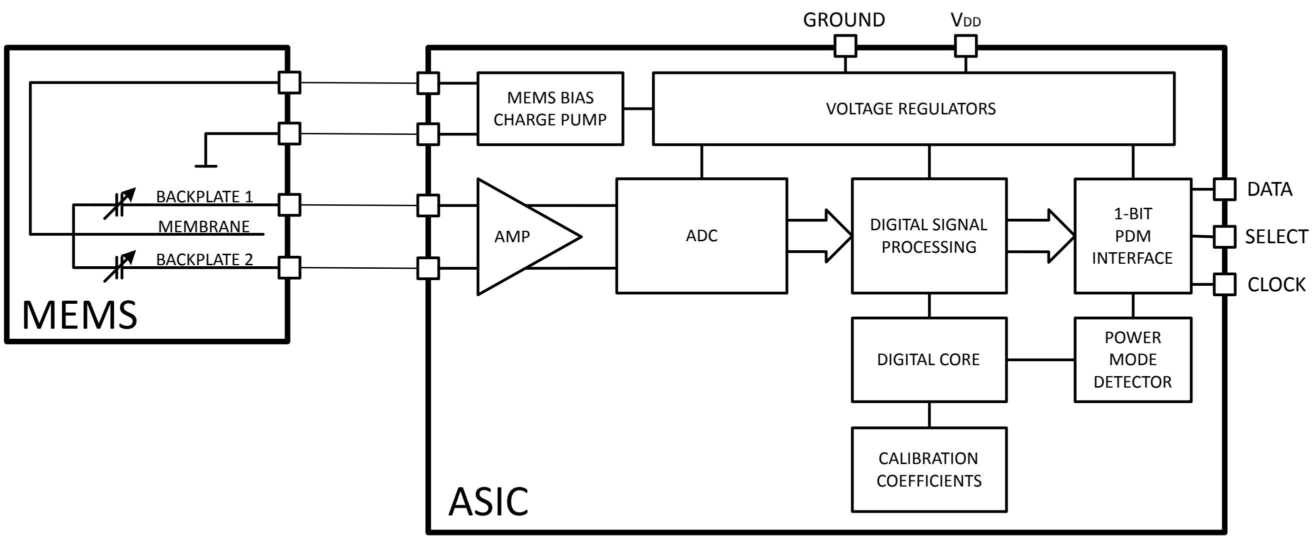


Figure 1 IM69D130 block diagram

Product validation

Technology qualified for industrial applications.

Ready for validation in industrial applications according to the relevant tests of IEC 60747 and 60749 or alternatively JEDEC47/20/22.

Table of contents

1 Typical performance characteristics

Test conditions: V_{DD} = 1.8V, f_{CLK} = 3.072MHz, no load on DATA

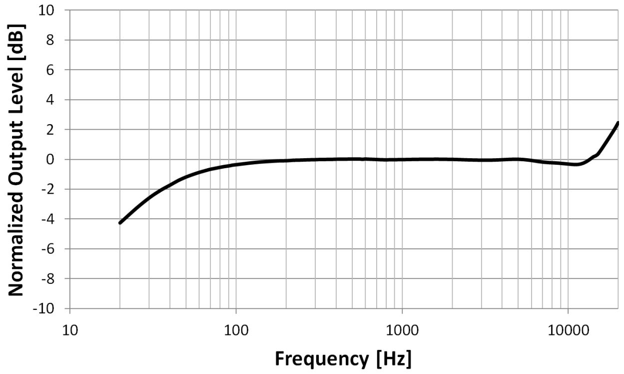


Figure 2 Typical freefield frequency response

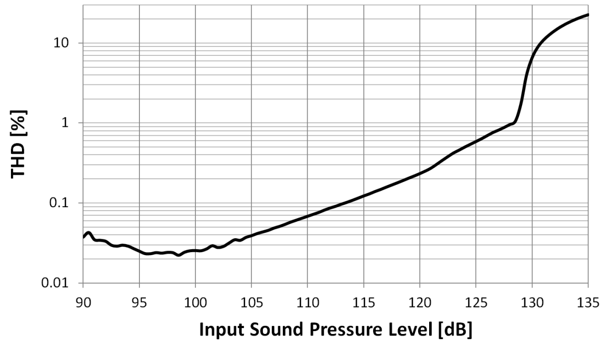


Figure 3 Typical THD vs SPL

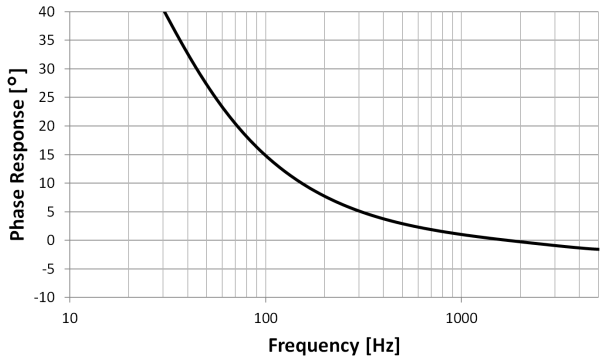


Figure 4 Typical phase response vs frequency

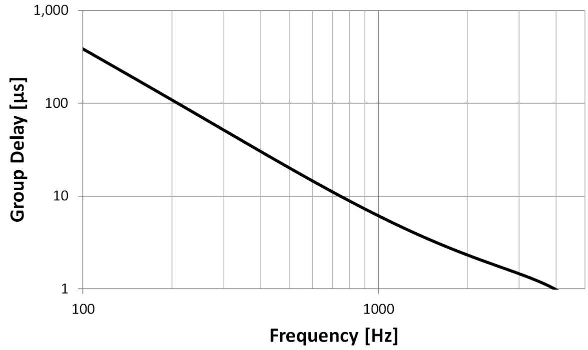


Figure 5 Typical group delay vs frequency

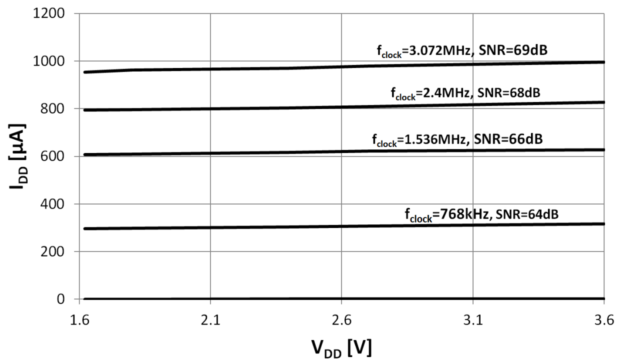


Figure 6 Typical I_{DD} vs V_{DD}

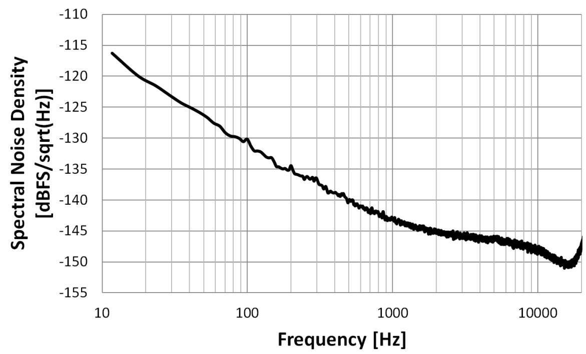


Figure 7 Typical noise floor (unweighted)

2 Acoustic characteristics

Test conditions (unless otherwise specified in the table): V_{DD} = 1.8V, f_{CLK} = 3.072MHz, T_A = 25°C, 55% R.H., audio bandwidth 20Hz to 20kHz, select pin grounded, no load on DATA, T_{edge} = 9ns

Table 1 IM69D130 acoustic specifications

Parameter		Symbol	Values			Unit	Note or Test condition
			Min.	Typ.	Max.		
Sensitivity			-37	-36	-35	dBFS	1kHz, 94 dBSPL, all operating modes
Acoustic Overload Point		AOP		130		dBSPL	THD = 10%, all operating modes
Signal to Noise Ratio	f_{clock}=3.072MHz	SNR		69		dB(A)	A-Weighted
	f_{clock}=2.4MHz			68			
	f_{clock}=1.536MHz			66			
	f_{clock}=768kHz			64			20Hz to 8kHz bandwidth, A-Weighted
Noise Floor	f_{clock}=3.072MHz			-105		dBFS(A)	A-Weighted
	f_{clock}=2.4MHz			-104			
	f_{clock}=1.536MHz			-102			
	f_{clock}=768kHz			-101			20Hz to 8kHz bandwidth, A-Weighted
Total Harmonic Distortion	94dBSPL	THD		0.5		%	Measuring 2nd to 5th harmonics; 1kHz, all operating modes
	128dBSPL			1.0			
	129dBSPL			2.0			
	130dBSPL			10.0			
Low Frequency Cutoff Point		$f_{C\ LP}$		28		Hz	-3dB point relative to 1kHz
Group Delay	250Hz			70		µs	
	600Hz			15			
	1kHz			6			
	4kHz			1			
Phase Response	75Hz			19		°	
	1kHz			2			
	3kHz			-1			
Directivity				Omnidirectional			Pickup pattern
Polarity				Positive pressure increases density of 1's, negative pressure decreases density of 1's in data output			

2.1 Free field frequency response

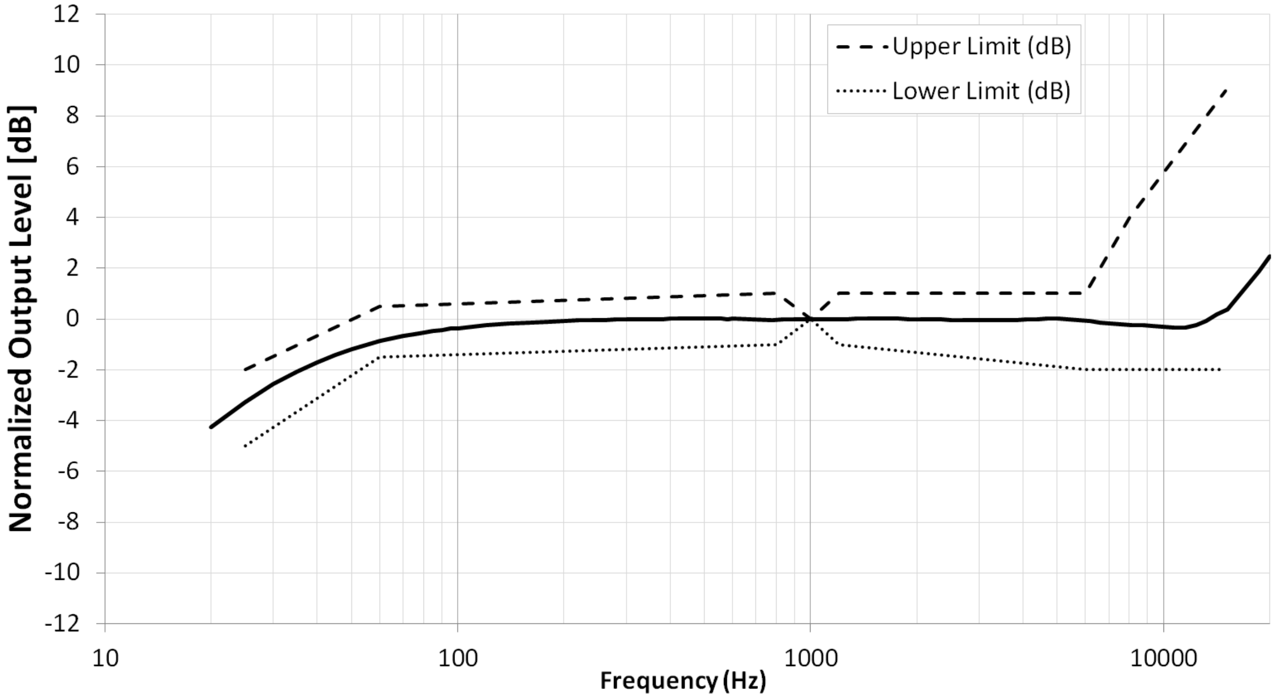


Figure 8 IM69D130 free field frequency response

Table 2 IM69D130 free field frequency response, normalized to 1kHz sensitivity value

Frequency (Hz)	Upper Limit (dB)	Lower Limit (dB)
25	-2	-5
60	+0.5	-1.5
800	+1	-1
1000	0	0
1200	+1	-1
6000	+1	-2
8000	+4	-2
15000	+9	-2

3 Electrical parameters and characteristics

3.1 Absolute maximum ratings

Stresses at or above the listed maximum ratings may affect device reliability or cause permanent device damage. Functional device operation at these conditions is not guaranteed.

Table 3 Absolute maximum ratings

Parameter	Symbol	Values		Unit	Note / Test Condition
		Min.	Max.		
Voltage on any Pin	V_{max}		4	V	
Storage Temperature	T_S	-40	125	°C	
Ambient Temperature	T_A	-40	70	°C	V_{DD}>3.0V
		-40	100	°C	

3.2 Electrical parameters

Table 4 Electrical parameters and digital interface input

Parameter		Symbol	Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Supply Voltage		V_{DD}	1.62		3.6	V	A 100nF bypass capacitor should be placed close to the microphone's VDD pin to ensure best SNR performance
Clock Frequency Range	Operating Modes	f_{clock}	2.9	3.072	3.3	MHz	
			2.1	2.4	2.65		
			1.05	1.536	1.9		
			400	768	950	kHz	
	Standby Mode				250		DATA = high-Z
V_{DD} Ramp-up Time					50	ms	Time until $V_{DD} \geq V_{DD\_min}$
PDM Clock Frequency		f_{clock}	0.4		3.3	MHz	
Clock Duty Cycle			40		60	%	f_{clock}<2.65MHz
			48		52	%	$f_{clock} \geq$2.9MHz
Clock Rise/Fall Time					13	ns	
Input Logic Low Level		V_{IL}	-0.3		0.35xV_{DD}	V	
Input Logic High Level		V_{IH}	0.65xV_{DD}		V_{DD}+0.3	V	
Output Load Capacitance on DATA		C_{load}			200	pF	

3.3 Electrical characteristics

Test conditions (unless otherwise specified in the table): V_{DD}= 1.8V, T_A=25°C, 55% R.H.

Table 5 General electrical characteristics

Parameter		Symbol	Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Current Consumption	f_{clock}=3.072MHz	I_{DD}		980	1300	µA	No load on DATA
	f_{clock}=2.4MHz			800	1050		
	f_{clock}=1.536MHz			620	800		
	f_{clock}=768kHz			300	380		
	Standby Mode	$I_{standby}$		25	50		
	Clock Off Mode	I_{clock_off}			1		CLOCK pulled low
Short Circuit Current			1		20	mA	Grounded DATA pin
Power Supply Rejection		PSR_{1k_NM}		-80		dBFS	100mV$_{pp}$ sine wave on V_{DD} swept from 200Hz to 20kHz
		PSR_{217_NM}		-86		dBFS(A)	100mV$_{rms}$, 217Hz square wave on V_{DD}. A-weighted
Startup Time	±0.5dB sensitivity accuracy				20	ms	Time to start up in all operating modes after V_{DD_min} and CLOCK have been applied
	±0.2dB sensitivity accuracy				50		
Mode Switch Time	±0.5dB sensitivity accuracy				20	ms	Time to switch between operating modes. V_{DD} remains on during the mode switch
	±0.2dB sensitivity accuracy				50		
Hysteresis Width		V_{hys}	0.1xV_{DD}		0.29xV_{DD}	V	
Output Logic Low Level		V_{OL}			0.3xV_{DD}	V	I_{out}= 2mA
Output Logic High Level		V_{OH}	0.7xV_{DD}				I_{out}= 2mA
Delay Time for DATA Driven		t_{DD}	40		80	ns	Delay time from CLOCK edge (0.5xV_{DD}) to DATA driven
Delay Time for DATA High-Z[1)]		t_{HZ}	5		30	ns	Delay time from CLOCK edge (0.5xV_{DD}) to DATA high impedance state

1 t_{hold} is depended on C_{load}

Table 5 General electrical characteristics (continued)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Delay Time for DATA Valid[2)]	t_{DV}			100	ns	Delay time from CLOCK edge ($0.5xV_{DD}$) to DATA valid ($<0.3xV_{DD}$ or $>0.7xV_{DD}$)

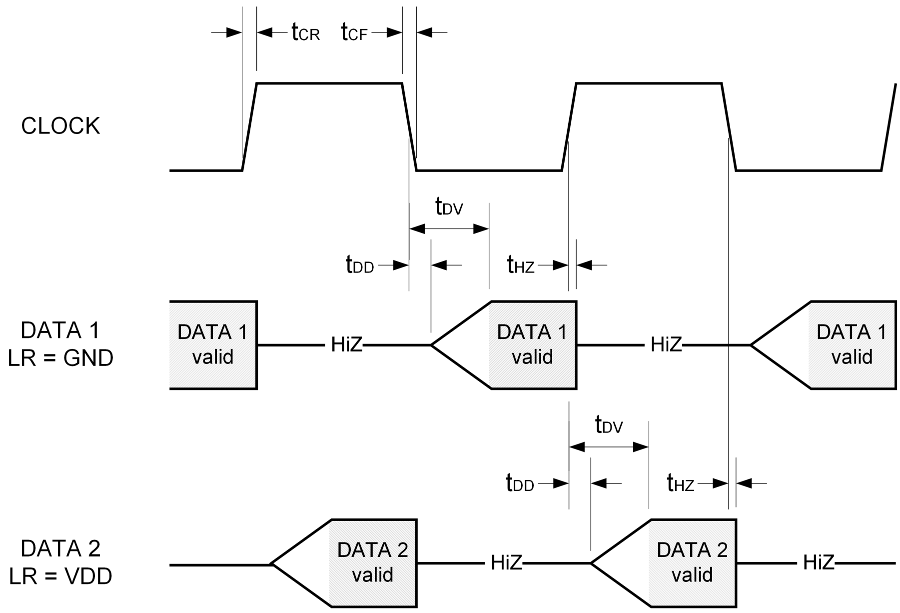


Figure 9 Timing diagram

2 Load on data: C_{load}=100pF, R_{load}=100kΩ

4 Typical stereo application circuit

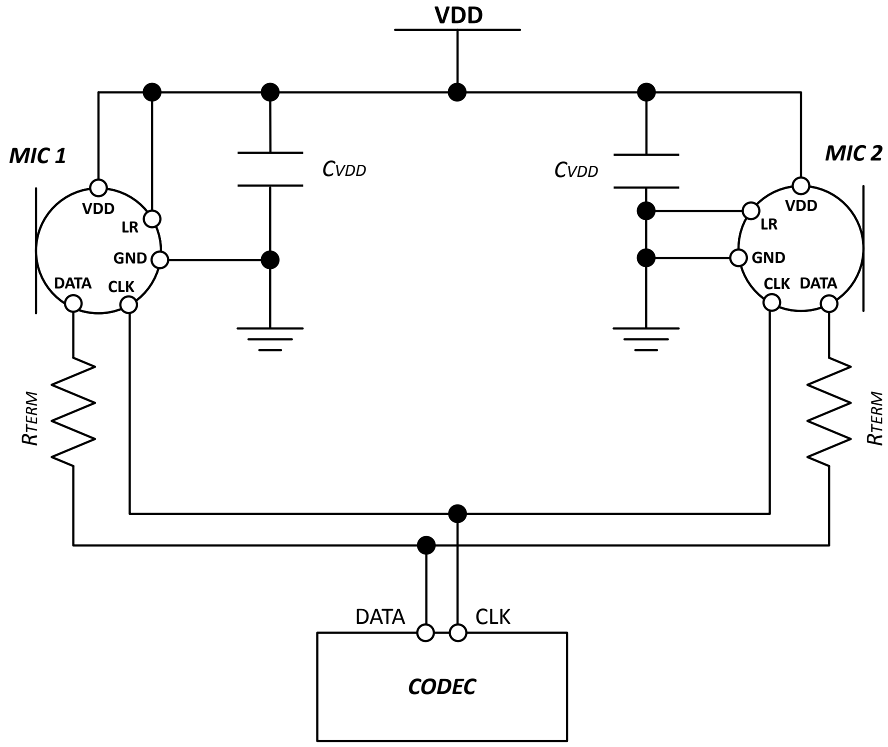


Figure 10 IM69D130 stereo mode configuration

Note: *For best performance it is strongly recommended to place a 100nF ($C_{VDD\_typical}$) capacitor between V_{DD} and ground. The capacitor should be placed as close to V_{DD} as possible. A termination resistor(R_{TERM}) of about 100Ω may be added to reduce the ringing and overshoot on the output signal.*

5 Reliability specifications

The microphone sensitivity after stress must deviate by no more than 3dB from the initial value.

Table 6 Reliability tests

Test	Test Condition	Standard
Vibration	20Hz to 2000Hz with a peak acceleration of 20g in X, Y, and Z for 4 minutes each, total 4 cycles	MIL-STD-883J
High Temperature Storage	T_a=+125°C, 1000 hours	JESD22 A-103E
Low Temperature Storage	T_a=-40°C, 1000 hours	JESD22-A119A
High Temperature Operation	T_a=+125°C, VDD=2.5V, 1000 hours	JESD22 A-108D
Cold Temperature Operation	T_a=-40°C, VDD=3.2V, 1000 hours	JESD22 A-108D
Temperature/Humidity Bias	T_a=+85°C, R.H = 85%, VDD=3.2V, 1000 hours	JESD22-A101D
Mechanical Shock	10000g/0.1msec direction ±x,y,z, 5 shocks in each direction, 30 shocks in total	IEC 60068-2-27
Thermal cycle	1000 cycles, -40°C to +125°C, 30 minutes per cycle	JESD22.A104E
Reflow Solder	3 reflow cycles, peak temperature = +260°C	IPC-JEDEC J-STD-020D-01
ESD-SLT	3 contact discharges of ±8kV to lid while V_{dd} and f_{clock} are supplied according to the operational modes; (V_{dd} and f_{clock} ground is separated from earth ground)	IEC-61000-4-2
ESD-HBM	1 pulse of ±2kV between all I/O pin combinations	JS001
Latch up	Trigger current from ±150mA	JESD 78E

6 Package information

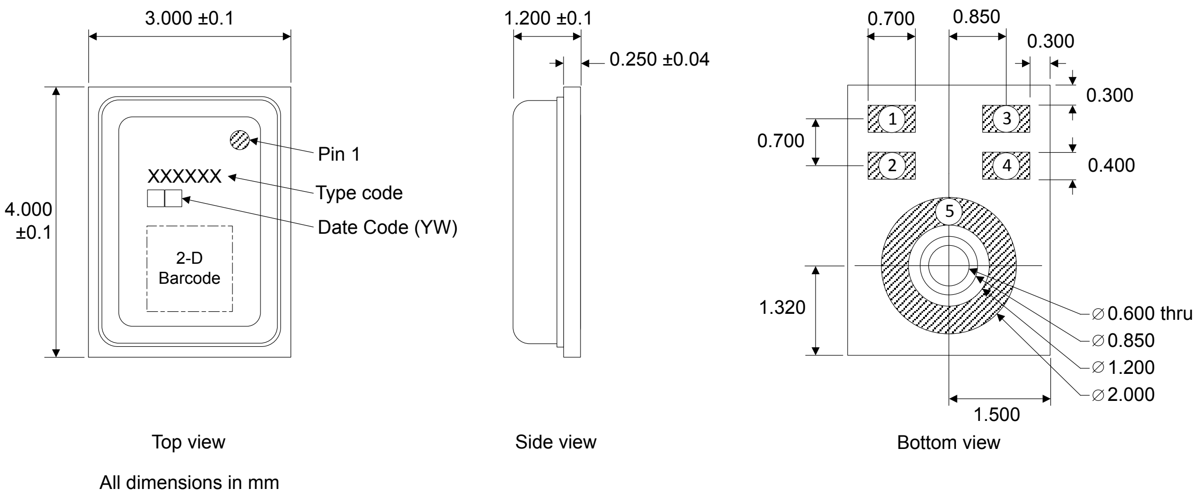


Figure 11 IM69D130 package drawing

Table 7 IM69D130 pin configuration

Pin Number	Name	Description
1	DATA	PDM data output
2	V_{DD}	Power supply
3	CLOCK	PDM clock input
4	SELECT	PDM left/right select
5	GND	Ground

7 Footprint and stencil recommendation

The acoustic port hole diameter in the PCB should be larger than the acoustic port hole diameter of the MEMS Microphone to ensure optimal performance. A PCB sound port size of radius 0.4 mm (diameter 0.8mm) is recommended.

The board pad and stencil aperture recommendations shown in ***Figure 12*** are based on Solder Mask Defined (SMD) pads. The specific design rules of the board manufacturer should be considered for individual design optimizations or adaptations.

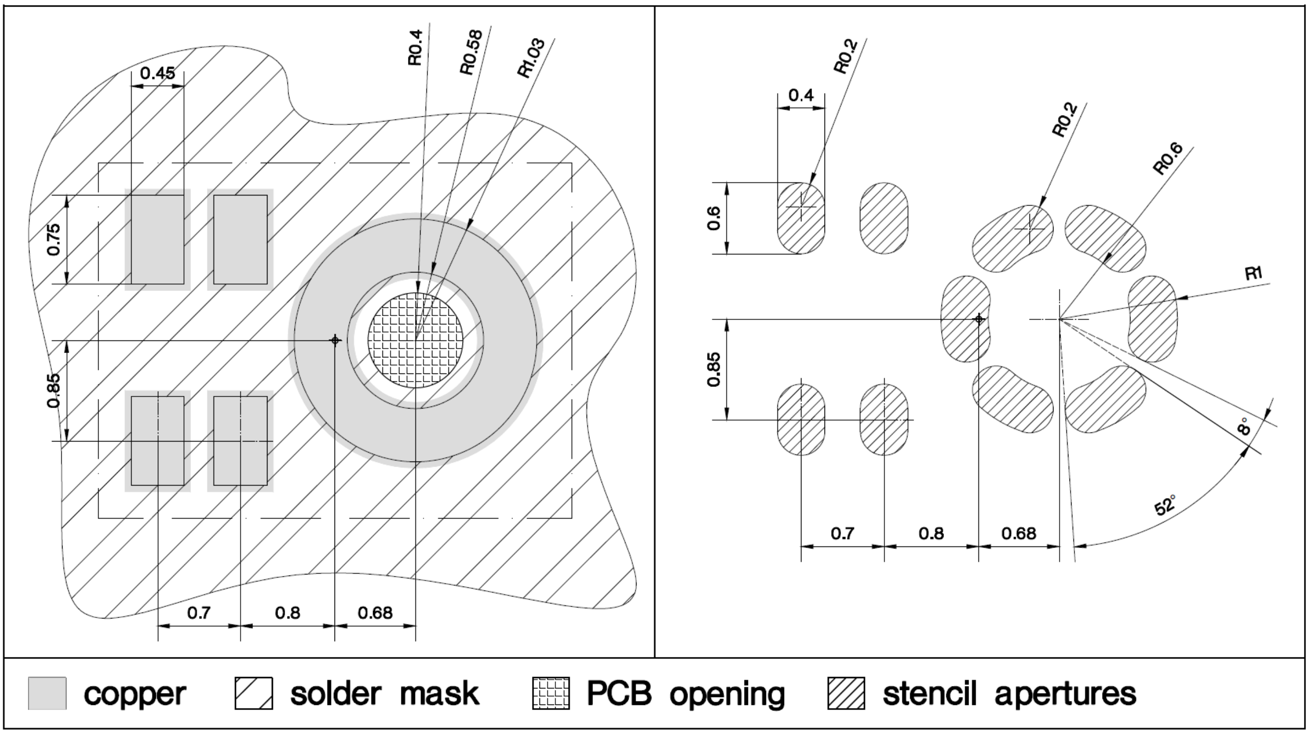


Figure 12 IM69D130 footprint and stencil recommendation

Note: *Dimensions are in millimeters unless otherwise specified*

8 Packing

For shipping and assembly the Infineon microphones are packed in product specific tape-and-reel carriers. A detailed drawing of the carrier can be seen in ***Figure 13***

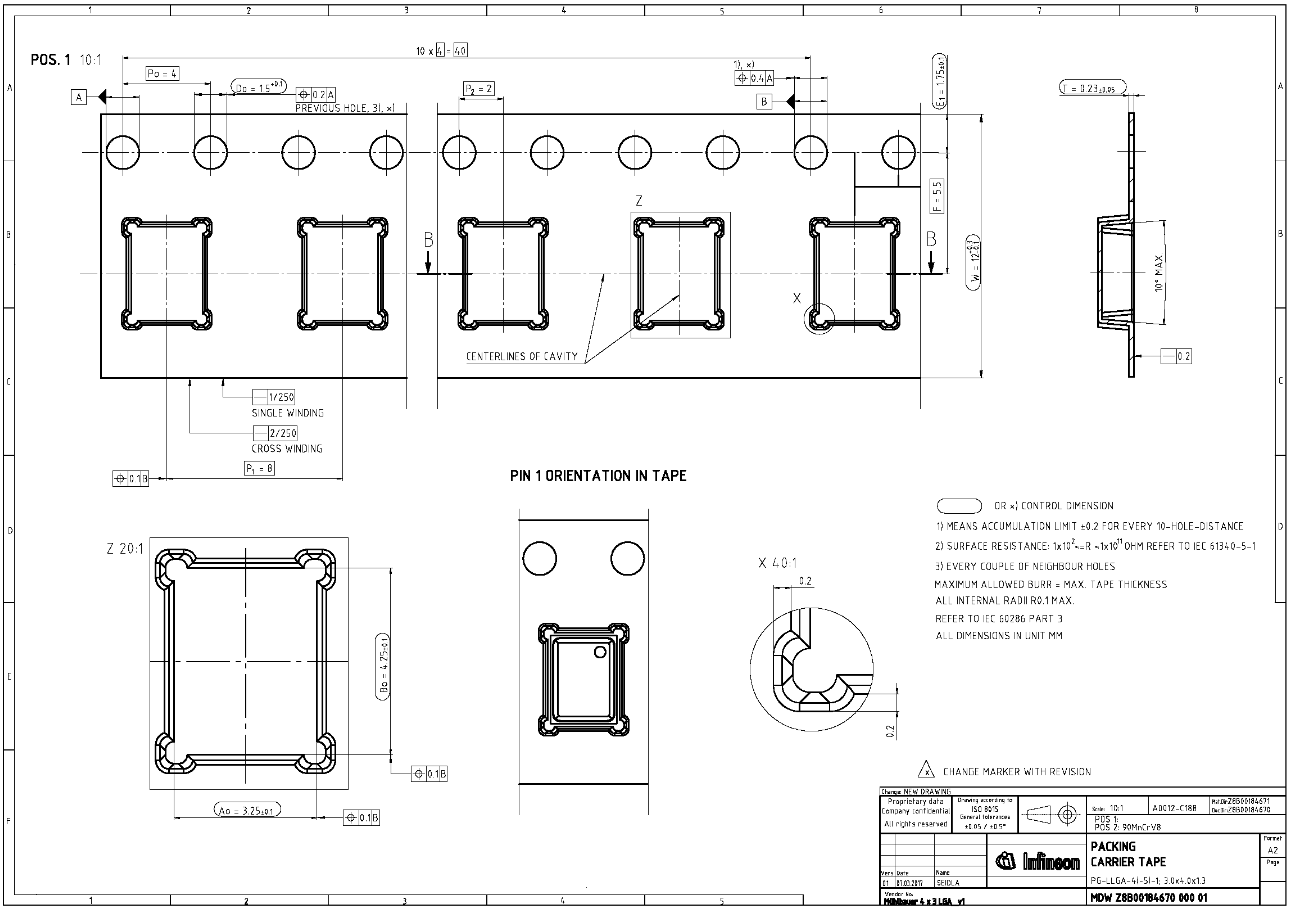


Figure 13 IM69D130 tape dimensions

Note: *For further information about Packing, please confer the Packing document which is available on the Infineon Technologies web page or contact your local sales, application, or quality engineer.*

Revision history

Major changes since previous revision

Document version	Date of release	Description of changes
1.0	19.12.2017	Initial Datasheet

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