TLV840-Q1 Nano-Power Voltage Supervisor with Adjustable Reset Time Delay

1 Features

Qualified for automotive applications:

- AEC-Q100 qualified with the following results:
  - Device temperature grade 1: –40°C to +125°C ambient operating temperature
  - Device HBM ESD classification level 2
  - Device CDM ESD classification level C7B

Designed for high performance:

- Nano supply current : 120 nA (Typ)
- High accuracy: ±0.5% (Typ)
- Built-in hysteresis (V_{HYS}): 5% (Typ)
- Fixed threshold voltage (V_{IT-}): 0.8 V to 5.4 V

Designed for a wide range of applications:

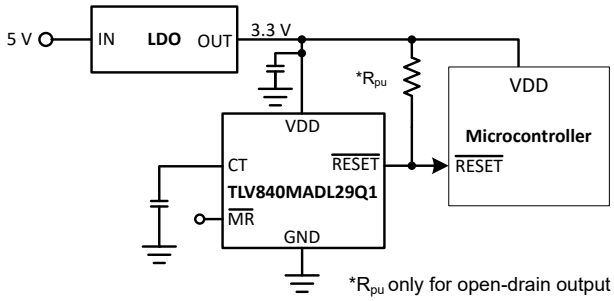
- Operating voltage range : 0.7 V to 6 V
- Fixed (V_{IT-}) voltage: 0.8 V to 5.4 V in 0.1 V steps
- Programmable reset time delay (t_D)
  - Min time delay: 40 µs (typ) without capacitor
- Active-low manual reset ($\overline{MR}$)

Multiple output topologies / Package type:

- Four output topologies ($\overline{RESET}$ / RESET):
  - TLV840MADL-Q1: open-drain, active-low
  - TLV840MAPL-Q1: push-pull, active-low
  - TLV840MADH-Q1: open-drain, active-high
  - TLV840MAPH-Q1: push-pull, active-high
- Package: SOT23-5 (DBV)

2 Applications

- Surround view system, front camera
- Automotive gateway
- Radar ECU
- Automotive head unit
- ADAS controller
- Emergency call
- Telematics control unit



Typical Application Circuit

3 Description

The TLV840-Q1 device is a voltage supervisor or reset IC that can operate at wide input voltage levels from 0.7 V to 6 V while maintaining very low quiescent current across the whole VDD and temperature range. TLV840-Q1 offers the best combination of low power consumption, high accuracy and low propagation delay (t_{p_HL}= 30 µs typical).

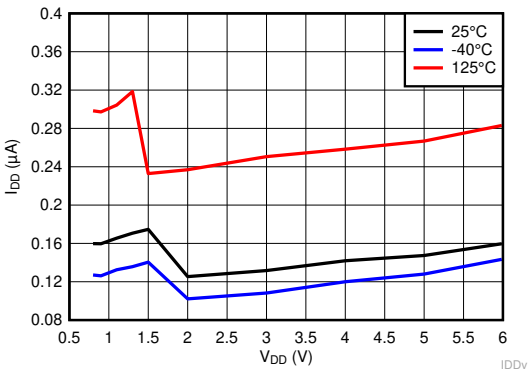
Reset output signal is asserted when the voltage at VDD drops below the negative voltage threshold (V_{IT-}). Reset signal is cleared when VDD rise above V_{IT-} plus hysteresis (V_{HYS}) and the reset time delay (t_D) expires. Reset time delay can be programmed by connecting a capacitor between the CT pin and ground. For a minimum reset delay time the CT pin can be left floating. The TLV840-Q1, with its manual reset pin ($\overline{MR}$), offers program flexibility by forcing the system into a hard reset when the pin is asserted.

Additional features: Low power-on reset voltage (V_{POR}), built-in glitch immunity protection for VDD, built-in hysteresis, low open-drain output leakage current ($I_{lkg(OD)}$). TLV840-Q1 is a perfect voltage monitoring solution for automotive applications and battery-powered / low-power applications.

Device Information

PART NUMBER	PACKAGE (1)	BODY SIZE (NOM)
TLV840-Q1	SOT-23 (5) (DBV)	2.90 mm × 1.60 mm

(1) For package details, see the mechanical drawing addendum at the end of the data sheet.



Typical Supply Current

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4 Revision History

Changes from Revision * (November 2020) to Revision A (April 2021)	Page
• RTM release	1

5 Device Comparison

Figure 5-1 shows the device naming nomenclature to compare the different device variants. See Section 12.1 for a more detailed explanation.

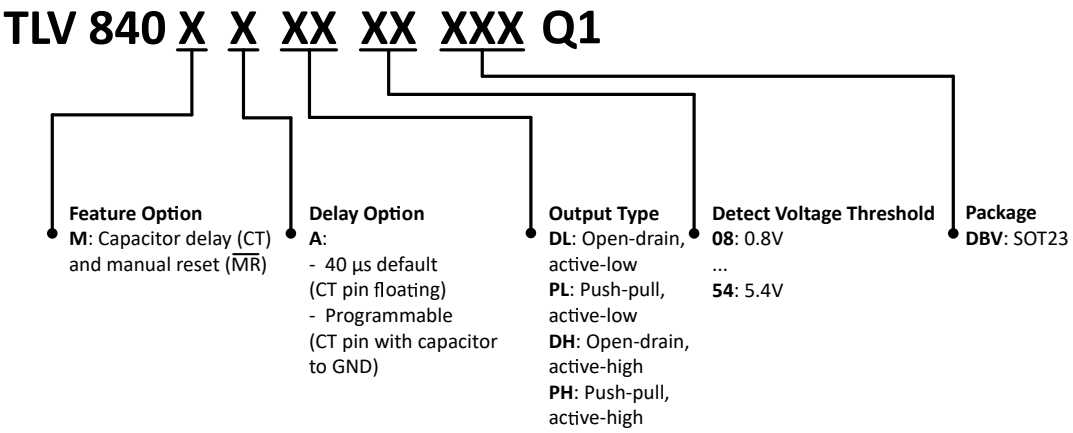


Figure 5-1. Device Naming Nomenclature

6 Pin Configuration and Functions

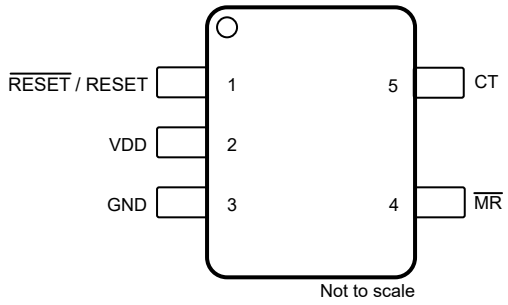


Figure 6-1. Pin Configuration TLV840M-Q1
DBV Package 5-Pin SOT-23
TLV840M-Q1 Top View

Table 6-1. Pin Functions

PIN			I/O	DESCRIPTION
PIN NO.	TLV840MAxL-Q1	TLV840MAxH-Q1		
1	$\overline{\text{RESET}}$	N/A	O	**Active-Low Output Reset Signal:** This pin is driven logic low when VDD voltage falls below the negative voltage threshold (V_{IT-}). $\overline{\text{RESET}}$ remains low (asserted) for the delay time period (t_D) after VDD voltage rises above $V_{IT+} = V_{IT-}+V_{HYS}$.
1	N/A	RESET	O	**Active-High Output Reset Signal:** This pin is driven logic high when VDD voltage falls below the negative voltage threshold (V_{IT-}). RESET remains high (asserted) for the delay time period (t_D) after VDD voltage rises above $V_{IT+} = V_{IT-}+V_{HYS}$.
2	VDD	VDD	I	**Input Supply Voltage:** TLV840-Q1 monitors VDD voltage
3	GND	GND	_	**Ground**
4	$\overline{\text{MR}}$	$\overline{\text{MR}}$	I	**Manual Reset:** Pull this pin to a logic low to assert a reset signal in the $\overline{\text{RESET}}$ output pin. After $\overline{\text{MR}}$ pin is left floating or pulls to logic high, the $\overline{\text{RESET}}$ output deasserts to the nominal state after the reset delay time (t_D) expires.
5	CT	CT	-	**Capacitor Time Delay Pin:** The CT pin offers a user-programmable delay time. Connect an external capacitor on this pin to adjust time delay. When not in use leave pin floating for the smallest fixed time delay.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range, unless otherwise noted(1)

		MIN	MAX	UNIT
Voltage	VDD	–0.3	6.5	V
Voltage	CT, $\overline{MR}$ (2), $\overline{RESET}$ (TLV840MAPL), RESET (TLV840MAPH)	–0.3	V_{DD}+0.3 (3)	V
	$\overline{RESET}$ (TLV840MADL)	–0.3	6.5	
Current	$\overline{RESET}$, RESET pin	–20	20	mA
Temperature (4)	Operating ambient temperature, T_A	–40	125	℃
Temperature (4)	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) If the logic signal driving $\overline{MR}$ is less than VDD, then I_{DD} current increases based on voltage differential.

(3) The absolute maximum rating is (VDD + 0.3) V or 6.5 V, whichever is smaller

(4) As a result of the low dissipated power in this device, it is assumed that $T_J = T_A$.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged device model (CDM), per AEC Q100-011	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Voltage	VDD (TLV840MAxL)	0.7		6	V
	CT, $\overline{RESET}$ (TLV840MAxL), RESET (TLV840MAPH) , $\overline{MR}$	0		6	
Current	$\overline{RESET}$ and RESET pin current	–5		5	mA
T_A	Operating ambient temperature	–40		125	℃

7.4 Thermal Information

THERMAL METRIC(1)		TLV840-Q1 DBV (SOT23-5) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	193.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	117.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	98.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	43.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	97.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

At 0.7 V ≤ V_{DD} ≤ 6 V, CT = $\overline{MR}$ = Open, $\overline{RESET}$ pull-up resistor ($R_{pull-up}$) = 100 kΩ to VDD, output reset load (C_{LOAD}) = 10 pF and over operating free-air temperature range –40°C to 125°C, unless otherwise noted. VDD ramp rate ≤ 100 mV/µs. Typical values are at T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
COMMON PARAMETERS						
V_{DD}	Input supply voltage	TLV840MAxL	0.7		6	V
$V_{IT–}$	Negative-going input threshold accuracy (1)	V_{IT-} = 0.8 V to 1.7 V	–2.5	±0.5	2.5	%
		V_{IT-} = 1.8 V to 5.4 V	–2	±0.5	2	
V_{HYS}	Hysteresis on $V_{IT–}$ pin		2.5	5	7	%
I_{DD}	Supply current into VDD pin (2)	V_{DD} = 2 V; $V_{IT–}$ = 0.8 V to 1.8 V		0.12	1.0	µA
		V_{DD} = 6 V; $V_{IT–}$ = 0.8 V to 5.4 V		0.15	1.2	
$V_{\overline{MR}\_L}$	Manual reset logic low input (2)				0.3V_{DD}	V
$V_{\overline{MR}\_H}$	Manual reset logic high input (2)		0.7V_{DD}			V
$R_{\overline{MR}}$	Manual reset internal pull-up resistance			100		kΩ
R_{CT}	CT pin internal resistance			500		kΩ
TLV840MADL (Open-drain active-low)						
V_{POR}	Power on Reset Voltage (3)	$V_{OL(max)}$ = 300 mV $I_{OUT(Sink)}$ = 15 µA			700	mV
V_{OL}	Low level output voltage	V_{DD} = 0.7 V, 0.8 V ≤ $V_{IT–}$ ≤ 1.5 V $I_{OUT(Sink)}$ = 15 µA			300	mV
		V_{DD} =1.5 V, 1.6 V ≤ $V_{IT–}$ ≤ 3.3 V $I_{OUT(Sink)}$ = 500 µA			300	
		V_{DD} = 3.3 V, 3.4 V ≤ $V_{IT–}$ ≤ 5.5 V $I_{OUT(Sink)}$ = 2 mA			300	
$I_{lkg(OD)}$	Open-Drain output leakage current	V_{DD} = V_{PULLUP} = 6V T_A = –40°C to 85°C		10	100	nA
		V_{DD} = V_{PULLUP} = 6V		10	350	nA
TLV840MAPL (Push-pull active-low)						
V_{POR}	Power on Reset Voltage (3)	$V_{OL(max)}$ = 300 mV $I_{OUT(Sink)}$ = 15 µA			700	mV
V_{OL}	Low level output voltage	V_{DD} = 0.7 V, 0.8 V ≤ $V_{IT–}$ ≤ 1.5 V $I_{OUT(Sink)}$ = 15 µA			300	mV
		V_{DD} = 1.5 V, 1.6 V ≤ $V_{IT–}$ ≤ 3.3 V $I_{OUT(Sink)}$ = 500 µA			300	
		V_{DD} = 3.3 V, 3.4 V ≤ $V_{IT–}$ ≤ 5.5 V $I_{OUT(Sink)}$ = 2 mA			300	
V_{OH}	High level output voltage	V_{DD} = 1.8 V, 0.8 V ≤ $V_{IT–}$ ≤ 1.4 V $I_{OUT(Source)}$ = 500 µA	0.8V_{DD}			V
		V_{DD} = 3.3 V, 1.5 V ≤ $V_{IT–}$ ≤ 3.0 V $I_{OUT(Source)}$ = 500 µA	0.8V_{DD}			
		V_{DD} = 6 V, 3.1 V ≤ $V_{IT–}$ ≤ 5.5 V $I_{OUT(Source)}$ = 2 mA	0.8V_{DD}			

7.5 Electrical Characteristics (continued)

At 0.7 V ≤ V_{DD} ≤ 6 V, CT = $\overline{MR}$ = Open, $\overline{RESET}$ pull-up resistor ($R_{pull-up}$) = 100 kΩ to VDD, output reset load (C_{LOAD}) = 10 pF and over operating free-air temperature range –40°C to 125°C, unless otherwise noted. VDD ramp rate ≤ 100 mV/µs. Typical values are at T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TLV840MAPH (Push-pull active-high)						
V_{POR}	Power on Reset Voltage (3)	$V_{OH(min)}$ = 0.8V_{DD} V $I_{OUT\ (Source)}$ = 15 uA			900	mV
V_{OL}	Low level output voltage	VDD=3.3 V 0.8 V ≤ V_{IT-} ≤ 3.0 V $I_{OUT(Sink)}$ = 500 µA			300	mV
		VDD=6 V 3.1 V ≤ V_{IT-} ≤ 5.5 V $I_{OUT(Sink)}$ = 2 mA			300	mV
V_{OH}	High level output voltage	VDD = 0.9 V 1 V ≤ V_{IT-} ≤ 1.5 V $I_{OUT(Sink)}$ = 15 µA	0.8V_{DD}			V
		VDD=1.5 V 1.6 V ≤ V_{IT-} ≤ 3.3 V $I_{OUT(Sink)}$ = 500 µA	0.8V_{DD}			V
		VDD=3.3 V 3.4 V ≤ V_{IT-} ≤ 5.5 V $I_{OUT(Sink)}$ = 2 mA	0.8V_{DD}			V

(1) V_{IT-} threshold voltage range from 0.8 V to 5.4 V (for DL, PL versions) in 100 mV steps

(2) If the logic signal driving $\overline{MR}$ is less than VDD, then I_{DD} current increases based on voltage differential

(3) V_{POR} is the minimum V_{DD} voltage level for a controlled output state

7.6 Timing Requirements

At 0.7 V ≤ V_{DD} ≤ 6 V, CT = $\overline{MR}$ = Open, $\overline{RESET}$ pull-up resistor ($R_{pull-up}$) = 100 kΩ to VDD, output reset load (C_{LOAD}) = 10 pF and over operating free-air temperature range –40°C to 125°C, unless otherwise noted. VDD ramp rate ≤ 100 mV/µs. Typical values are at T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{P_HL}	Propagation detect delay for VDD falling below V_{IT-}	V_{DD} : (V_{IT+} + 10%) to (V_{IT-} – 10%) (1)		30	50	µs
t_D	Reset time delay	CT pin = Open or NC (V_{IT-} - 10%) to (V_{IT+} + 10%)		40	80	µs
		CT pin = 10 nF		6.2		ms
		CT pin = 1 µF		619		ms
t_{GI_VIT-}	Glitch immunity V_{IT-}	5% V_{IT-} overdrive(2)		10		µs
t_{STRT}	Startup Delay (3)	CT pin = Open or NC			300	µs
$t_{\overline{MR}\_PW}$	$\overline{MR}$ pin pulse duration to assert reset (4)			500		ns
$t_{\overline{MR}\_RES}$	Propagation delay from $\overline{MR}$ low to reset assertion	V_{DD} = 3.3 V, $\overline{MR}$ = $V_{\overline{MR}\_H}$ to $V_{\overline{MR}\_L}$		1		µs
$t_{\overline{MR}\_tD}$	Delay from $\overline{MR}$ release to reset deassert	V_{DD} = 3.3 V, $\overline{MR}$ = $V_{\overline{MR}\_L}$ to $V_{\overline{MR}\_H}$		t_D		ms

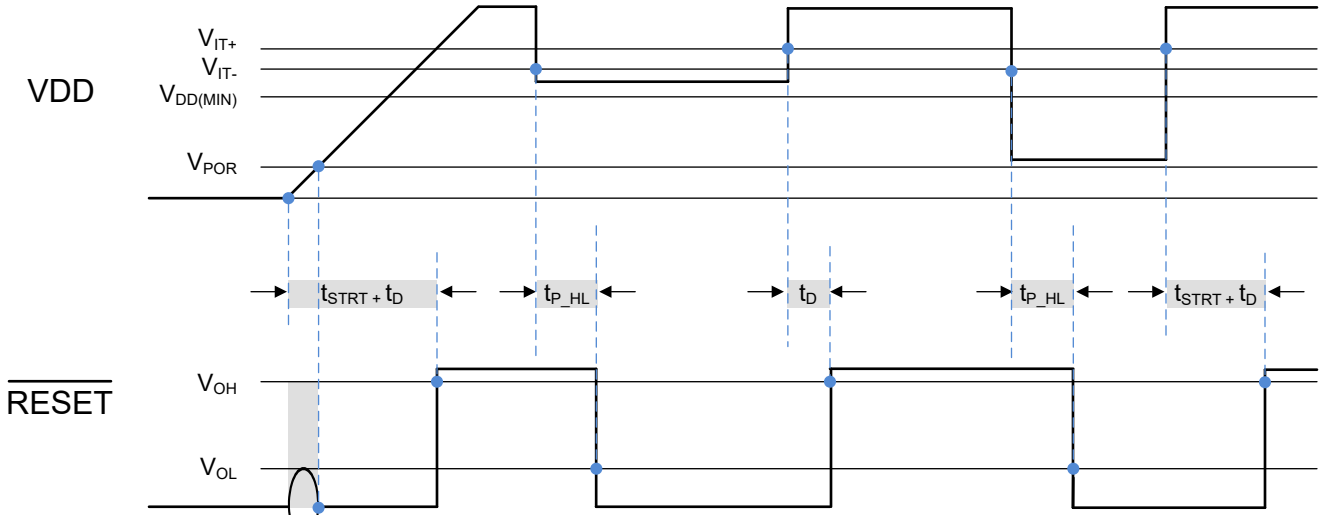
(1) t_{P_HL} measured from threshold trip point (V_{IT-}) to RESET assert. V_{IT+} = V_{IT-} + V_{HYS}

(2) Overdrive % = [(V_{DD}/ V_{IT-}) – 1] × 100%

(3) When VDD starts from less than the specified minimum V_{DD} and then exceeds V_{IT-}, reset is release after the startup delay (t_{STRT}), a capacitor at CT pin will add t_D delay to t_{STRT} time

(4) Refer section on Manual Reset Input for min pulse width needed on $\overline{MR}$ pin

7.7 Timing Diagrams

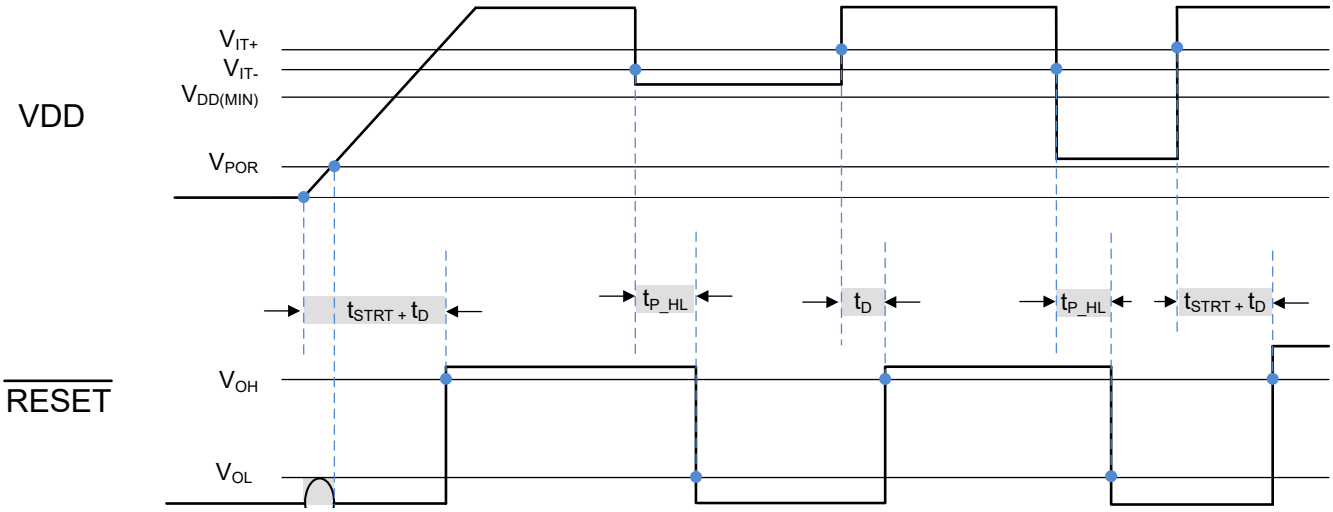


(1) $t_{D\ (no\ cap)}$ is included in t_{STRT} time delay. If t_D delay is programmed by an external capacitor connected to CT pin then t_D programmed time will be added to the startup time, VDD slew rate = 100 mV / µs.

(2) Open-Drain timing diagram where $\overline{RESET}$ is pulled up to VDD via an external pull-up resistor

(3) $\overline{RESET}$ output is undefined when V_{DD} is < V_{POR}

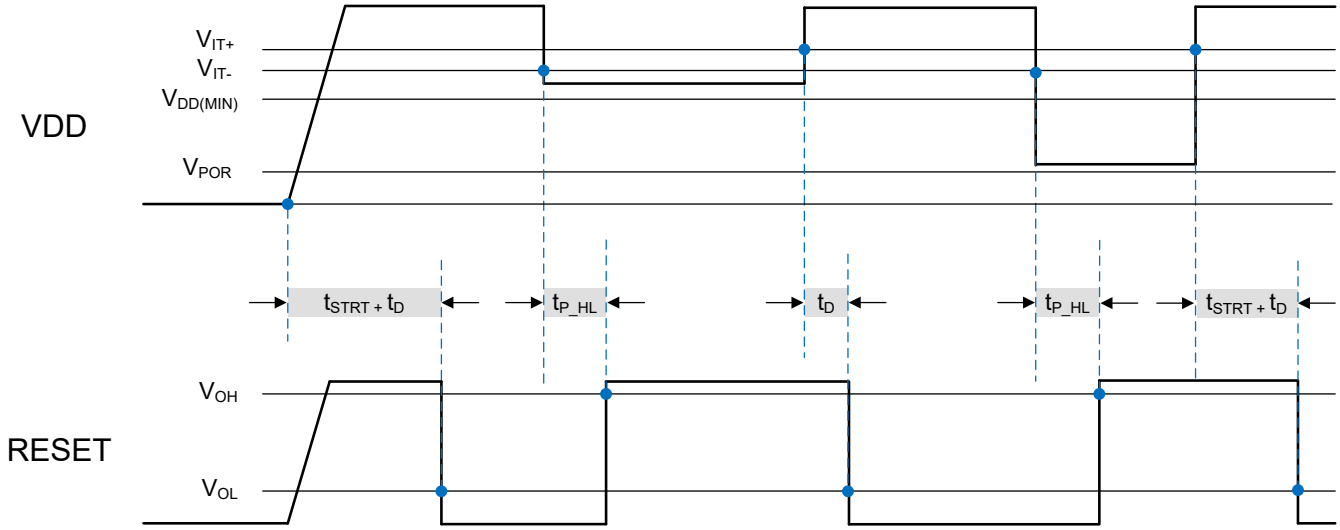
Figure 7-1. Timing Diagram TLV840MADL-Q1 (Open-Drain Active-Low)



(4) $t_{D\ (no\ cap)}$ is included in t_{STRT} time delay. If t_D delay is programmed by an external capacitor connected to CT pin then t_D programmed time will be added to the startup time, VDD slew rate = 100 mV / µs.

(5) $\overline{RESET}$ output is undefined when V_{DD} is < V_{POR} and limited to V_{OL} for V_{DD} slew rate = 100 mV / µS

Figure 7-2. Timing Diagram TLV840MAPL-Q1 (Push-Pull Active-Low)



(6) $t_{D\ (no\ cap)}$ is included in t_{STRT} time delay. If t_D delay is programmed by an external capacitor connected to CT pin then t_D programmed time will be added to the startup time, VDD slew rate = 100 mV / µs.

Figure 7-3. Timing Diagram TLV840MAPH-Q1 (Push-Pull Active-High)

7.8 Typical Characteristics

Typical characteristics show the typical performance of the TLV840-Q1 device. Test conditions are T_A = 25°C, VDD = 3.3 V, $R_{Pull-Up}$ = 100 kΩ, C_{LOAD} = 50 pF, unless otherwise noted.

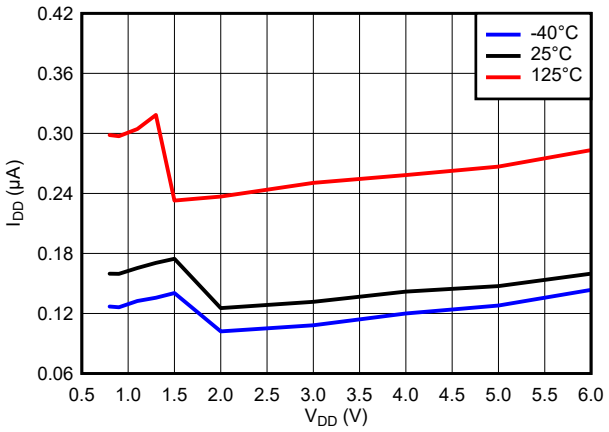


Figure 7-4. Supply Current vs Supply Voltage

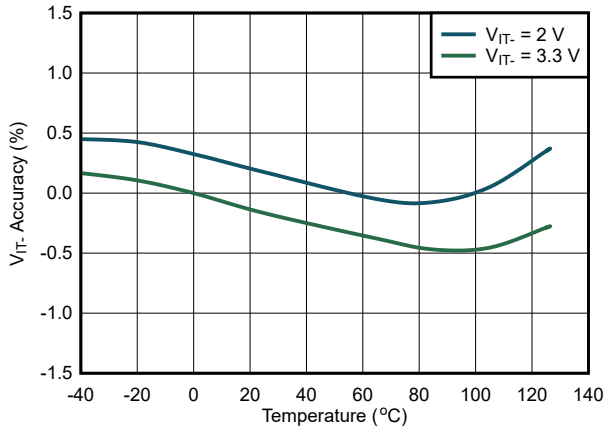


Figure 7-5. V_{IT-} Accuracy vs Temperature

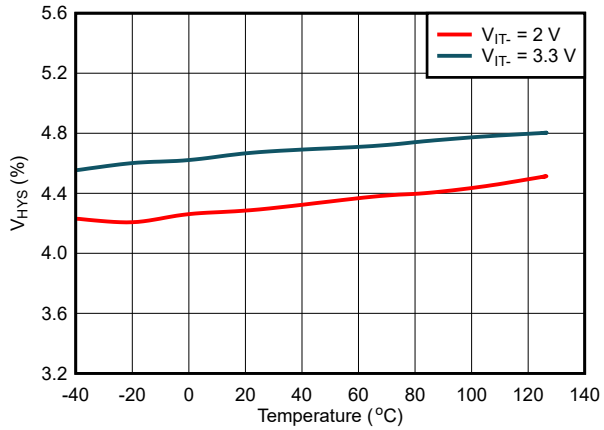


Figure 7-6. V_{HYS} vs Temperature

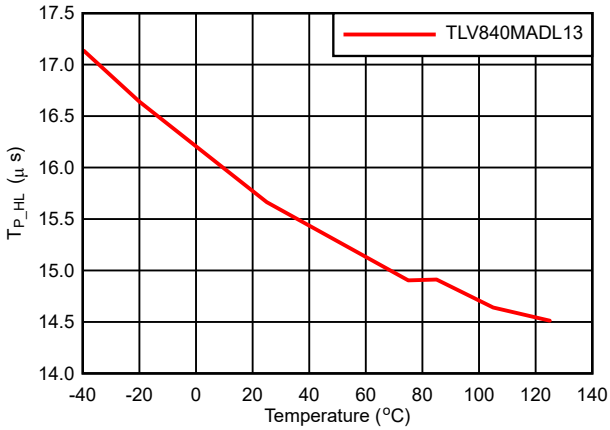


Figure 7-7. Propagation Delay vs Temperature

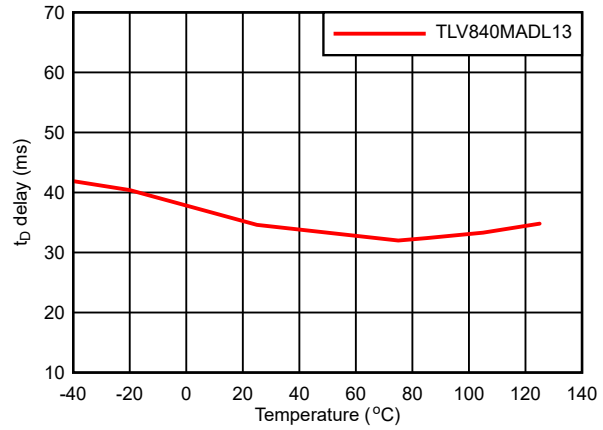


Figure 7-8. Reset Time Delay vs Temperature

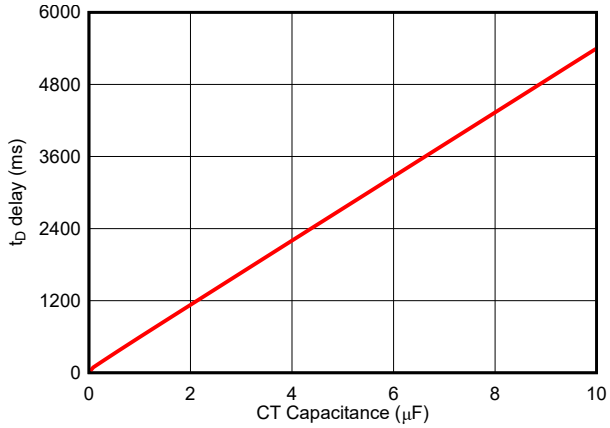


Figure 7-9. Reset Time Delay vs CT Capacitance

7.8 Typical Characteristics (continued)

Typical characteristics show the typical performance of the TLV840-Q1 device. Test conditions are T_A = 25°C, VDD = 3.3 V, $R_{Pull-Up}$ = 100 kΩ, C_{LOAD} = 50 pF, unless otherwise noted.

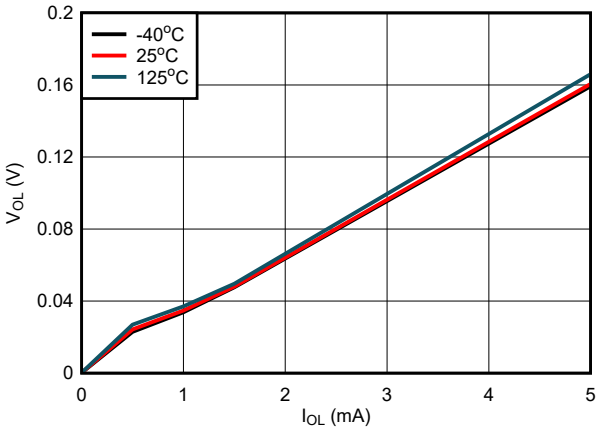


Figure 7-10. V_{OL} vs I_{OL}

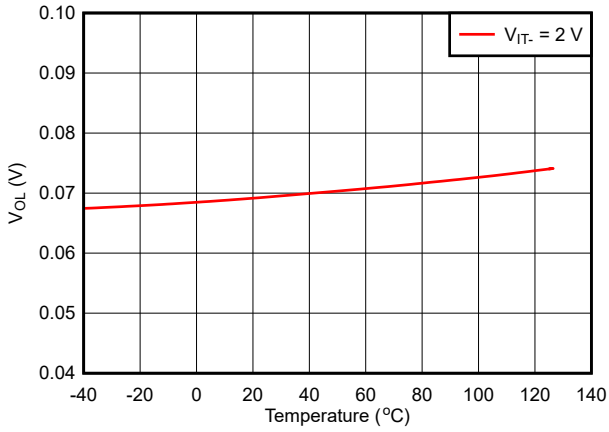


Figure 7-11. V_{OL} vs Temperature

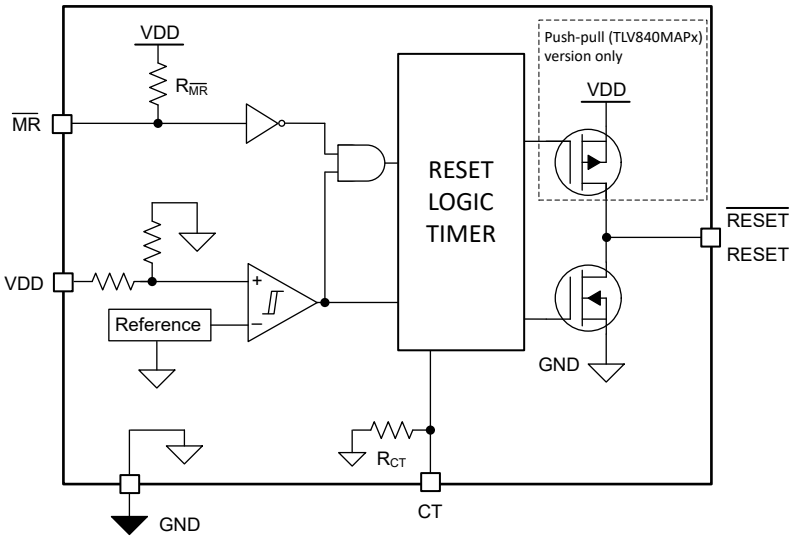
8 Detailed Description

8.1 Overview

The TLV840-Q1 is a family of nano-quiescent current voltage detectors with fixed threshold voltage. TLV840-Q1 features include programable reset time delay using external capacitor, active-low manual reset, 0.5% typical monitor threshold accuracy with hysteresis and glitch immunity.

Fixed negative threshold voltages (V_{IT-}) can be factory set from 0.8 V to 5.4 V. TLV840-Q1 is available in SOT-23 5-pin industry standard package.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Input Voltage (VDD)

VDD pin is monitored by the internal comparator to indicate when VDD falls below the fixed threshold voltage. VDD also functions as the supply for the internal bandgap, internal regulator, state machine, buffers and other control logic blocks. Good design practice involve placing a 0.1 µF to 1 µF bypass capacitor at VDD input for noisy applications to ensure enough charge is available for the device to power up correctly.

8.3.1.1 VDD Hysteresis

The internal comparator has built-in hysteresis to avoid erroneous output reset release. If the voltage at the VDD pin falls below V_{IT-} the output reset is asserted. When the voltage at the VDD pin goes above V_{IT-} plus hysteresis (V_{HYS}) the output reset is deasserted after t_D delay.

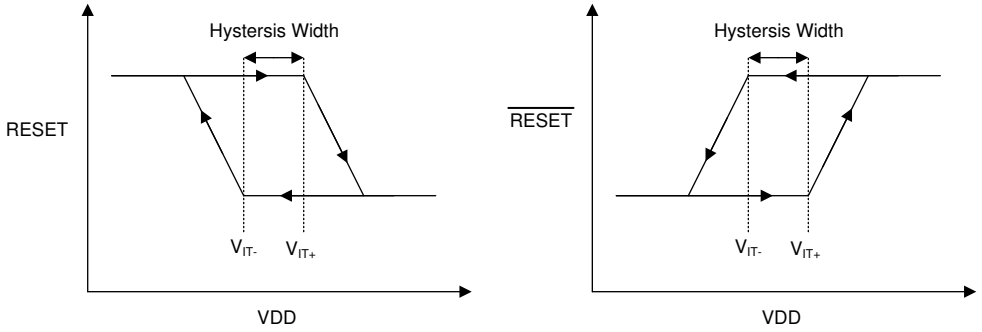


Figure 8-1. Hysteresis Diagram

8.3.1.2 VDD Transient Immunity

The TLV840-Q1 is immune to quick voltage transients or excursion on VDD. Sensitivity to transients depends on both pulse duration (t_{GI_VIT-}) found in Section 7.6 and overdrive. Overdrive is defined by how much VDD deviates from the specified threshold. Threshold overdrive is calculated as a percent of the threshold in question, as shown in Equation 1.

$$\text{Overdrive} = | [(V_{DD} / V_{IT-}) - 1] \times 100\% | \quad (1)$$

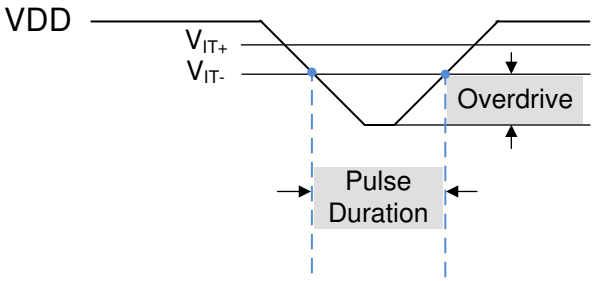


Figure 8-2. Overdrive vs Pulse Duration

8.3.2 User-Programmable Reset Time Delay

The reset time delay can be set to a minimum value of 80 µs by leaving the CT pin floating, or a maximum value of approximately 6.2 seconds by connecting 10 µF delay capacitor. The reset time delay (t_D) can be programmed by connecting a capacitor no larger than 10 µF between CT pin and GND.

The relationship between external capacitor (C_{CT}) in µF at CT pin and the time delay (t_D) in seconds is given by Equation 2.

$$t_{D\ (typ)} = -\ln (0.29) \times R_{CT} \times C_{CT} + t_{D\ (no\ cap)} \quad (2)$$

Equation 3 solves for external capacitor (µF) by plugging R_{CT} and t_D (CT pin = Open) given in Section 7.5 section:

$$C_{CT} = (t_D - 80\ \mu s) \div 618937 \quad (3)$$

The reset delay varies according to three variables: the external capacitor (C_{CT}), CT pin internal resistance (R_{CT}) provided in Section 7.5, and a constant. The minimum and maximum variance due to the constant is show in Equation 4 and Equation 5:

$$t_{D\ (min)} = -\ln (0.37) \times R_{CT\ (min)} \times C_{CT\_EXT\ (min)} + t_{D\ (no\ cap)} \quad (4)$$

$$t_{D\ (max)} = -\ln (0.25) \times R_{CT\ (max)} \times C_{CT\_EXT\ (max)} + t_{D\ (no\ cap)} \quad (5)$$

The recommended maximum delay capacitor for the TLV840-Q1 is limited to 10 µF as this ensures there is enough time for the capacitor to fully discharge when the reset condition occurs. When a voltage fault occurs, the previously charged up capacitor discharges, and if the monitored voltage returns from the fault condition before the delay capacitor discharges completely, the reset delay will be shorter than expected because the delay capacitor will begin charging from a voltage above zero. Larger delay capacitors can be used so long as the capacitor has enough time to fully discharge during the duration of the voltage fault. The amount of time required to discharge the delay capacitor relative to the reset delay increases as VDD overdrive increases as shown in Figure 8-3. From the graph below, to ensure the CT capacitor is fully discharged, the time period or duration of the voltage fault needs to be greater than 10% of the programmed reset time delay.

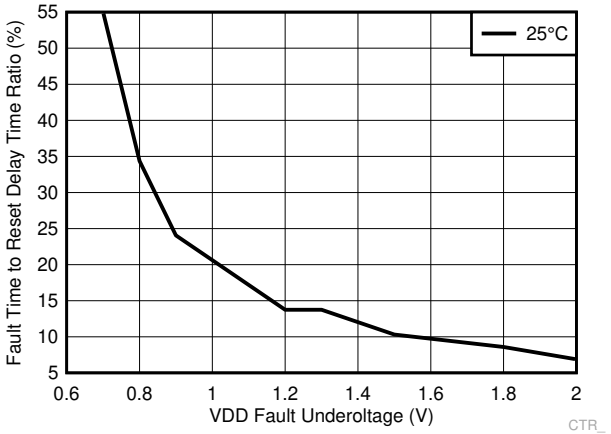


Figure 8-3. C_{CT} Discharge Time During Fault Condition (V_{IT-} = 2 V, C_{CT} = 1 µF)

8.3.3 Manual Reset ($\overline{MR}$) Input

The manual reset ($\overline{MR}$) input allows a processor GPIO or other logic circuits to initiate a reset. A logic low on $\overline{MR}$ with pulse duration longer than $t_{\overline{MR}\_PW}$ will cause the reset output to assert. After $\overline{MR}$ returns to a logic high ($V_{\overline{MR}\_H}$) and VDD is above V_{IT+}, reset is deasserted after the user programmed reset time delay (t_D) expires.

The minimum duration for which $\overline{MR}$ is held under $V_{\overline{MR}\_L}$ must be at least 1% of $t_{\overline{MR}\_tD}$. Otherwise, the effective reset delay will be shorter roughly by the difference between 1% of $t_{\overline{MR}\_tD}$ and the actual $\overline{MR}$ pulse width. For large capacitor based delays this difference could be noticeable unless care is taken to lengthen the $\overline{MR}$ pulse width.

$\overline{MR}$ is internally connected to VDD through a pull-up resistor $R_{\overline{MR}}$ shown in Section 8.2. If the logic signal controlling $\overline{MR}$ is less than VDD, then additional current flows from VDD into $\overline{MR}$ internally. For minimum current consumption, drive $\overline{MR}$ to either VDD or GND. $V_{\overline{MR}}$ should not be higher than VDD voltage.

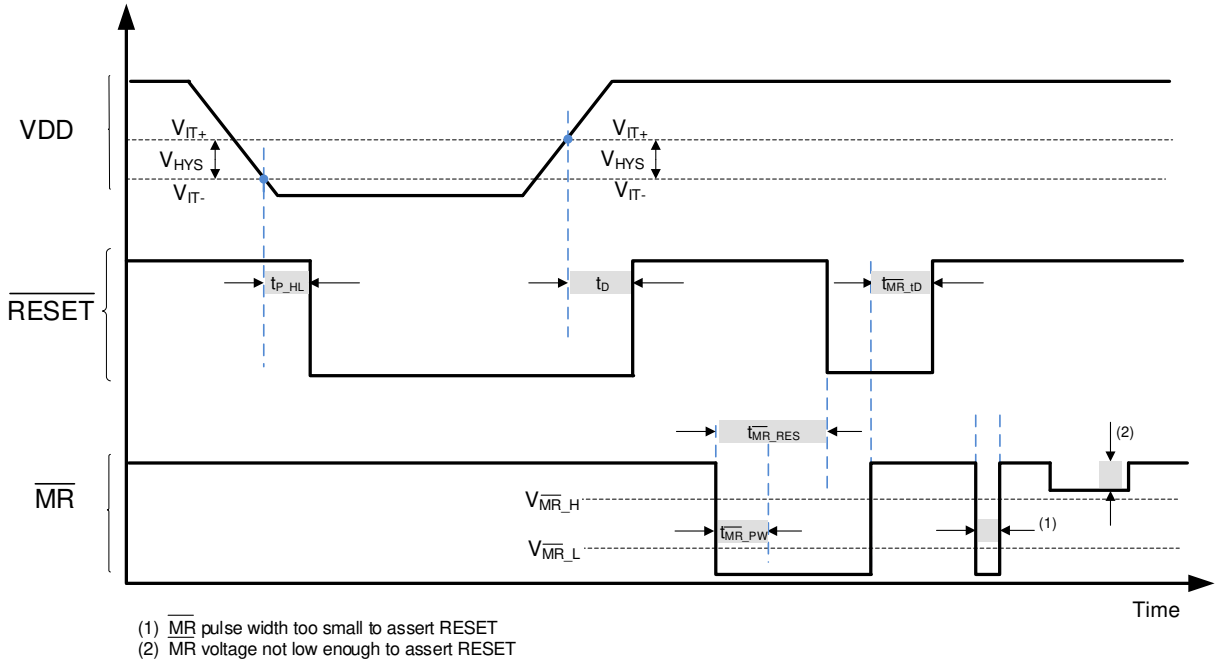


Figure 8-4. Timing Diagram $\overline{MR}$ and $\overline{RESET}$

8.3.4 Output Logic

8.3.4.1 $\overline{\text{RESET}}$ Output, Active-Low

$\overline{\text{RESET}}$ (Active-Low) applies to TLV840D**L**-Q1 (Open-Drain) and TLV840P**L**-Q1 (Push-Pull) hence the "**L**" in the device name. $\overline{\text{RESET}}$ remains high (deasserted) as long as VDD is above the negative threshold (V_{IT-}) and the $\overline{\text{MR}}$ pin is floating or above $V_{\overline{MR}\_H}$. If VDD falls below the negative threshold (V_{IT-}) or if $\overline{\text{MR}}$ is driven low, then $\overline{\text{RESET}}$ is asserted.

When $\overline{\text{MR}}$ is again logic high or floating and VDD rise above V_{IT+}, the delay circuit will hold $\overline{\text{RESET}}$ low for the specified reset time delay (t_D). When the reset time delay has elapsed, the $\overline{\text{RESET}}$ pin goes back to logic high voltage (V_{OH}).

The TLV840**D**L-Q1 (Open-Drain) version, denoted with "**D**" in the device name, requires an external pull-up resistor to hold $\overline{\text{RESET}}$ pin high. Connect the external pull-up resistor to the desired pull-up voltage source and $\overline{\text{RESET}}$ can be pulled up to any voltage up to 6.5 V independent of the VDD voltage. To ensure proper voltage levels, give some consideration when choosing the pull-up resistor values. The external pull-up resistor value determines the actual V_{OL}, the output capacitive loading, and the output leakage current ($I_{lkg(OD)}$).

The Push-Pull variants (TLV840**P**L-Q1 and TLV840**P**H-Q1), denoted with "**P**" in the device name, does not require an external pull-up resistor.

8.3.4.2 RESET Output, Active-High

RESET (Active-High), denoted with no bar above the pin label, applies to TLV840D**H**-Q1 (Open-Drain) and TLV840P**H**-Q1 push-pull active-high version, hence the "**H**" in the device name. RESET remains low (deasserted) as long as VDD is above the negative threshold (V_{IT-}) and the $\overline{\text{MR}}$ pin is floating or above $V_{\overline{MR}\_H}$. If VDD falls below the negative threshold (V_{IT-}) or if $\overline{\text{MR}}$ is driven low, then RESET is asserted driving the RESET pin to high voltage (V_{OH}).

When $\overline{\text{MR}}$ is again logic high or floating and VDD rise above V_{IT+} the delay circuit will hold RESET high for the specified reset time delay (t_D). When the reset time delay has elapsed, the RESET pin goes back to logic low voltage (V_{OL}).

The TLV840**D**H-Q1 (Open-Drain) version, denoted with "**D**" in the device name, requires an external pull-up resistor to hold RESET pin high. Connect the external pull-up resistor to the desired pull-up voltage source and RESET can be pulled up to any voltage up to 6.5 V independent of the VDD voltage. To ensure proper voltage levels, give some consideration when choosing the pull-up resistor values. The external pull-up resistor value determines the actual V_{OL}, the output capacitive loading, and the output leakage current ($I_{lkg(OD)}$).

The Push-Pull variants (TLV840**P**L-Q1 and TLV840**P**H-Q1), denoted with "**P**" in the device name, does not require an external pull-up resistor.

8.4 Device Functional Modes

Table 8-1 summarizes the various functional modes of the device. Logic high is represented by "H" and logic low is represented by "L".

Table 8-1. Truth Table

VDD	$\overline{MR}$	RESET	$\overline{RESET}$
VDD < V_{POR}	Ignored	Undefined	Undefined
V_{POR} < V_{DD} < V_{IT-}	Ignored	H	L
VDD ≥ V_{IT-}	L	H	L
VDD ≥ V_{IT-}	H	L	H
VDD ≥ V_{IT-}	Floating	L	H

8.4.1 Normal Operation (V_{DD} > V_{POR})

When VDD is greater than V_{POR}, the reset signal is determined by the voltage on the VDD pin with respect to the trip point (V_{IT-})

- $\overline{MR}$ high: the reset signal corresponds to VDD with respect to the threshold voltage.
- $\overline{MR}$ low: in this mode, the reset is asserted regardless of the threshold voltage.

8.4.2 Below Power-On-Reset (V_{DD} < V_{POR})

When the voltage on VDD is lower than V_{POR}, the device does not have enough bias voltage to internally pull the asserted output low or high and reset voltage level is undefined.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The following sections describe in detail how to properly use this device, depending on the requirements of the final application.

9.2 Typical Application

9.2.1 Design 1: Dual Rail Monitoring with Power-up Sequencing

A typical application for the TLV840-Q1 is voltage rail monitoring and power-up sequencing as shown in Figure 9-1. The TLV840-Q1 can be used to monitor any rail above 0.9 V. In this design application, two TLV840-Q1 devices monitor two separate voltage rails and sequences the rails upon power-up. The TLV840MAPL29-Q1 is used to monitor the 3.3-V main power rail and the TLV840MADL10-Q1 is used to monitor the 1.2-V rail provided by the LDO for other system peripherals. The $\overline{\text{RESET}}$ output of the TLV840MAPL29-Q1 is connected to the enable (EN) input of the LDO. A reset event is initiated on either voltage supervisor when the VDD voltage is less than V_{IT-}. For a system-wide reset event, both $\overline{\text{MR}}$ pins are tied to the $\overline{\text{SYS\_RST}}$. For the purpose of this application, the design detail on $\overline{\text{MR}}$ are not covered. For more information on the function of $\overline{\text{MR}}$, please see Section 8.3.3

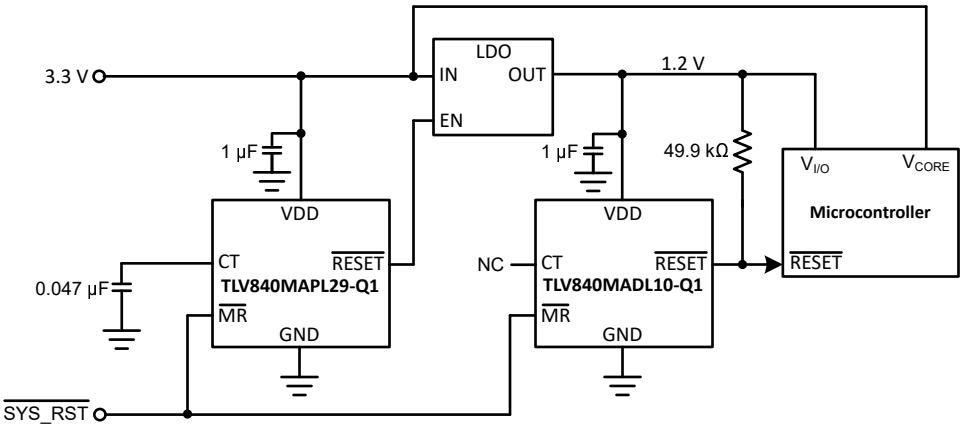


Figure 9-1. TLV840-Q1 Voltage Rail Monitor and Power-Up Sequencer Design Block Diagram

9.2.1.1 Design Requirements

This design requires voltage supervision on two separate rails: 3.3-V and 1.2-V rails. The voltage rail needs to sequence upon power up with the 3.3-V rail coming up first followed by the 1.2-V rail at least 25 ms after.

PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT
Two Rail Voltage Supervision	Monitor 3.3-V and 1.2-V rails	Two TLV840-Q1 devices provide voltage monitoring with 1% accuracy with device options available in 0.1 V variations
Voltage Rail Sequencing	Power up the 3.3-V rail first followed by 1.2-V rail 25 ms after	The CT capacitor on TLV840MAPL29-Q1 is set to 0.047 µF for a reset time delay of 29 ms typical
Maximum device current consumption	1 µA	Each TLV840-Q1 requires 120 nA typical

9.2.1.2 Detailed Design Procedure

The primary constraint for this application is choosing the correct device to monitor the supply voltage of the microprocessor. The TLV840-Q1 can monitor any voltage between 0.8 V and 5.4 V. Depending on how far away from the nominal voltage rail the user wants the voltage supervisor to trigger determines the correct voltage supervisor variant to choose. In this example, the first TLV840-Q1 triggers when the 3.3-V rail falls to 2.9 V. The second TLV840-Q1 triggers a reset when the 1.2-V rail falls to 0.9 V. The secondary constraint for this application is the reset time delay that must be at least 25 ms to allow the microprocessor, and all other devices using the 3.3-V rail, enough time to startup correctly before the 1.2-V rail is enabled via the LDO. Because a minimum time is required, the user must account for capacitor tolerance. For applications with ambient temperatures ranging from –40°C to +125°C, C_{CT} can be calculated using R_{CT} and solving for C_{CT} in Equation 2. Solving Equation 2 for 25 ms gives a minimum capacitor value of 0.0403 µF which is rounded up to a standard value 0.047 µF to account for capacitor tolerance.

A 1 µF decoupling capacitor is connected to the VDD pin as a good analog design practice. The pull-up resistor is only required for the Open-Drain device variants and is calculated to ensure that V_{OL} does not exceed max limit given the Isink possible at the expected supply voltage. In this design example nominal VDD is 1.2 V but dropping to 0.9 V. In Section 7.5, max V_{OL} provides 15 µA I sink for 0.7 V VDD, which is the closest voltage to this design example. Using 15 µA of Isink and 300 mV max V_{OL}, gives us 40 kΩ for the pull-up resistor. Any value higher than 40 kΩ would ensure that V_{OL} will not exceed 300 mV max specification.

9.2.1.3 Application Curves

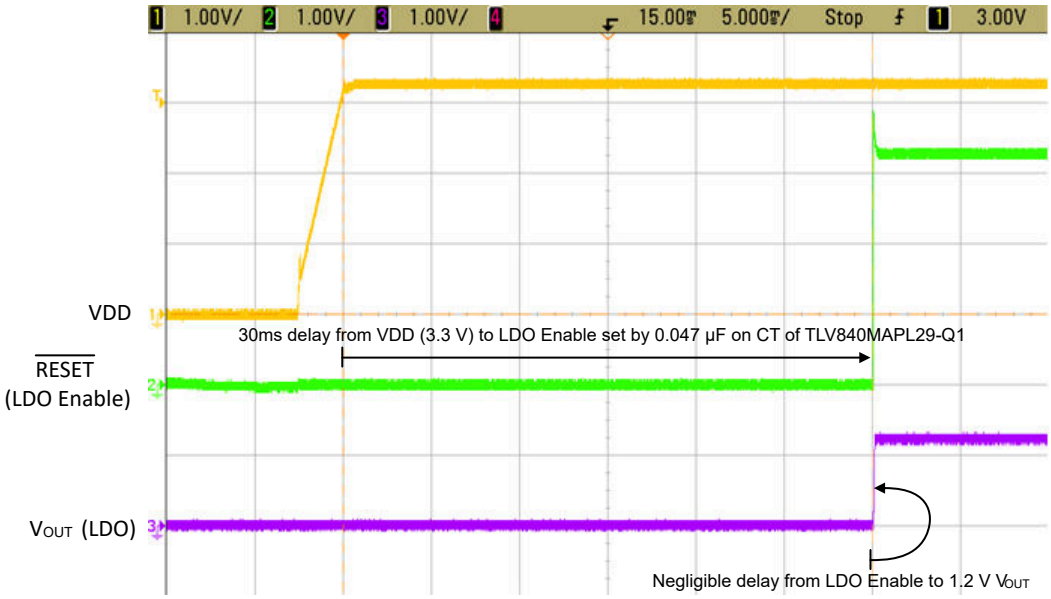


Figure 9-2. Startup Sequence Highlighting the Delay Between 3.3 V and 1.2 V Rails

9.2.2 Application Curve: Adjusting Output Reset Delay on TLV840EVM

These application curves are taken with the TLV840EVM and they display a change in reset delay time with different capacitor values. The output reset delay time was designed with the ease of programability for the customer. Figure 9-3 displays an output reset delay time of 57.6 µs with no capacitor on the CT pin. Figure 9-4 and Figure 9-5 have output reset delay times of 5.42 ms and 56.8 ms, respectively. Both the output delay times and capacitors used resulted in an order of magnitude difference. Please see the *TLV840EVM User Guide* for more information.

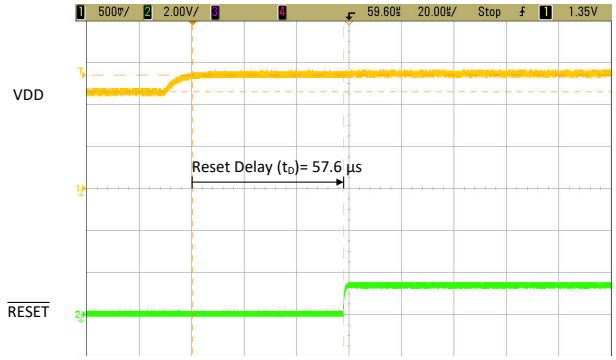


Figure 9-3. TLV840EVM $\overline{\text{RESET}}$ Time Delay (t_D) with No Capacitor

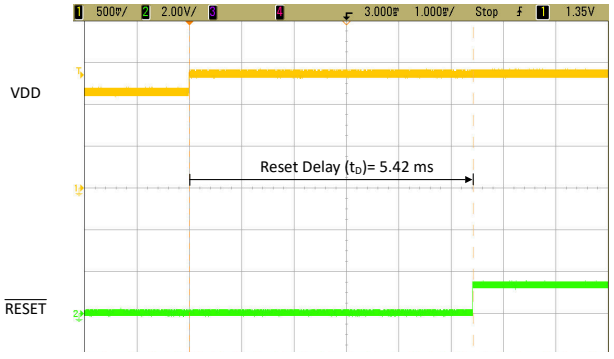


Figure 9-4. TLV840EVM $\overline{\text{RESET}}$ Time Delay (t_D) with 0.01-µF Capacitor

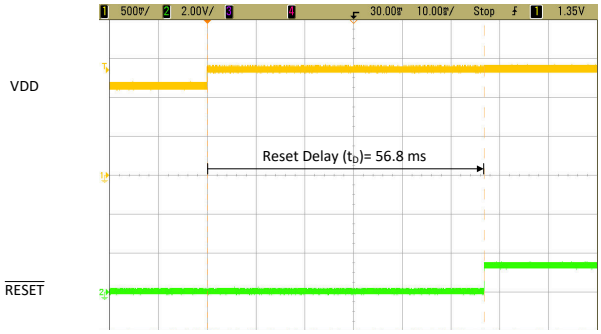


Figure 9-5. TLV840EVM $\overline{\text{RESET}}$ Time Delay (t_D) with 0.1-µF Capacitor

10 Power Supply Recommendations

The TLV840 is designed to operate from an input supply with a voltage range between 0.7 V and 6 V. TI recommends an input supply capacitor between the VDD pin and GND pin. This device has a 6.5 V absolute maximum rating on the VDD pin. If the voltage supply providing power to VDD is susceptible to any large voltage transient that can exceed 6.5 V, additional precautions must be taken.

11 Layout

11.1 Layout Guidelines

Make sure that the connection to the VDD pin is low impedance. Good analog design practice recommends placing a minimum 0.1 µF ceramic capacitor as near as possible to the VDD pin. If a capacitor is not connected to the CT pin, then minimize parasitic capacitance on this pin so the rest time delay is not adversely affected.

- Make sure that the connection to the VDD pin is low impedance. Good analog design practice is to place a > 0.1 µF ceramic capacitor as near as possible to the VDD pin.
- If a C_{CT} capacitor is used, place these components as close as possible to the CT pin. If the CT pin is left unconnected, make sure to minimize the amount of parasitic capacitance on the pin to < 5 pF.
- Place the pull-up resistors on $\overline{\text{RESET}}$ pin as close to the pin as possible.

11.2 Layout Example

The layout example in shows how the TLV840DL-Q1 is laid out on a printed circuit board (PCB) with a user-defined delay.

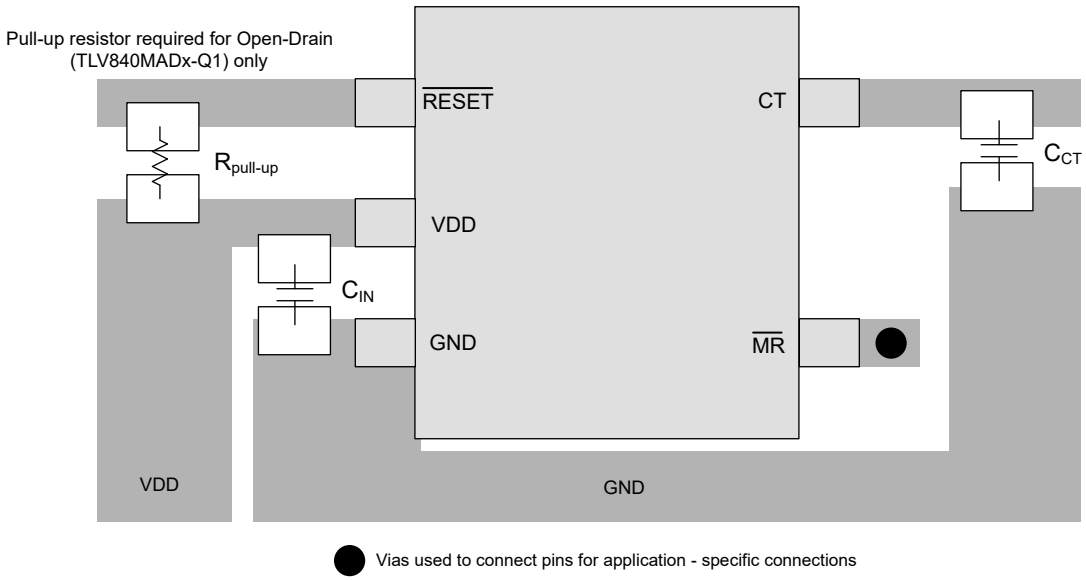


Figure 11-1. TLV840M-Q1 Recommended Layout

12 Device and Documentation Support

12.1 Device Nomenclature

Table 12-1 shows how to decode the function of the device based on its part number

Table 12-1. Device Naming Convention

DESCRIPTION	NOMENCLATURE	VALUE
Generic Part number	TLV840	TLV840
Feature Option	M 1	Manual Reset option in addition to CT pin
Delay Option	A	40 µs (Default internal reset time delay)
Variant code (Output Topology)	DL	Open-Drain, Active-Low
	PL	Push-Pull, Active-Low
	DH	Open-Drain, Active-High
	PH	Push-Pull, Active-High
Detect Voltage Option	## (two characters)	Example: 12 stands for 1.2 V threshold
Package	DBV	SOT23-5
Reel	R	Large Reel
Automotive Version	Q1	AEC-Q100

1. Orderable part numbers with TLV840M-Q1 are only available with the delay option A. However, longer delays can be achieved through an external capacitor on the CT pin. Leaving the CT pin floating will result in typical 40 µs delay feature option.

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

12.4 Trademarks

All trademarks are the property of their respective owners.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV840MADL12DBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2HNF	Samples
TLV840MADL22DBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2HOF	Samples
TLV840MADL30DBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2HPF	Samples
TLV840MADL31DBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2HMF	Samples
TLV840MADL32DBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2HQF	Samples
TLV840MADL40DBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2HDF	Samples
TLV840MAPH29DBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2INF	Samples
TLV840MAPL36DBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	2HVF	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TLV840-Q1 :

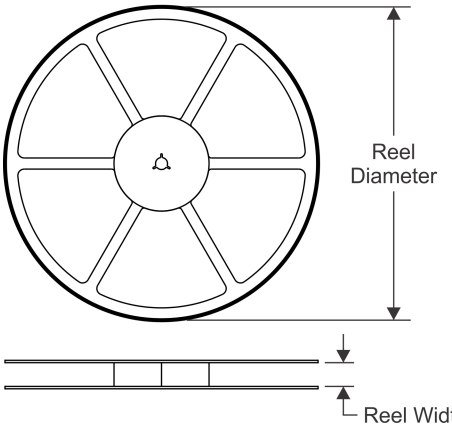
- Catalog : TLV840

NOTE: Qualified Version Definitions:

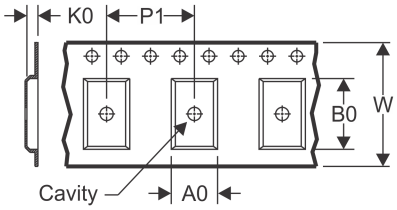
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

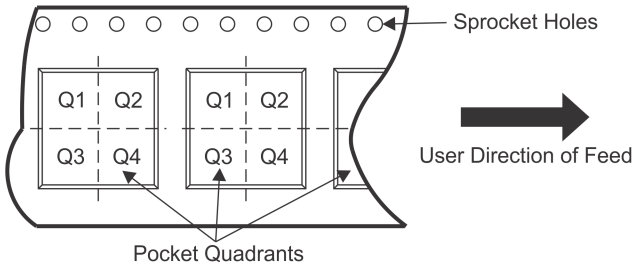


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

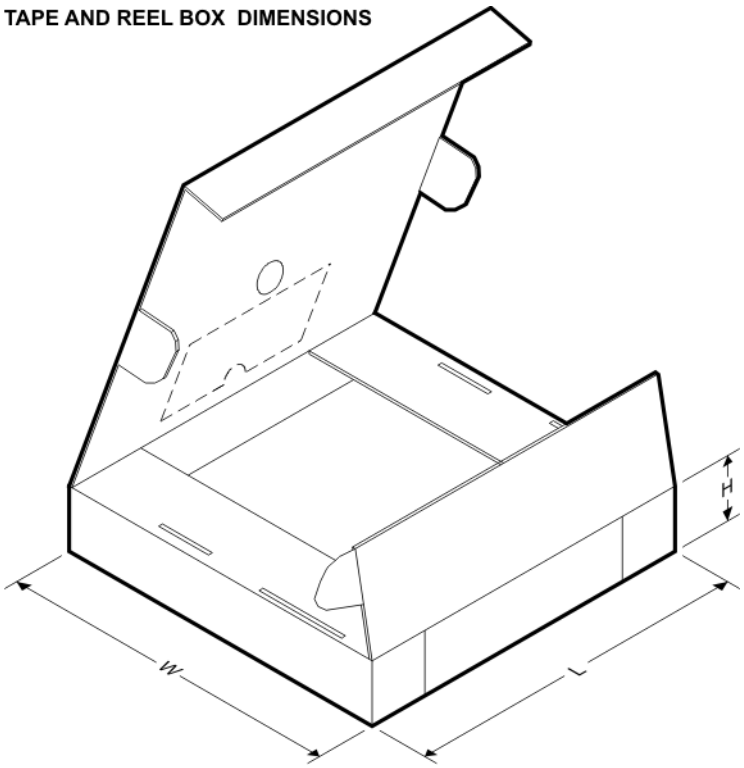
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV840MADL12DBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV840MADL22DBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV840MADL30DBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV840MADL31DBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV840MADL32DBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV840MADL40DBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV840MAPH29DBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV840MAPL36DBVRQ1	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

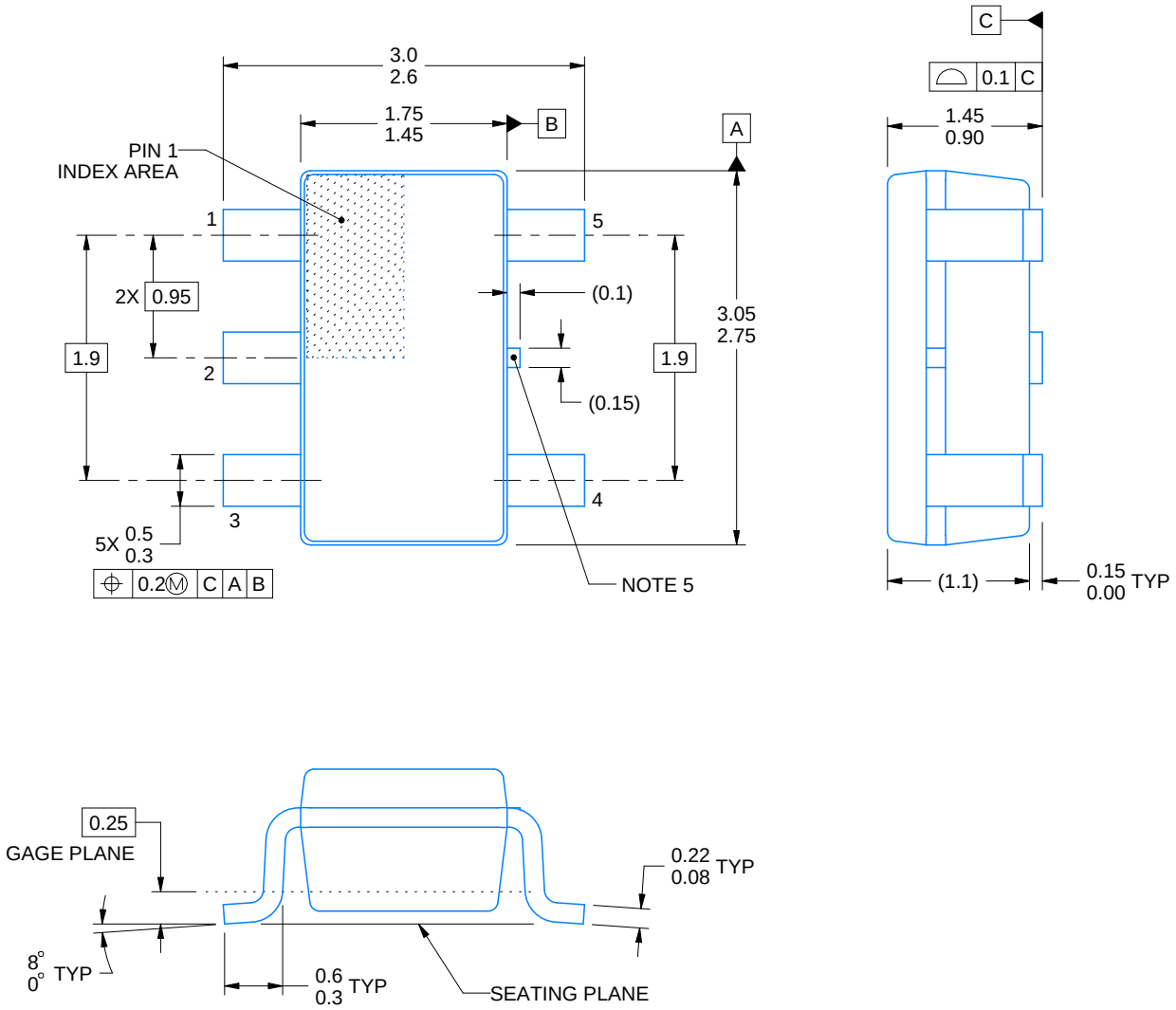
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV840MADL12DBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV840MADL22DBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV840MADL30DBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV840MADL31DBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV840MADL32DBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV840MADL40DBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV840MAPH29DBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV840MAPL36DBVRQ1	SOT-23	DBV	5	3000	210.0	185.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

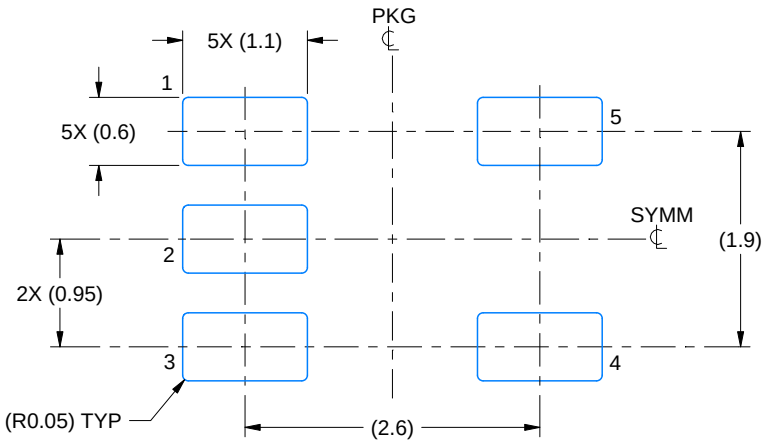
SMALL OUTLINE TRANSISTOR



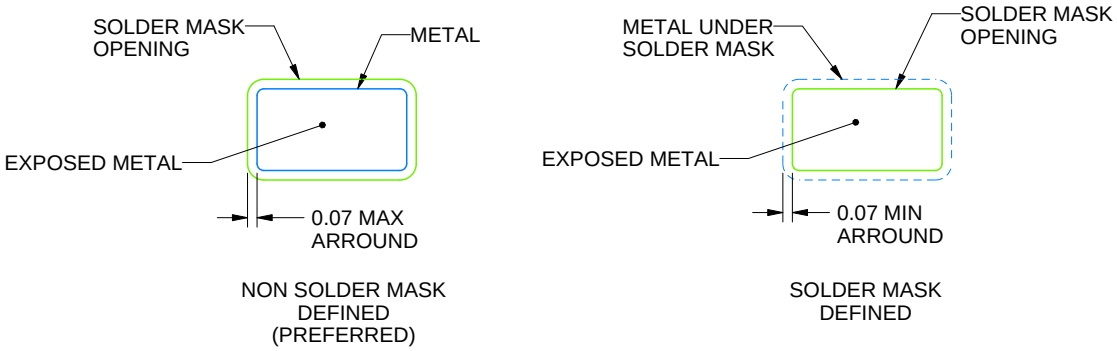
4214839/G 03/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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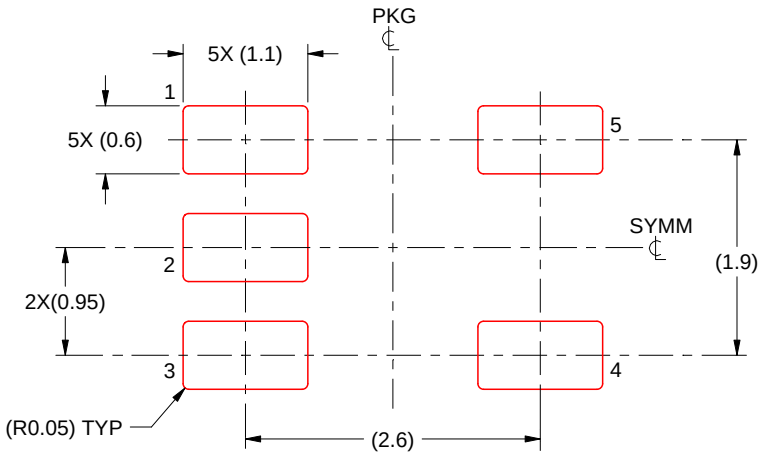
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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