CHANGE NOTIFICATION

Linear Technology Corporation
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November 02, 2015

Dear Sir/Madam: PCN# 110215

Subject: Notification of Change to LTC4217

Please be advised that Linear Technology Corporation has made a change to the lead frame of the LTC4217 device to meet IPC/ JEDEC JSTD-020 Moisture Sensitivity Level 1 Classification. Moisture Sensitivity Level 1 classified devices can be shipped without dry pack with unlimited shelf life. Device with improved leadframe have longer moisture soak and more aggressive IR temp ramps.

The change includes adding an array of slot holes along the edge of the die attach paddle as mold locking feature to enhance mold adhesion mechanism to the lead frames. In addition to facilitate improvement in our manufacturing yield, a minor change was done to the datasheet as shown on the attached page of the marked up datasheet. The improved product with approximate date code of 1601 will be tested to the new limits.

Besides these changes, there was no change in form, fit, function, quality or reliability of the product. Similarly, there are no changes associated with the package footprint, PCB layout or product top marking, so the customer applications will be unaffected.

Parts incorporating the new lead frame design have been fully characterized and tested for package level reliability. The change was qualified by performing extensive characterization over the full operating voltage and temperature ranges and MSL1 preconditioning. Device with the new lead frame has been subjected to 1000 cycles of temperature cycles and thermal shock. Products built using the improved design will be shipped with a date code of approximately 1601.

Should you have any further questions or concerns please contact your local Linear Technology Sales person or you may contact me at 408-432-1900 ext. 2077, or by e-mail at jason.hu@linear.com. If I do not hear from you by January 4, 2016, we will consider this change to be approved by your company.

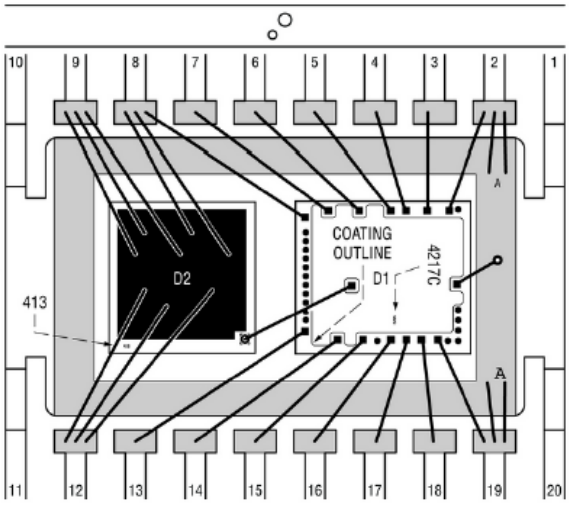
Sincerely,

Jason Hu

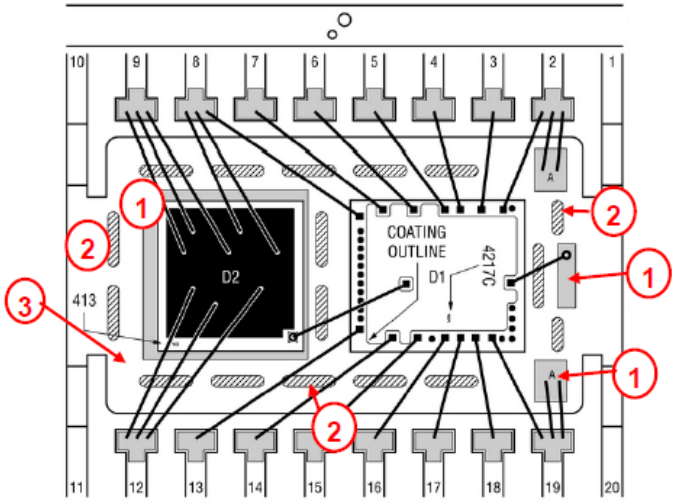
Quality Assurance Engineer

LTC4217 Leadframe Design Improvement

Existing Leadframe Design

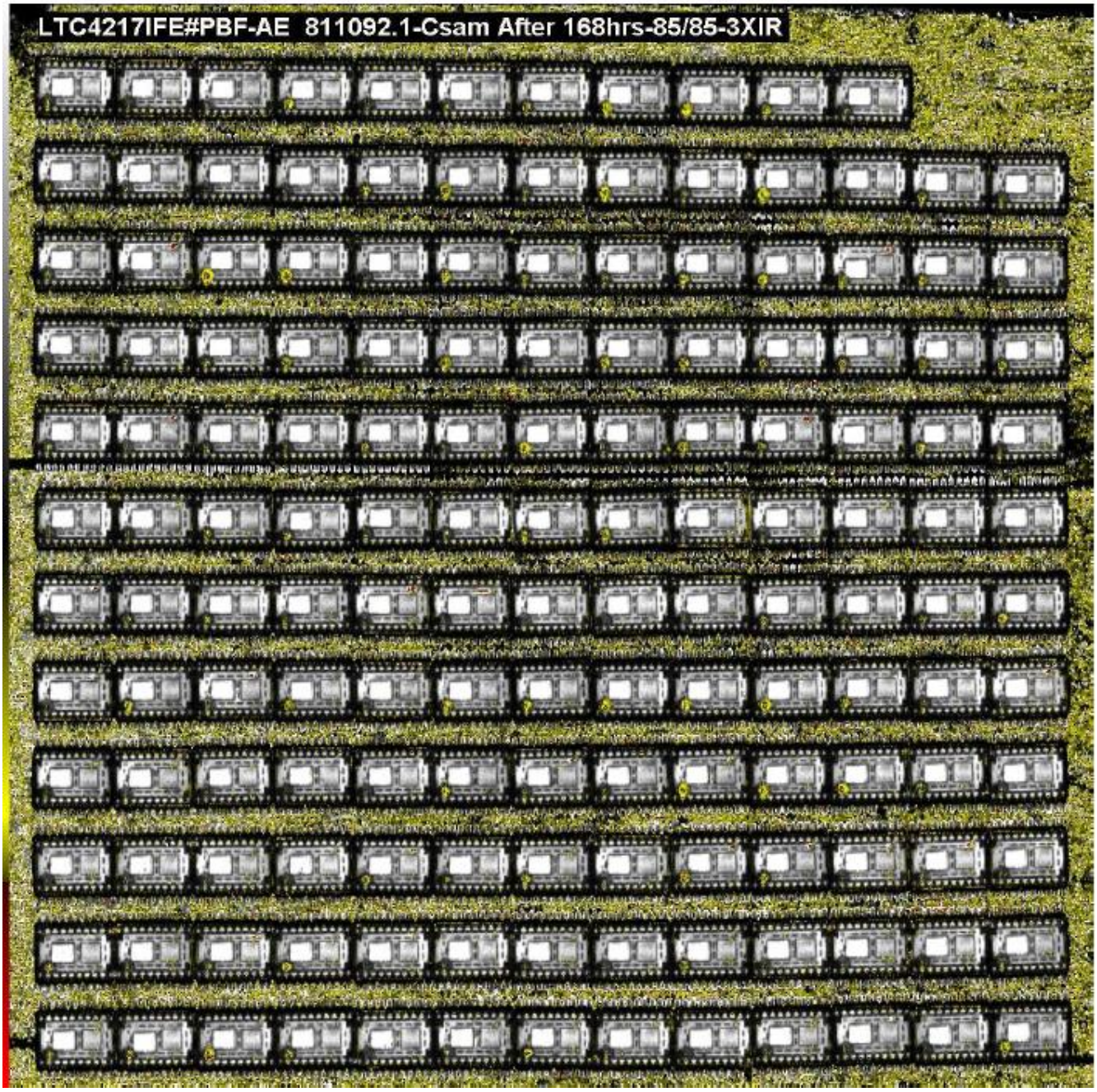


Improved Leadframe Design



1. Silver ring is replaced by spot silver on areas under FET die (D2), and for Rsense and down bond bonding to improve adhesion.
2. Half etched slots are added on the peripheral of die pad and between dies to enhance adhesion.
3. Brown oxide is added to die pad surface other than spot Ag areas to improve adhesion.

Post MSL 1 Precondition C-SAM image without delamination



QUALIFICATION DATA
LTC4217 Leadframe Change
9/24/2015

• HIGH TEMPERATURE OPERATING LIFE AT 125°C

DEVICE TYPE	SAMPLE SIZE	DATE CODE	HOURS ON HTOL	DEVICE HOURS AT +125°C	NUMBER OF FAILURES
LTC4217	78	1521	500	39,000	0

• HIGHLY ACCELERATED STRESS TEST (HAST) AT +130°C/85% R.H. WITH BIAS[1]

DEVICE TYPE	SAMPLE SIZE	DATE CODE	HOURS ON HAST	DEVICE HOURS AT +130°C	NUMBER OF FAILURES
LTC4217	146	1521	96	14,016	0

• PRESSURE COOKER TEST (PCT) AT 15 PSIG, +121°C/100% R.H[1,2]

DEVICE TYPE	SAMPLE SIZE	DATE CODE	HOURS ON PCT	DEVICE HOURS AT +130°C	NUMBER OF FAILURES
LTC4217	220	1521	168.00	36,960	0

• TEMP CYCLE FROM -65°C TO +150°C[1,2]

DEVICE TYPE	SAMPLE SIZE	DATE CODE	CYCLES ON TC	DEVICE HOURS	NUMBER OF FAILURES
LTC4217	229	1521	1000.00	229,000	0

• THERMAL SHOCK FROM -65°C TO +150°C[1,2]

DEVICE TYPE	SAMPLE SIZE	DATE CODE	CYCLES ON TS	DEVICE HOURS	NUMBER OF FAILURES
LTC4217	231	1521	1000.00	231,000	0

• HIGH TEMPERATURE BAKE AT 150°C

DEVICE TYPE	SAMPLE SIZE	DATE CODE	HOURS ON HTB	DEVICE HOURS AT +125°C	NUMBER OF FAILURES
LTC4217	148	1521	1,000	148,000	0

• ACCELERATED PRECONDITIONING, 3h PCT + 3x REFLOW AT +260°C PEAK[2]

DEVICE TYPE	SAMPLE SIZE	DATE CODE	HOURS ON PCT	DEVICE HOURS AT +121°C	NUMBER OF FAILURES
LTC4217	75	1521	3.00	225	0

• SOLDER SHOCK, 3h PCT + 1x IMMERSION AT +245°C PEAK

DEVICE TYPE	SAMPLE SIZE	DATE CODE	HOURS ON PCT	DEVICE HOURS AT +121°C	NUMBER OF FAILURES
LTC4217	75	1521	3.00	225	0

(1) Environmental stress are preceded by JEDEC Level 1 Preconditioning: 168h 85°C/85% R.H. plus 3x Reflow at 260°C.
(2) C-SAM analysis shows superior lamination performance of new leadframe / die attach material compared to control after reflow.
(3) Initial electrical test yields at hot are superior for new leadframe / die attach material compared to control.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{DD} = 12V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Inputs							
I_{IN}	OV, UV, FB Pin Input Current	V_{IN} = 1.2V, LTC4217	●		0	±1	µA
R_{IN}	OV, UV, FB Pin Input Resistance	LTC4217-12	●	13	18	23	kΩ
V_{TH}	OV, UV, FB Pin Threshold Voltage	V_{IN} Rising	●	1.21	1.235	1.26	V
$\Delta V_{OV(HYST)}$	OV Pin Hysteresis		●	10	20	30	mV
$\Delta V_{UV(HYST)}$	UV Pin Hysteresis		●	50	80	110	mV
$V_{UV(RTH)}$	UV Pin Reset Threshold Voltage	V_{UV} Falling	●	0.55	0.62	0.7	V
$\Delta V_{FB(HYST)}$	FB Pin Power Good Hysteresis		●	10	20	30	mV
R_{ISET}	I_{SET} Pin Internal Resistor		●	19	20	21	kΩ
Outputs							
V_{OL}	PG, $\overline{FLT}$ Pin Output Low Voltage	I_{OUT} = 2mA C-Grade, I-Grade H-Grade	 ● ●		 0.4 0.4	 0.8 0.92	 V V
I_{OH}	PG, $\overline{FLT}$ Pin Input Leakage Current	V_{OUT} = 30V	●		0	±10	µA
$V_{TIMER(H)}$	TIMER Pin High Threshold	V_{TIMER} Rising	●	1.2	1.235	1.28	V
$V_{TIMER(L)}$	TIMER Pin Low Threshold	V_{TIMER} Falling	●	0.1	0.21	0.3	V
$I_{TIMER(UP)}$	TIMER Pin Pull-Up Current	V_{TIMER} = 0V	●	–80	–100	–120	µA
$I_{TIMER(DN)}$	TIMER Pin Pull-Down Current	V_{TIMER} = 1.2V	●	1.4	2	2.6	µA
$I_{TIMER(RATIO)}$	TIMER Pin Current Ratio $I_{TIMER(DN)}/I_{TIMER(UP)}$		●	1.6	2	2.7	%
A_{IMON}	I_{MON} Pin Current Gain	I_{OUT} = 2A	●	47.5	50	52.5	µA/A
$I_{OFF(IMON)}$	I_{MON} Pin Offset Current	I_{OUT} = 132mA	●		0	±7.5	µA
$I_{GATE(UP)}$	Gate Pull-Up Current	Gate Drive On, $V_{GATE} = V_{OUT}$ = 12V	●	–19	–24	–29	µA
$I_{GATE(DN)}$	Gate Pull-Down Current	Gate Drive Off, V_{GATE} = 18V, V_{OUT} = 12V C-Grade, I-Grade H-Grade	 ● ●	 190 164	 250 140	 400 500	 µA µA
$I_{GATE(FST)}$	Gate Fast Pull-Down Current	Fast Turn Off, V_{GATE} = 18V, V_{OUT} = 12V			140		mA
AC Characteristics							
$t_{PHL(GATE)}$	Input High (OV), Input Low (UV) to Gate Low Propagation Delay	V_{GATE} < 16.5V Falling	●		8	10	µs
$t_{PHL(ILIM)}$	Short-Circuit to Gate Low	V_{FB} = 0, Step I_{SENSE} to 1.2A, V_{GATE} < 16.5V Falling	●		1	5	µs
$t_{D(ON)}$	Turn-On Delay	Step V_{UV} to 2V, V_{GATE} > 13V	●	50	100	150	ms
$t_{D(CB)}$	Circuit Breaker Filter Delay Time (Internal)	V_{FB} = 0V, Step I_{SENSE} to 1.2A C-Grade, I-Grade H-Grade	 ● ●	 1.5 1.4	 2 2	 2.7 2.7	 ms ms
$t_{D(AUTO-RETRY)}$	Auto-Retry Turn-On Delay (Internal)		●	50	100	150	ms

used to be 340uA; now changed to 400uA

used to be 355uA; now changed to 500uA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All currents into pins are positive, all voltages are referenced to GND unless otherwise specified.

Note 3: An internal clamp limits the GATE pin to a maximum of 6.5V above OUT. Driving this pin to voltages beyond the clamp may damage the device.

Note 4: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 5: T_J is calculated from the ambient temperature, T_A, and power dissipation, P_D, according to the formula:

LTC4217DHC, LTC4217DHC-12: $T_J = T_A + (P_D \bullet 43°C/W)$

LTC4217FE: $T_J = T_A + (P_D \bullet 38°C/W)$