LM3495 Emulated Peak Current Mode Buck Controller for Low Output Voltage

Check for Samples: LM3495

FEATURES

- **Input Voltage from 2.9V to 18V**
- **Output Voltage Adjustable from 0.6V to 5.5V**
- **Feedback Accuracy: ±1%**
- **Low-Side Sensing, Programmable Current Limit without Sense Resistor**
- **Input Under Voltage Lockout**
- **Hiccup Mode Current Limit Protection Eliminates Thermal Runaway During Fault Conditions**
- **Internal Soft Start with Tracking Capability**
- **200 kHz to 1.5 MHz Switching Frequency, Synchronizable**
- **On-Chip Gate Drivers**
- **Soft Output Discharge During Shutdown**
- **Startup into Output Pre-Bias**
- **Operation from a Single Input Rail**
- **Adaptive Duty Cycle Limit**
- **TSSOP-16 Package**

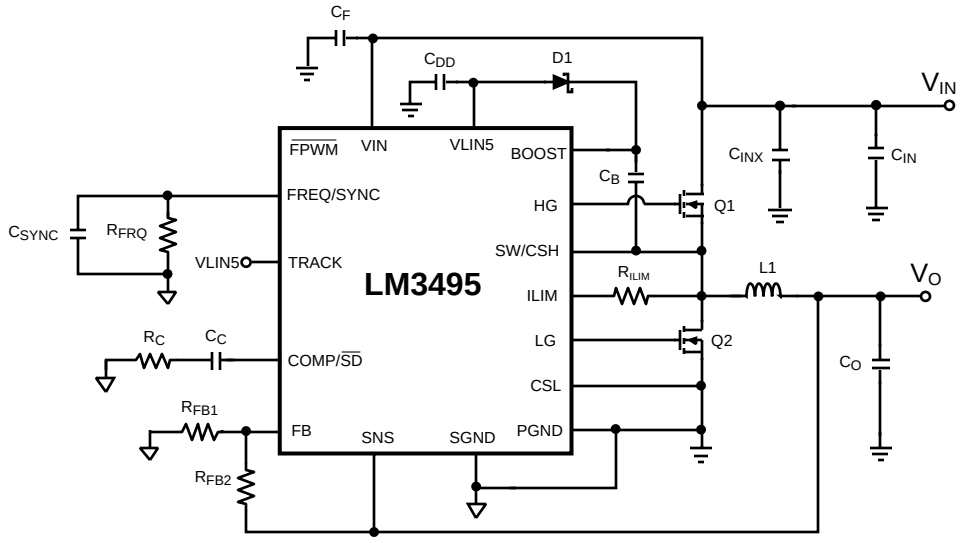
DESCRIPTION

The LM3495 is a PWM buck regulator which implements a unique emulated peak current mode control. This control method eliminates the switching noise which typically limits current mode operation at extremely short duty cycles and high operating frequency. The switching frequency is programmable between 200 kHz and 1.5 MHz, and can also be synchronized to an external clock. The LM3495 is also very fault tolerant with both switch node short, hiccup mode, and adaptive duty cycle limit protection. A 0.6V 1% reference and glitch free pre-biased start-up ensure the most demanding digital loads operate reliably. Internal soft start and the ability to track the output of another supply make the LM3495 versatile and efficient.

APPLICATIONS

- **Wide Input Voltage Buck Converters with Low Voltage, High Accuracy Outputs**
- **Core Logic Regulators**
- **High-Efficiency Buck Regulation**

Typical Application



Connection Diagram

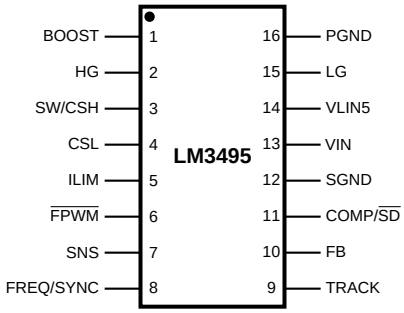


Figure 1. 16-Lead Plastic TSSOP Package (Top View)
See Package Number PW0016A
θ_{JA} = 155°C/W

PIN DESCRIPTIONS

BOOST (Pin 1): Supply rail for the high-side FET gate drive. The voltage should be at least one gate threshold above the regulator input voltage to properly turn on the high-side FET.
HG (Pin 2): Gate drive for the high-side N-channel FET. This signal is interlocked with LG to avoid shoot-through.
SW/CSH (Pin 3): Return path for the high-side FET driver and top Kelvin sense point for the load current. Connect this pin as close as possible to the drain of the low-side FET with a separate trace. Also used along with CSL for zero crossing detection.
CSL (Pin 4): Bottom sense point for the load current. Connect this as close as possible to the source of the low-side FET with a separate trace.
ILIM (Pin 5): Current limit threshold setting. This pin sources a fixed 20 µA current. A resistor of appropriate value should be connected between this pin and the drain of the low-side FET.
$\overline{\text{FPWM}}$ (Pin 6): Control mode select. An open circuit at this pin allows the IC to operate in skip mode at light loads. A logic low or connection to ground forces PWM operation at all times. This pin should not be pulled up to any voltage above 3.0V.
SNS (Pin 7): Output voltage sense pin. Connect this pin as close as possible to the positive terminal of the output capacitor with a separate trace. This pin connects to an internal FET that discharges the output capacitor during shutdown.
FREQ/SYNC (Pin 8): Switching frequency select pin and input for external clock. Connect a resistor from this pin to ground to determine switching frequency. Alternatively, a logic level clock signal between 200 kHz and 1.5 MHz can be applied to this pin through a 100 pF DC blocking capacitor to set the switching frequency.
TRACK (Pin 9): Tracking pin. To force the output of the LM3495 to track another power supply, connect a resistor divider (smaller than 10 kΩ for better precision) from the output of the other supply directly to this pin. When not used, this pin should be connected directly to the VLIN5 pin.
FB (Pin 10): Feedback pin. Connecting a resistor divider from the output voltage to this pin sets the DC level of the output voltage.
COMP/$\overline{\text{SD}}$ (Pin 11): Output of the error amplifier. The voltage level on this pin is compared with an internally generated ramp signal to determine the duty cycle. This pin is necessary for compensating the control loop. This pin must be left floating for the converter to regulate the output voltage in steady state. Forcing this pin below 0.3V shuts down the regulator.
SGND (Pin 12): Signal ground. Ground connection for the low power analog circuitry. Connect this pin to the PGND pin with a separate trace.
VIN (Pin 13): Input voltage. Input to an internal 4.7V linear regulator. Bypass this pin with a minimum 1 µF ceramic capacitor.
VLIN5 (Pin 14): Output of the internal 4.7V linear regulator. Provides power to the high-side bootstrap and low-side driver. Bypass this pin with a 2.2 µF ceramic capacitor to PGND.
LG (Pin 15): Gate drive for the low-side N-channel FET. This signal is interlocked with HG to avoid shoot-through.
PGND (Pin 16): Ground connection for the power circuitry. Connect to the source of the low-side FET and the output capacitor with heavy traces or a copper plane.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

VIN, ILIM		−0.3V to 20V
SW/CSH(3)		−0.5V to 20V
BOOST, HG		−0.3V to 25V
BOOST to SW		−0.3V to 6V
FB		−0.3V to 2V
TRACK, FREQ, FPWM, VLIN5, SNS, LG, CSL		−0.3V to 6V
Storage Temperature		−65°C to +150°C
Soldering Information	Lead Temperature (soldering, 10 sec)	260°C
	Infrared or Convection (15 sec)	235°C
ESD Rating(4)		2kV

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For ensured specifications and test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.
(3) An extended negative voltage limit of –2V applies for a duration of 20 ns per switching cycle
(4) The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin.

Operating Ratings(1)

Supply Voltage Range (V_{IN})	2.9V to 18V
BOOST to SW	2.5V to 5.5V
Junction Temperature	−40°C to +125°C

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For ensured specifications and test conditions, see the Electrical Characteristics.

Electrical Characteristics

Specifications with standard type are for T_J = 25°C only; limits in **boldface** type apply over the full Operating Junction Temperature (T_J) range. Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise indicated, V_{IN} = 12V.

Symbol	Parameter	Conditions	Min	Typ(1)	Max	Units
SYSTEM PARAMETERS						
V_{FB}	FB Pin Voltage	-20°C to 85°C	**0.594**	0.6	**0.606**	V
		-40°C to 125°C	**0.591**	0.6	**0.609**	
$\Delta V_{FB}/V_{FB}$	Line Regulation	2.9V < VIN < 18V, COMP/$\overline{SD}$ = 1.5V		0.1		%
	Load Regulation	1.1V < COMP/$\overline{SD}$ <1.8V		0.1		%
V_{ON}	UVLO Thresholds	VIN Rising	**2.55**	2.6	**2.7**	V
		VIN Falling	**2.26**	2.3	**2.45**	
I_Q	Operating VIN Current	COMP/$\overline{SD}$ > 0.3V, Not switching		1.8		mA
	Quiescent Current	COMP/$\overline{SD}$ < 0.3V, Shutdown, VIN = 18V		33		µA
I_{ILIM}	ILIM Pin Source Current		**18**	20	**22**	µA
$V_{ILIM-MAX}$	Maximum Current Limit Sense Voltage			200		mV
I_{SD}	COMP/$\overline{SD}$ Pin Pull-up current	COMP/$\overline{SD}$ = 0V		2	2.6	µA
V_{HICCUP}	COMP/$\overline{SD}$ Pin Hiccup Threshold			2		V
t_{DELAY}	Hiccup Delay			16		Cycles
t_{COOL}	Cool Down Time Until Restart			4096		Cycles
t_{SS}	Internal Soft start Time			400		Cycles
V_{OVP}	Over Voltage Protection Threshold	As a % of nominal output voltage	**116**	125	**132**	%
$I_{\overline{FPWM}}$	$\overline{FPWM}$ Pin Pull-up Current	$\overline{FPWM}$ = 0V		4.5		µA
$V_{FPWM-LO}$	FPWM Operation Threshold	FPWM Voltage Falling		0.9		V
R_{SNS}	SNS Pin Input Resistance	SNS = 1.5V, COMP/$\overline{SD}$ > 0.3V		30		kΩ
R_{DIS}	SNS Pin Discharge FET R_{DSON}	SNS = 1.5V, COMP/$\overline{SD}$ = 0V	**350**	440	**530**	Ω
GATE DRIVE						
I_{BOOST}	BOOST Pin Leakage Current	BOOST - SW = 5.5V		25		nA
R_{DS1}	High-Side FET Driver Pull-up ON resistance	BOOST - SW = 4.5V		4.5		Ω
R_{DS2}	High-Side FET Driver Pull-down ON resistance	BOOST - SW = 4.5V		0.9		Ω
R_{DS3}	Low-Side FET Driver Pull-up ON resistance	VLIN5 = 5.5V		1.4		Ω
R_{DS4}	Low-Side FET Driver Pull-down ON resistance	VLIN5 = 5.5V		0.7		Ω
OSCILLATOR						
f_{SW}	PWM Frequency	R_{ADJ} = 150 kΩ		200		kHz
		R_{ADJ} = 54.9 kΩ	**450**	500	**550**	
		R_{ADJ} = 17.8 kΩ		1500		
$V_{SYNC-HI}$	Threshold for SYNC on FREQ Pin	SYNC Voltage Rising		1.2		V
$V_{SYNC-LO}$	Threshold for SYNC on FREQ Pin	SYNC Voltage Falling		0.3		V
$t_{ON-SKIP}$	On Time During Skip Mode	V_O = 1.5V, f_{SW} = 500 kHz		125		ns
t_{ON-MAX}	Adaptive Maximum On-time Limit	V_O = 1.5V, f_{SW} = 500 kHz		750		ns
$t_{OFF-MIN}$	Minimum Off-time			300		ns
ERROR AMP						
g_M	Transconductance			750		µmho
BW_{-3dB}	Open Loop Bandwidth	COMP/$\overline{SD}$ Floating		5		MHz
I_{FB}	FB Pin Bias Current	V_{FB} = 0.6V		1		nA

(1) Typical specifications represent the most likely parametric norm at 25°C operation.

Electrical Characteristics (continued)

Specifications with standard type are for T_J = 25°C only; limits in **boldface** type apply over the full Operating Junction Temperature (T_J) range. Minimum and Maximum limits are specified through test, design, or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise indicated, V_{IN} = 12V.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Units
I_{SOURCE}	COMP/$\overline{SD}$ Pin Source Current	V_{FB} = 0.5V, COMP/$\overline{SD}$ = 1.5V		40		µA
I_{SINK}	COMP/$\overline{SD}$ Pin Sink Current	V_{FB} = 0.7V, COMP/$\overline{SD}$ = 1.5V		40		µA
$V_{COMP-HI}$	COMP/$\overline{SD}$ Pin Voltage High Clamp	V_{FB} = 0.5V		2		V
$V_{COMP-LO}$	COMP/$\overline{SD}$ Pin Voltage Low Clamp	V_{FB} = 0.7V		0.9		V
TRACKING						
V_{TEND}	Track End Threshold			0.6		V
$V_{TRACK-OS}$	Track to FB Offset	TRACK = 0.55V		15		mV
INTERNAL VOLTAGE REGULATOR						
V_{VLIN5}	Voltage at VLIN5 Pin[2]	V_{IN} = 12V, VLIN5 Current = 25 mA		4.72		V
		V_{IN} = 3.3V, VLIN5 Current = 25 mA		3.0		V
LOGIC INPUTS AND OUTPUTS						
V_{SD-HI}	COMP/$\overline{SD}$ Pin Logic High Trip Point	COMP/$\overline{SD}$ Pin Voltage Rising		0.3	**0.4**	V
V_{SD-LO}	COMP/$\overline{SD}$ Pin Logic Low Trip Point	COMP/$\overline{SD}$ Pin Voltage Falling	**0.2**	0.26		V
THERMAL CHARACTERISTICS						
θ_{JA}	Junction-to-Ambient Thermal Resistance			155		°C/W
T_{SD}	Thermal Shutdown Threshold			150		°C
T_{SD-HYS}	Thermal Shutdown Hysteresis			15		°C

(2) VLIN5 provides self bias for the internal gate drive and control circuits. Device thermal limitations limit external loading.

Typical Performance Characteristics

V_{IN} = 12V unless specified, T_A = 25°C unless specified.

FB Reference Voltage vs Temperature

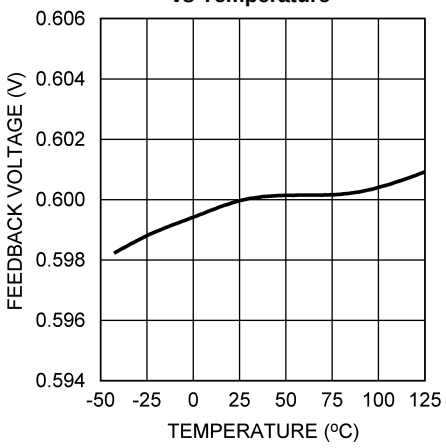


Figure 2.

Switching Frequency vs Temperature

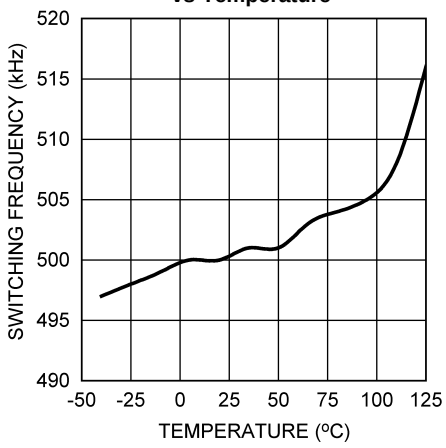


Figure 3.

VLIN5 Voltage vs Temperature

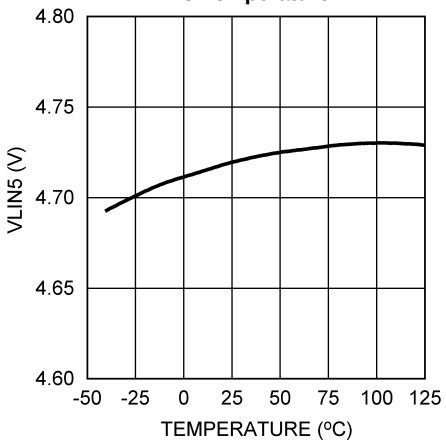


Figure 4.

Error Amplifier Transconductance vs Temperature

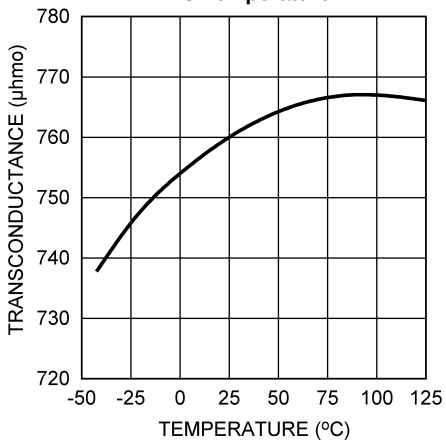


Figure 5.

VLIN5 Voltage vs VIN

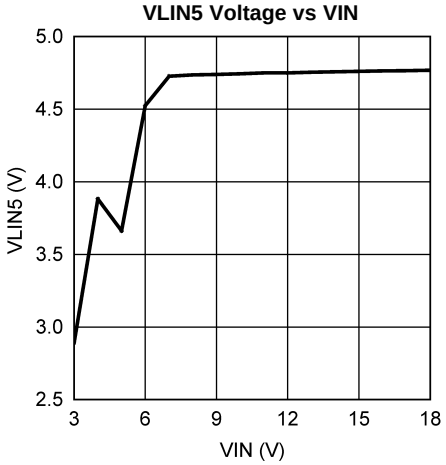


Figure 6.

Efficiency in SKIP Mode V_O = 2.2V, I_O = 10 mA to 500 mA BOM in Table 2

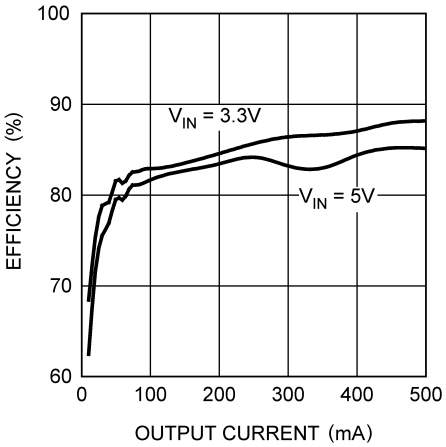


Figure 7.

Typical Performance Characteristics (continued)

V_{IN} = 12V unless specified, T_A = 25°C unless specified.

Efficiency in FPWM Mode
V_O = 1.0V, I_O = 0.5A to 7A
BOM in Table 1

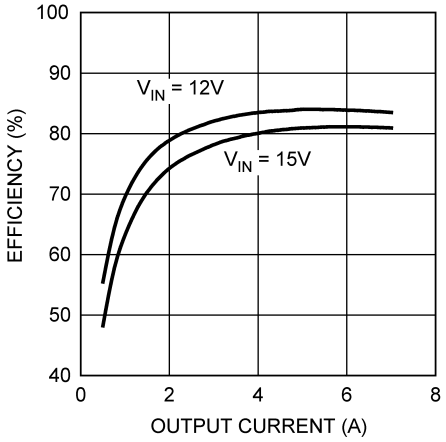


Figure 8.

Efficiency in FPWM Mode
V_O = 2.2V, I_O = 0.5A to 7A
BOM in Table 2

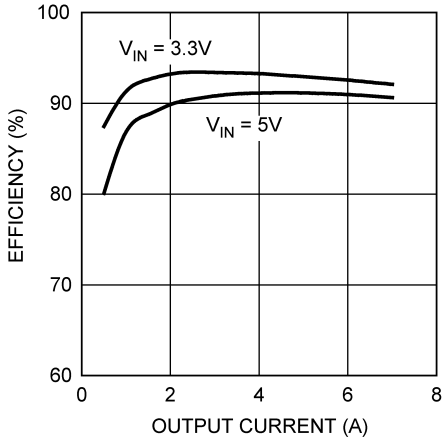


Figure 9.

Load Transient Response
V_{IN} = 3.3V, V_O = 2.2V
BOM in Table 2

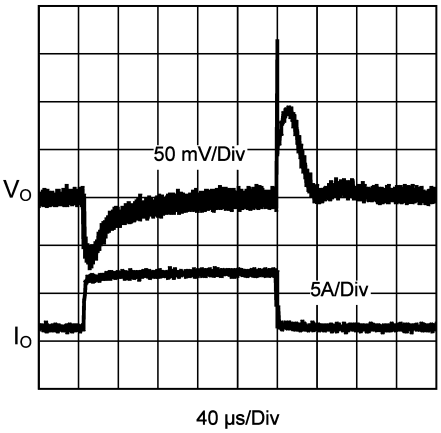


Figure 10.

Load Transient Response
V_{IN} = 12V, V_O = 1.0V
BOM in Table 1

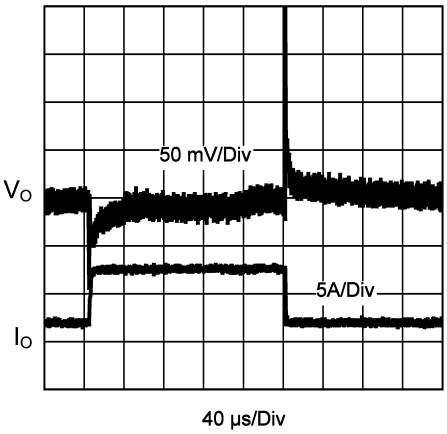


Figure 11.

Soft-Start in SKIP Mode
V_{IN} = 12V, V_O = 1.0V, I_O = 0A
BOM in Table 1

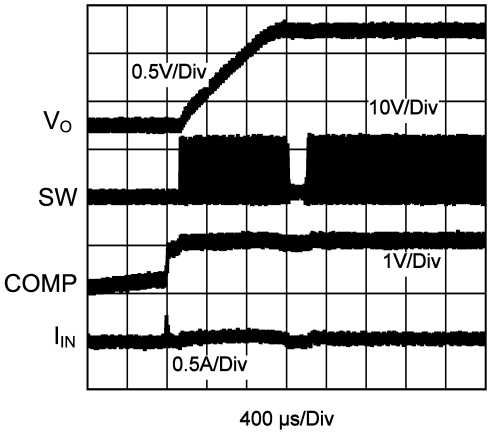


Figure 12.

Soft-Start in FPWM Mode
V_{IN} = 3.3V, V_O = 2.2V, I_O = 0A
BOM in Table 2

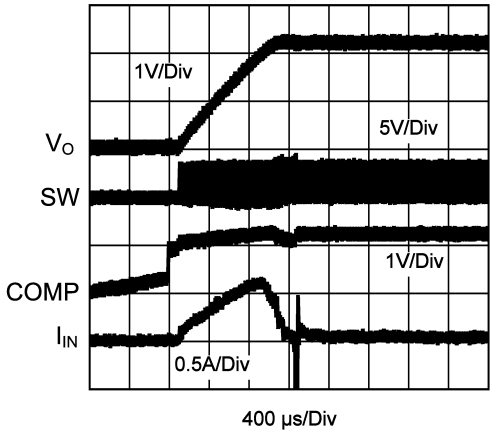


Figure 13.

Typical Performance Characteristics (continued)

V_{IN} = 12V unless specified, T_A = 25°C unless specified.

Soft-Start in FPWM Mode
V_{IN} = 12V, V_O = 1.0V, I_O = 5A
BOM in Table 1

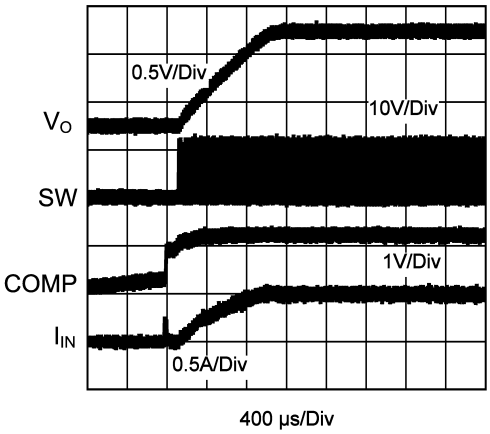


Figure 14.

Soft-Start in FPWM Mode
V_{IN} = 3.3V, V_O = 2.2V, I_O = 5A
BOM in Table 2

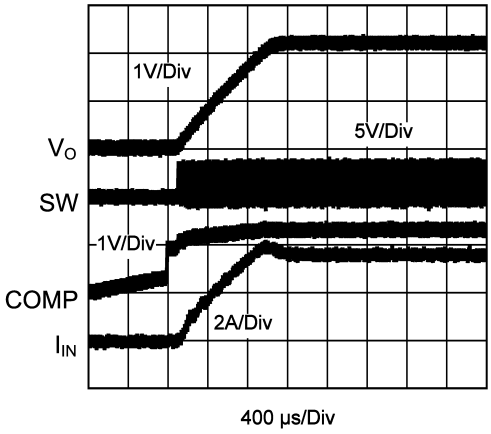


Figure 15.

Soft-Start with Output Pre-bias
V_{IN} = 12V, V_O = 1.0V, I_O = 0A
BOM in Table 1

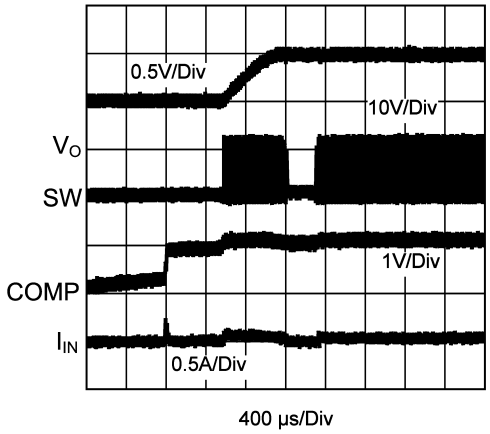


Figure 16.

Soft-Start with Output Pre-bias
V_{IN} = 3.3V, V_O = 2.2V, I_O = 0A
BOM in Table 2

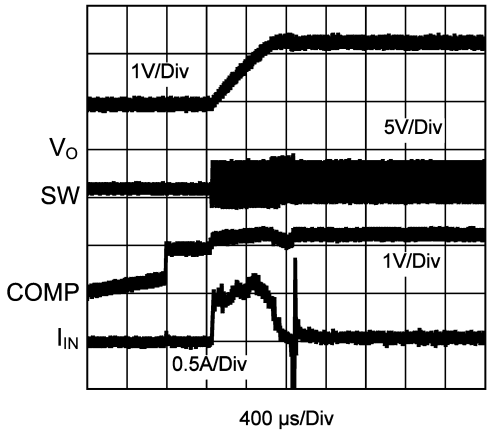


Figure 17.

Shutdown
V_{IN} = 12V, V_O = 1.0V, I_O = 0A
BOM in Table 1

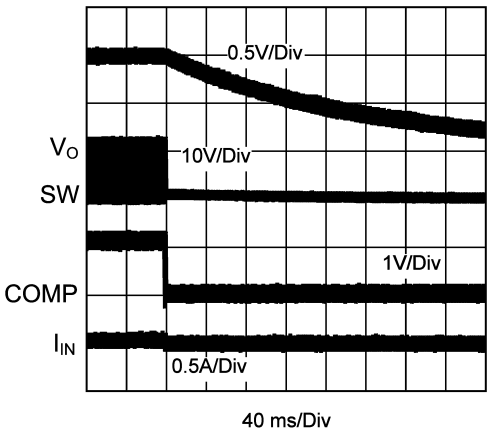


Figure 18.

Shutdown
V_{IN} = 12V, V_O = 1.0V, I_O = 5A
BOM in Table 1

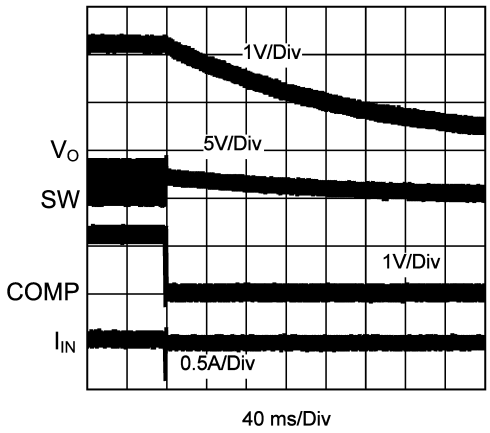


Figure 19.

Typical Performance Characteristics (continued)

V_{IN} = 12V unless specified, T_A = 25°C unless specified.

FA to SYNC Transition
Clock Starts on Logic Low
BOM in Table 1

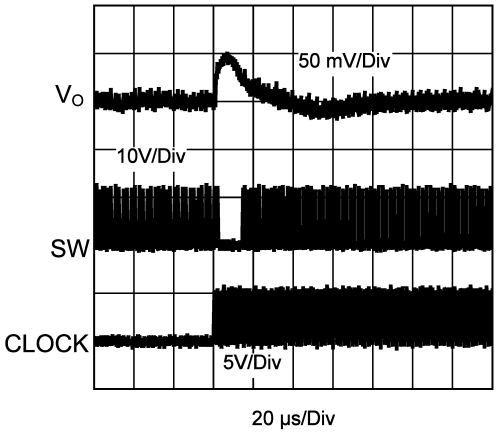


Figure 20.

FA to SYNC Transition
Clock Starts on Logic High
BOM in Table 1

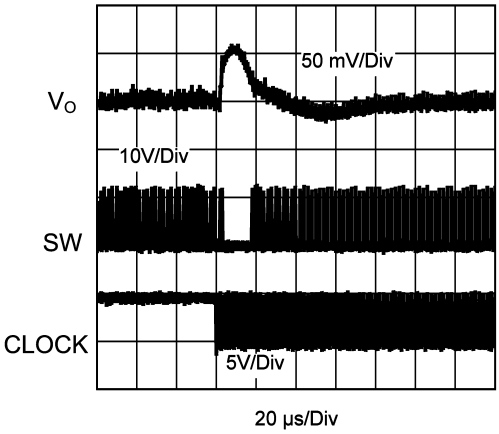


Figure 21.

SYNC to FA Transition
Clock Ends on Logic Low
BOM in Table 1

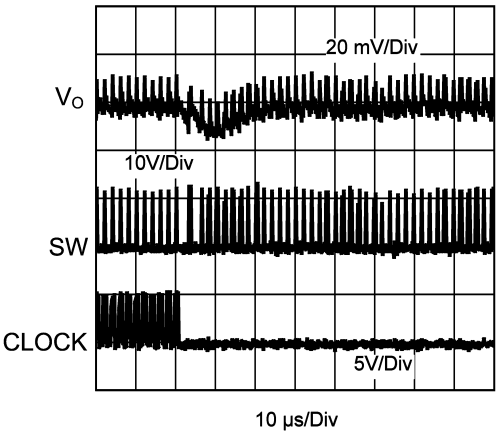


Figure 22.

SYNC to FA Transition
Clock Ends on Logic High
BOM in Table 1

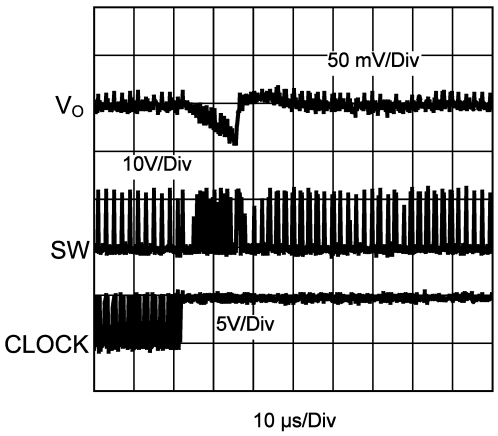


Figure 23.

Tracking With Equal Soft Start Time
V_{IN} = 12V, V_O = 1.0V, No Load
BOM in Table 1

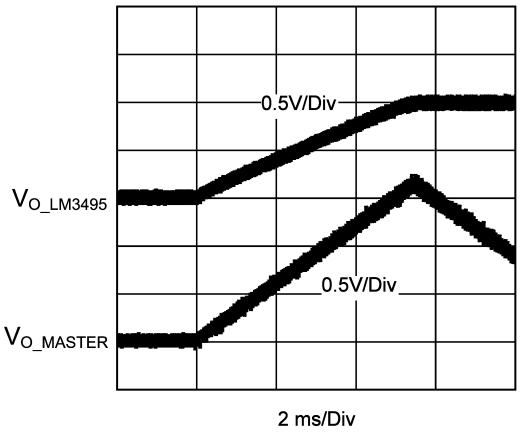


Figure 24.

Tracking With Equal Soft Start Time
V_{IN} = 5V, V_O = 2.2V, No Load
BOM in Table 2

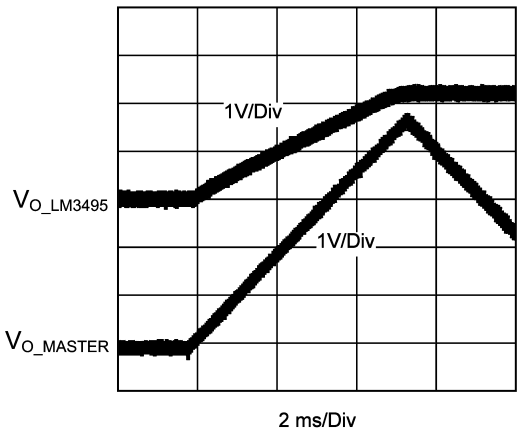


Figure 25.

Typical Performance Characteristics (continued)

V_{IN} = 12V unless specified, T_A = 25°C unless specified.

Tracking With Equal Slew Rate
V_{IN} = 12V, V_O = 1.0V, No Load
BOM in Table 1

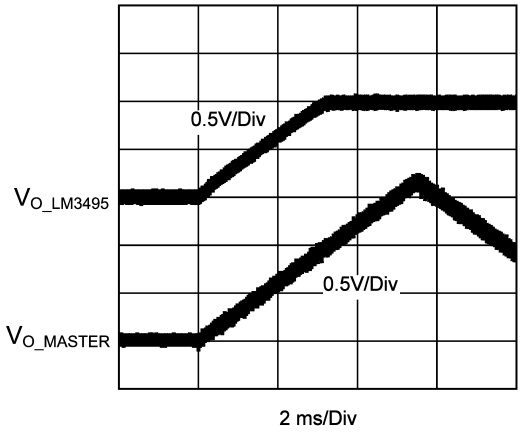


Figure 26.

Tracking With Equal Slew Rate
V_{IN} = 5V, V_O = 2.2V, No Load
BOM in Table 2

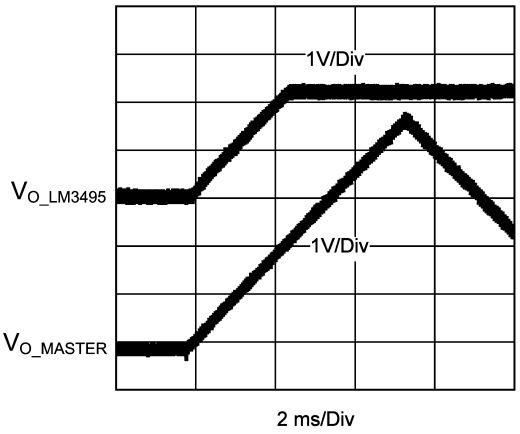


Figure 27.

SKIP to FPWM Transition
V_{IN} = 12V, V_O = 1.0V, I_O = 5A
BOM in Table 1

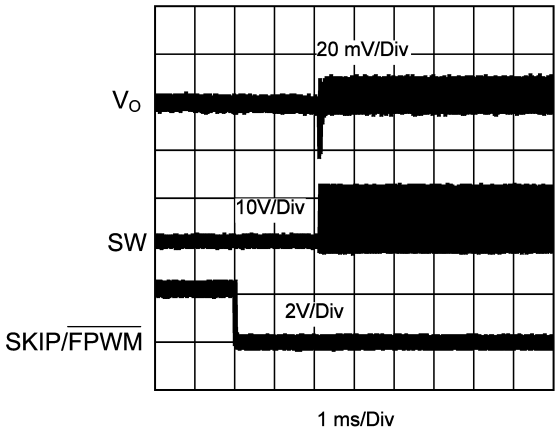


Figure 28.

f_{SW} vs R_{FRQ}
V_{IN} = 12V, V_O = 1.0V, No Load
BOM in Table 1

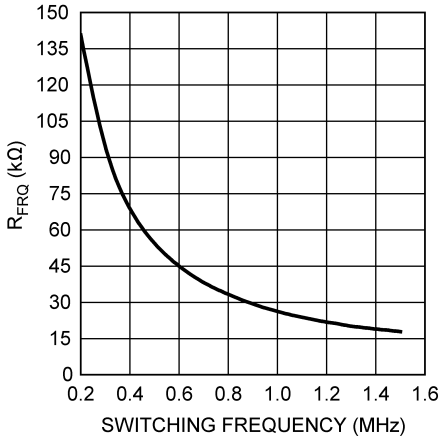
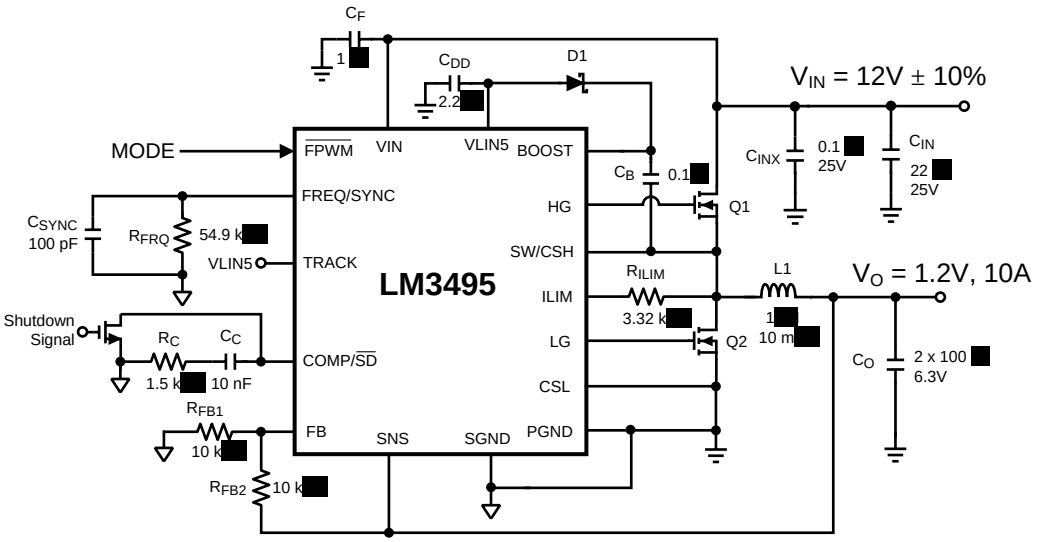
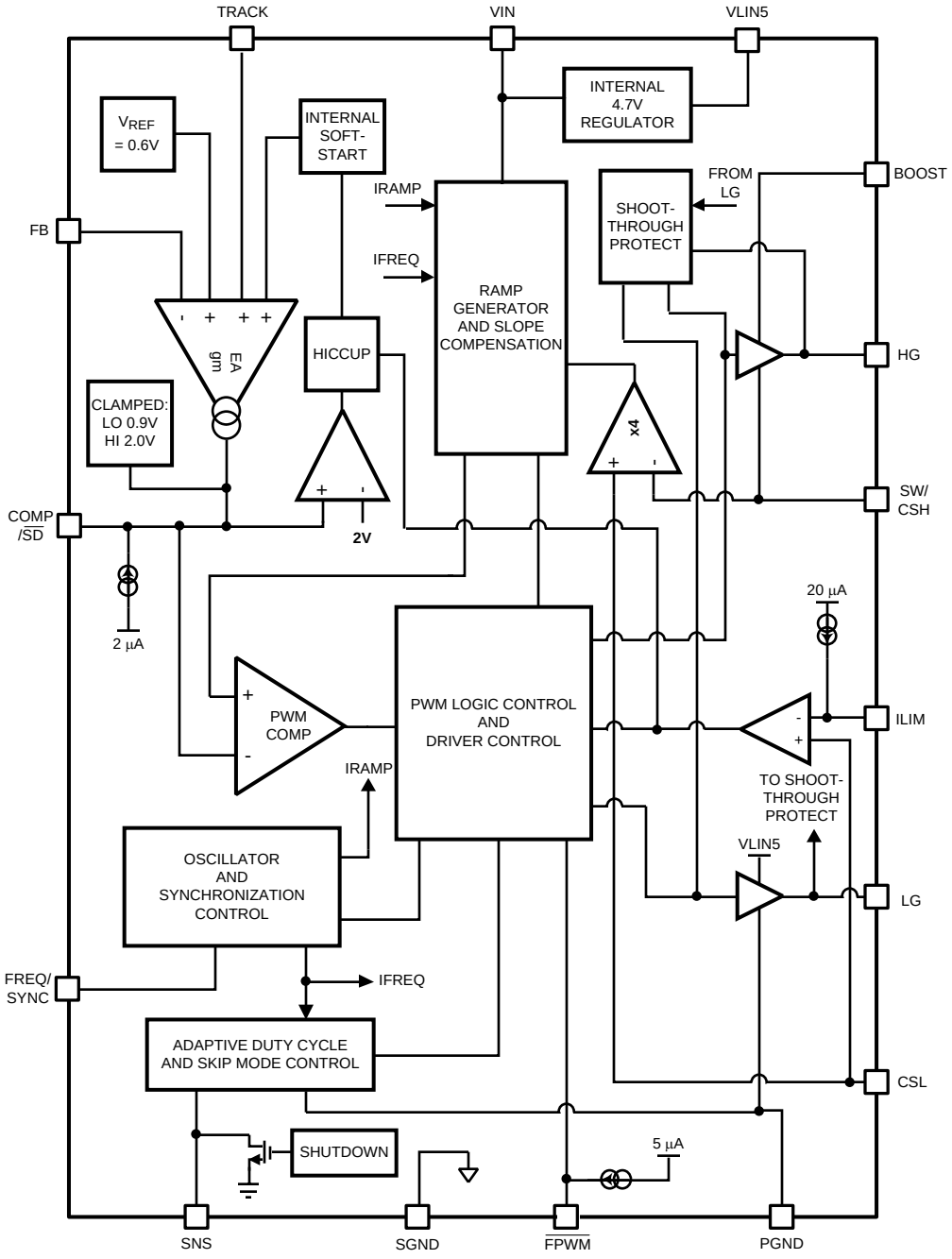


Figure 29.

Typical Application Circuit



Block Diagram



APPLICATIONS INFORMATION

THEORY OF OPERATION

The LM3495 is an advanced, current mode PWM synchronous controller. Unlike traditional peak current mode controllers which sense the current while the high-side FET is on, the LM3495 senses current while the low-side FET is on. The LM3495 then emulates the peak current waveform and uses that information to regulate the output voltage. High-side ON pulses as low as 50 ns are possible to achieve low duty cycle operation. The LM3495 therefore enjoys both excellent line transient response and the ability to regulate low output voltages from high input voltages.

START UP

The LM3495 will begin to operate when the COMP/$\overline{SD}$ pin is open-circuited and the voltage at the VIN pin has exceeded 2.6V. Once these two conditions have been met an internal soft start begins and lasts for 400 switching cycles. When soft start is complete the converter enters steady state operation. Current limit is enabled during soft start to protect against a short circuit at the output.

START UP INTO OUTPUT PRE-BIAS

If the output capacitor of the LM3495 regulator has been charged up to some pre-bias level before the converter is enabled, the soft start will ramp the output voltage from the pre-bias level up to the target output voltage without ever discharging the output capacitor. Note that the pre-bias voltage must not be greater than the target output voltage of the LM3495, otherwise the LM3495 will pull the pre-bias supply down during steady state operation. A zero-cross comparator prevents the current in the inductor from reversing during soft start and prevents discharge of the output capacitor through the low-side FET. In FPWM mode, once soft-start is complete the zero-cross threshold decreases over 16 cycles and then is disabled, allowing the converter to sink current at the output if needed.

The LM3495 contains an internal N-FET with an on-resistance of approximately 500Ω connected between the SNS and PGND pins. When the converter is disabled, this FET is turned on to discharge the output capacitor in a controlled fashion. If the LM3495 is used in a system with a pre-bias at the output the power supply providing the pre-bias must be able to supply enough current for the 500Ω load that the internal FET creates.

TRACKING

The LM3495 can track the output of a master power supply during soft start by connecting a resistor divider to the TRACK pin (Figure 30). In this way, the output voltage slew rate of the LM3495 will be controlled by the master supply for loads that require precise sequencing. Because the output of the master supply is divided down, the output voltage of the LM3495 must be lower than the voltage of the master supply in order to track properly. When the tracking function is not being used, the TRACK pin should be connected directly to the VLIN5 pin.

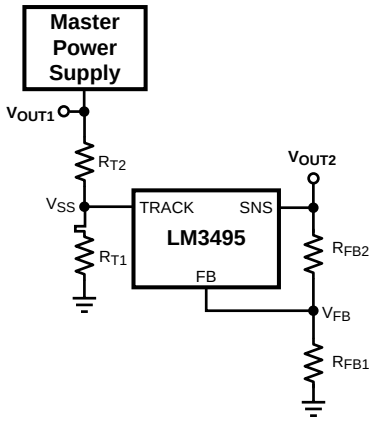


Figure 30. Tracking Circuit

One way to use the tracking feature is to design the tracking resistor divider so that the master supply output voltage (V_{OUT1}) and the LM3495 output voltage (V_{OUT2}) both rise together and reach their target values at the same time. For this case, the equation governing the values of the tracking divider resistors R_{T1} and R_{T2} is:

$$0.65V = V_{OUT1} \frac{R_{T1}}{R_{T1} + R_{T2}} \quad (1)$$

The above equation is set equal to 0.65V in order to ensure that the final value of the track pin voltage exceeds the reference voltage of the LM3495, and this 50 mV offset will cause the LM3495 output voltage to reach regulation slightly before the master supply. A value of 10 kΩ 1% is recommended for R_{T2} as a good compromise between high precision and low quiescent current through the divider. If the master supply voltage V_{OUT1} is 5V, for example, then the value of R_{T1} needed to give the two supplies identical soft start times would be 1.5 kΩ 1%. A timing diagram for this example, the equal soft start time case, is shown in Figure 31.

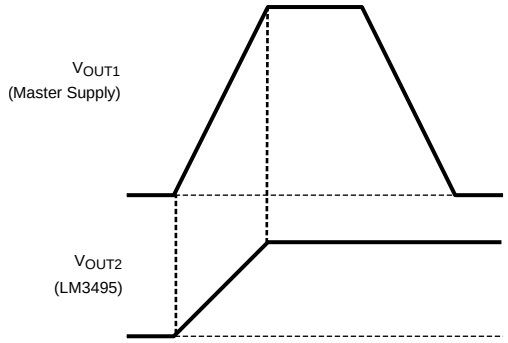


Figure 31. Tracking with Equal Soft Start Time

Alternatively, the tracking feature can be used to create equal slew rates between the output voltages of the LM3495 and the master supply. This method ensures that the output voltage of the LM3495 always reaches regulation before the output voltage of the master supply. In this case, the tracking resistors can be determined based on the following equation:

$$0.6V = V_{OUT2} \frac{R_{T1}}{R_{T1} + R_{T2}} \quad (2)$$

Again, a value of 10 kΩ 1% is recommended for R_{T2}. For the example case of V_{OUT1} = 5V and V_{OUT2} = 1.8V, R_{T1} would be 5.62 kΩ 1%. A timing diagram for this example, the case of equal slew rates, is shown in Figure 32.

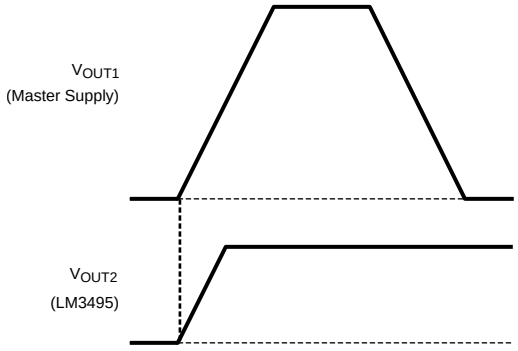


Figure 32. Tracking with Equal Slew Rates

FPWM MODE OPERATION

The LM3495 operates under forced PWM when the $\overline{FPWM}$ pin is connected to ground. While in FPWM operation, the LM3495 controls the output voltage by adjusting the duty cycle of the power FETs with trailing edge PWM. The output inductor and capacitor filter the square wave produced as the power FETs chop the input voltage, thereby creating a regulated output voltage. The DC level of the output voltage can be set anywhere from 0.6V up to 5.5V, and is determined by a pair of feedback resistors using the following equation:

$$V_O = 0.6V \times \frac{R_{FB1} + R_{FB2}}{R_{FB1}} \quad (3)$$

In steady state FPWM mode, the inductor current can flow from the drain to the source of the low-side FET, keeping the converter in continuous conduction mode (CCM) at all times. CCM has the advantage of constant frequency and nearly constant duty cycle ($D = V_O/V_{IN}$) over all load conditions, and it allows the converter to sink current at the output if needed.

The switching frequency of the internal oscillator is set by a resistor, R_{FRQ}, connected from the FREQ/SYNC pin to ground. The proper resistor for a desired switching frequency, f_{SW}, can be determined by using the following equation:

$$R_{FRQ} = \frac{25.26 \times 10^3}{f_{SW} - 48.4} \ k\Omega, \ f_{SW} \text{ in kHz} \quad (4)$$

SKIP MODE OPERATION

If the $\overline{FPWM}$ pin is left open-circuited, the LM3495 can enter into SKIP mode operation, delivering better efficiency at light loads. As long as the inductor current is positive (flowing from the switch node to the output node), SKIP mode is identical to FPWM mode. Once the inductor current becomes negative, however, an internal zero-cross comparator will disable the low-side FET. This 'diode-emulation' mode allows the converter to operate in discontinuous conduction mode (DCM). In DCM, the duty cycle decreases as the load current decreases. A minimum on-time comparator prevents the duty cycle during DCM from decreasing below 80% of the steady state duty cycle, D. The converter will allow one on-time pulse, causing the output voltage to rise and the COMP/$\overline{SD}$ voltage to droop. If COMP/$\overline{SD}$ drops below the skip cycle comparator threshold of 1.05V, the control logic will disable the high-side FET for one cycle, effectively skipping a pulse. This skipping action continues until the COMP/$\overline{SD}$ voltage rises above the skip cycle threshold. Multiple pulses can be skipped depending on load, input voltage, and output voltage. Switching frequency is not fixed during SKIP Mode, but energy is saved because the high and low-side FETs are driven less frequently than in FPWM mode. In SKIP mode the regulator cannot sink current at the output.

SKIP TO FPWM TRANSITION

The LM3495 employs circuitry to transition from SKIP mode to FPWM mode with minimal discontinuity in inductor current and output voltage. When the $\overline{FPWM}$ pin is grounded, the threshold of the zero-cross comparator decreases from 0V to -9.9 mV over fifteen switching cycles. After fifteen cycles have elapsed, the zero-cross comparator is disabled entirely and the circuit switches to FPWM mode.

Note that "on-the-fly" changes from FPWM mode to SKIP mode are not recommended due to the possibility of discontinuity in the inductor current and/or output voltage.

FREQUENCY SYNCHRONIZATION

The switching action of the LM3495 can be synchronized to external clocks or other fixed frequency signals in the range of 200 kHz to 1.5 MHz. The external clock should be applied through a 100 pF coupling capacitor, C_{SYNC}, as shown in Figure 33. In order for the LM3495 to synchronize properly, the external clock should exceed 1.2V on each rising edge and remain above 1.2V for at least 100 ns.

The external clock should also fall below 0.3V on each falling edge, and remain below 0.3V for at least 100 ns. Circuits that use an external clock should still have a resistor, R_{FRQ}, connected from the FREQ/SYNC pin to signal ground. R_{FRQ} should be selected using the equation from FPWM MODE OPERATION to match the external clock frequency. This allows the regulator to continue operating at approximately the same switching frequency if the external clock fails and the coupling capacitor on the clock side is grounded or pulled to a logic high.

If the external clock fails low, timeout circuits will prevent the high-side FET from staying off for longer than 1.5 times the switching period (Switching period T_{SW} = 1/f_{SW}). At the end of this timeout period the regulator will begin to switch at the frequency set by R_{FRQ}.

If the external clock fails high, timeout circuits will again prevent the high-side FET from staying off longer than 1.5 times the switching period. After this timeout period, the internal oscillator takes over and switches at a fixed 1 MHz until the voltage on the FREQ/SYNC pin has decayed to approximately 0.6V. This decay follows the time constant of C_{SYNC} and R_{FRQ}, and once it is complete the regulator will switch at the frequency set by R_{FRQ}.

Care must be taken to prevent errant pulses from triggering the synchronization circuitry. In applications that will not synchronize to an external clock, C_{SYNC} should be connected from the FREQ/SYNC pin to signal ground as a noise filter. When a clock pulse is first detected, the LM3495 begins switching at the external clock frequency. Noise or a short burst of clock pulses can result in off times as long as 7.5 µs for the high-side FET if they occur while the internal synchronization circuits are adjusting.

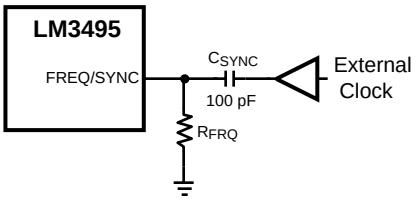


Figure 33. Clock Synchronization Circuit

MOSFET GATE DRIVE

The LM3495 has two gate drivers designed for driving N-channel MOSFETs in a synchronous mode. Power for the high-side driver is supplied through the BOOST pin. For the high-side gate drive to fully turn on the top FET, the BOOST pin voltage must be at least one threshold voltage, $V_{GS(th)}$, greater than V_{IN}. This voltage is supplied from a local charge pump structure which consists of a Schottky diode and 0.1 µF capacitor, shown in Figure 34.

Both the bootstrap and the low-side FET driver are fed from VLIN5, which is the output of a 4.7V internal linear regulator. This regulator has a dropout voltage of approximately 1V. If V_{IN} drops below 4V, an internal switch shorts the VIN and VLIN5 pins together. The drive voltage for the top FET driver is therefore VLIN5-V_D, where V_D is the drop across the Schottky diode D1. This information is needed to select the type of MOSFETs to be used.

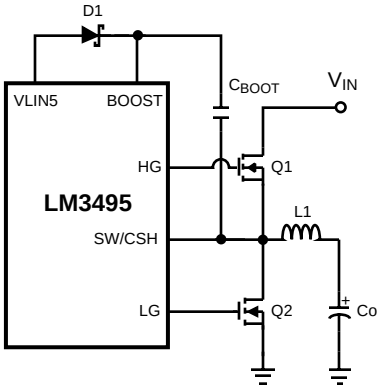


Figure 34. Bootstrap Circuit

INPUT VOLTAGE BELOW 5.5V

The LM3495 includes an internal 4.7V linear regulator connected from the VIN pin to the VLIN5 pin. This linear regulator feeds the logic and FET drive circuitry. For input voltages less than 5.5V, the VIN and VLIN5 pins can be shorted together externally. The external short circuit bypasses both the internal linear regulator and the internal PMOS switch, allowing the full input voltage to be used for driving the power FETs and minimizing conduction loss in the LM3495 itself. For voltage inputs that range above and below 5.5V the LM3495 must not use a short from VIN to VLIN5.

UNDER VOLTAGE LOCK-OUT

The 2.6V turn-on threshold on the voltage at VIN has a built in hysteresis of 300 mV. If input voltage drops below 2.3V the chip enters under voltage lock-out (UVLO) mode. UVLO consists of turning off both the top and bottom FETs and remaining in that condition until input voltage rises above 2.6V.

BOOTSTRAP DIODE SELECTION

Schottky diodes are the preferred choice for the bootstrap circuit because of their low forward voltage drop. For circuits that will operate at high ambient temperature the Schottky diode datasheet must be read carefully to ensure that the reverse leakage current at high temperature does not increase enough to deplete the charge on the bootstrap capacitor while the high-side FET is off. Some Schottky diodes increase their reverse leakage by as much as 1000x at their upper temperature limit. Fast recovery and PN junction diodes maintain low reverse leakage even at high ambient temperature. For high ambient temperature operation Schottky diodes with low leakage across temperature or fast recovery type diodes should be used.

OVER VOLTAGE PROTECTION

The LM3495 will shut down if the output voltage exceeds 125% of the steady state target voltage for longer than 4 µs. The high-side FET is turned off and the low-side FET is turned on. The LM3495 will remain in this condition until either the VIN pin voltage is cycled to ground, or the COMP/$\overline{SD}$ pin voltage is pulled to below 0.3V and then released. Either of these reset mechanisms will cause the device to perform a soft-start.

LOW-SIDE CURRENT LIMIT

The current limit of the LM3495 operates by sensing the current in the low-side FET while the load current, I_O, circulates through it. The low-side FET drain-to-source voltage, V_{DS}, is compared against the voltage of a fixed, internal 20 µA current source and a user-selected resistor, R_{ILIM}. The value of R_{ILIM} for a desired current limit threshold, I_{CL}, can be selected with the following equation:

$$R_{ILIM} = \frac{I_{CL} \times R_{DSON\text{-}LO}}{20\ \mu A} \tag{5}$$

R_{ILIM} is connected between the switch node and the ILIM pin. A current limit event is sensed when V_{DS} exceeds V_{ILIM}. **(V_{ILIM} = 20 µA x R_{ILIM})**. The high-side switch is disabled for the following cycle and the low-side FET is kept on during this time.

During long duration current limit conditions or a short circuit the output voltage droops. This in turn causes the COMP/$\overline{SD}$ pin voltage to rise. If the COMP/$\overline{SD}$ pin voltage exceeds 2V and a high-side FET on-pulse is skipped, the LM3495 increments a 4 bit counter. If 16 high-gate pulses are skipped consecutively while COMP/$\overline{SD}$ stays above 2V, the LM3495 will enter hiccup mode. The counter is reset when the COMP/$\overline{SD}$ pin goes below 2V. During soft-start the cycle skipping function of the low-side current limit is active, but the ability to enter hiccup mode is disabled.

CURRENT LIMIT SENSE RESISTOR

For applications that require a higher degree of accuracy for the low-side current limit, a dedicated current sense resistor can be added between ground and the source of the low-side FET. Figure 35 shows the circuit connection when using a dedicated current limit sensing resistor, R_{SNS}.

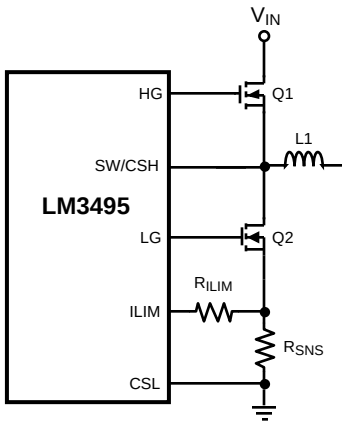


Figure 35. Current Limit Sense Resistor

When using a dedicated current limit sensing resistor, the equation governing the low-side current limit becomes:

$$R_{ILIM} = \frac{I_{CL} \times R_{SNS}}{20\ \mu A} \tag{6}$$

MAXIMUM CURRENT SENSE

In order to keep the low-side current sense amplifier within its linear range, the peak sense voltage, V_{SNS}, between the CSL and SW/CSH pins should remain below 200 mV.

$$V_{SNS} = I_{PK} \times (R_{DSON-LO} + R_{SNS}) \tag{7}$$

The value I_{PK} can be determined by following the equations in the Output Inductor.

HIGH-SIDE CURRENT LIMIT

The LM3495 employs a second comparator that monitors the voltage across the high-side FET when it is on. This provides protection against a short circuit at the switch node, which the low-side current limit cannot detect. If the drain-to-source voltage of the high-side FET exceeds 500 mV while the FET is on, the LM3495 will immediately enter hiccup mode. A 200 ns blanking period after the high-side FET turns on is used to prevent switching transient voltages from tripping the high-side current limit without cause.

HICCUP MODE

During hiccup mode, the LM3495 disables both the high-side and low-side FETs and begins a cool down period of 4096 switching cycles. At the conclusion of this cool down period, the regulator performs an internal 400 cycle soft start identical to the soft start at turn-on. During soft start only the high-side current limit can put the LM3495 into hiccup mode. low-side current cannot put the LM3495 into hiccup mode during soft start, although it can limit duty cycle. If a short at the output persists when soft start is done, the part will begin counting high-side pulses skipped due to the low-side current limit and will re-enter hiccup mode 16 cycles later. The long term effect observed will be 4096 cycles with the power FETs disabled, and then 416 (400 + 16) cycles where they are enabled.

The hiccup protection mode is designed to protect the external components of the circuit (output inductor, FETs and input voltage source) from thermal stress. For example, assume that the low–side current limit is10A. Once in hiccup mode the effective duty cycle for the high-side FET and output inductor will be D*(416/4096). For the low-side FET it will be (1-D)(416/4096). This means that even under the worst case conditions (minimum switching frequency and maximum duty cycle, D_{MAX} = 96%), the average current through the inductor and high-side FET will be 975 mA and the average current seen by the low-side FET will be 40 mA.

PARALLEL LOW-SIDE SCHOTTKY DIODE

Many synchronous buck regulators include a Schottky diode in parallel with the low-side power FET. The low forward drop and short reverse recovery time of Schottky diodes can improve efficiency by preventing the FET's body diode from turning on. This technique is most effective in circuits with output currents of 5A or less. The parallel Schottky diode must be placed as close as possible to the power FET to prevent trace inductance from negating the gains in efficiency.

ADAPTIVE DUTY CYCLE CLAMP

The adaptive duty cycle clamp is an extra layer of protection used during high current conditions or large load transients. When a high-side pulse is skipped due to current limit, the output voltage tends to decrease rapidly. The steady state control loop of the LM3495 responds by commanding a higher duty cycle at the next high-side turn-on. The result is a combination of high voltage across the output inductor and long duty cycles that could result in inductor saturation. The adaptive duty cycle clamp prevents inductor saturation by providing a dynamic maximum duty cycle, D_{CLAMP}. The clamp is based on the sensed input and output voltages. D_{CLAMP} can be predicted with the following equation:

$$D_{CLAMP} = 3.2 \times \frac{V_O}{V_{IN}} \quad (8)$$

D_{CLAMP} cannot exceed 100% (9)

SHUTDOWN

The LM3495 can be put into a low power shutdown mode by bringing the voltage at the COMP/$\overline{SD}$ pin below 0.3V. A signal-level BJT or FET can be controlled by most CMOS or TTL logic signals to perform this function. The collector-to-emitter or drain-to-source capacitance should be less than 20 pF to minimize the effect on the control loop compensation. During shutdown, both the high-side and low-side FETs are disabled. The output voltage is discharged through the SNS pin by an internal 500Ω FET.

THERMAL SHUTDOWN

The LM3495 will enter a thermal shutdown state if the die temperature exceeds 150°C. Both the high-side and low-side power FETs are turned off, the output voltage is discharged through an internal 500Ω FET, and the IC will remain in this condition until the die temperature has dropped to approximately 135°C. At this point the LM3495 will perform a soft-start.

Design Considerations

The most common circuit controlled by the LM3495 is a non-isolated, synchronous buck regulator. The buck regulator steps down the input voltage and has a duty cycle, D, of:

$$D = \frac{V_O}{V_{IN}} \quad (10)$$

The following is a design procedure for selecting all the components in the Typical Application circuit on the front page. This circuit delivers a 1.2V ± 1% output voltage at output currents up to 10A from an input voltage of 12V ± 10%. This circuit is typical of a point-of-load (POL) module. A BOM for this typical application is listed in Table 3 at the end of this datasheet.

SWITCHING FREQUENCY

The selection of switching frequency is based on the tradeoffs between size, cost, and efficiency. In general, a lower frequency means larger, more expensive inductors and capacitors will be needed. A higher switching frequency generally results in a smaller but less efficient solution, as the power FET gate capacitances must be charged and discharged more often in a given amount of time. For this application, a frequency of 500 kHz was selected because the space on a POL circuit board is limited. This frequency is a good compromise between the size of the inductor and FETs, transient response, and efficiency. Following the equation given for R_{FRQ} in the Applications Information section, a 54.9 kΩ 1% resistor should be used to switch at 500 kHz.

MOSFETS

Selection of the power FETs is governed by the same tradeoffs as switching frequency. Breaking down the losses in the high-side and low-side FETs is one way to determine relative efficiencies between different FETs. When using discrete SO-8 FETs the LM3495 is most efficient for output currents of 2A to 10A.

Losses in the power FETs can be broken down into conduction loss, gate charging loss, and switching loss.

Conduction, or I^2R loss, P_C, is approximately:

$$P_C = D \ (I_O^2 \times R_{DSON\text{-}HI} \times 1.3) \text{ (High-Side MOSFET)} \quad (11)$$

$$P_C = (1 - D) \times (I_O^2 \times (R_{DSON\text{-}LO} \times 1.3 + R_{SNS})) \text{ (Low-Side MOSFET)} \quad (12)$$

In the above equations $R_{DSON\text{-}HI}$ and $R_{DSON\text{-}LO}$ refer to on-resistance of the high-side and low-side FETs, respectively. R_{SNS} is 0 if it is not used. The factor 1.3 accounts for the increase in FET on-resistance due to heating. Alternatively, the factor of 1.3 can be ignored and the on-resistance of the FET can be estimated using the R_{DSON} vs Temperature curves in the FET datasheets. Gate charging loss, P_{GC}, results from the current driving the gate capacitance of the power FETs and is approximated as:

$$P_{GC} = n \times (V_{LIN5} - V_D) \times Q_{G\text{-}HI} \times f_{SW} \text{ (High-Side MOSFET)} \quad (13)$$

$$P_{GC} = n \times V_{LIN5} \times Q_{G\text{-}LO} \times f_{SW} \text{ (Low-Side MOSFET)} \quad (14)$$

In the above equations $Q_{G\text{-}HI}$ and $Q_{G\text{-}LO}$ refer to the gate charge of the high-side and low-side FETs, respectively. The factor 'n' is the number of FETs (if multiple devices have been placed in parallel) and Q_G is the total gate charge of the FET. If different types of FETs are used, the 'n' term can be ignored and their gate charges summed to form a cumulative Q_G. Gate charge loss differs from conduction and switching losses in that the actual dissipation occurs in the LM3495 and not in the FET itself. Further loss in the LM3495 is incurred as the gate driving current passes through the internal linear regulator. This loss term is factored into the Chip Operating Loss portion of the Efficiency Calculations section.

Switching loss, P_{SW}, occurs during the brief transition period as the FET turns on and off. During the transition period both current and voltage are present in the channel of the FET. The loss can be approximated as:

$$P_{SW} = 0.5 \times V_{IN} \times I_O \times (t_R + t_F) \times f_{SW} \quad (15)$$

Where t_R and t_F are the rise and fall times of the FET. Switching loss is calculated for the high-side FET only. Switching loss in the low-side FET is negligible because the body diode of the low-side FET turns on before the FET itself, minimizing the voltage from drain to source before turn-on.

For this example, the maximum drain-to-source voltage applied to either FET is 13.2V. The maximum drive voltage at the gate of the high-side FET is 4.5V, and the maximum drive voltage for the low-side FET is 5V. Any FET selected must be able to withstand 13.2V plus any ringing from drain to source, and be able to handle at least 5V plus ringing from gate to source. One good choice of FET for the high-side has an R_{DSON} of 9.6 mΩ, total gate charge Q_G of 11 nC, and rise and fall times of 5 and 8 ns, respectively. For the low-side FET, a good choice has an R_{DSON} of 3.4 mΩ and gate charge of 33 nC. These values have been taken from the FET datasheets with a V_{GS} of 4.5V.

OUTPUT INDUCTOR

The first criterion for selecting an output inductor is the inductance itself. In most buck converters, this value is based on the desired ripple current, Δi_O, which flows in the inductor along with the load current. This ripple current will flow through the ESR and impedance of the output capacitor to create the output voltage ripple, Δv_O. Due to the unique control architecture of the LM3495, a second requirement for minimum inductance must be used based on the R_{DSON} of the low-side FET and the desired switching frequency. As with switching frequency, the inductance used is a tradeoff between size and cost. Larger inductance means low current ripple and hence low output voltage ripple. However, less inductance results in smaller, less expensive devices. An inductance that gives a ripple current of 30% to 40% of the maximum load current is a good starting point (Δi_O = 30% to 40%*I_O). Minimum inductance should be calculated from this value, using the maximum input voltage, as:

$$L_{MIN1} = \frac{V_{IN(MAX)} - V_O}{f_{SW} \times \Delta i_O} \times D \quad (16)$$

By calculating in terms of amperes, volts, and megahertz, the inductance value will come out in micro henries. The second minimum inductance equation specific to the LM3495 is:

$$L_{MIN2} = \frac{64 \times (R_{DSON\text{-}LO} + R_{SNS})}{f_{SW}} \times \frac{V_{IN}}{V_{IN} + 2} \quad (17)$$

By calculating in terms of milliohms and kilohertz the inductance value will come out in micro henries.

For this design:

$$L_{MIN1} = \frac{13.2V - 1.2V}{500\ kHz \times 3A} \times 0.1 = 0.8\ \mu H$$

$$L_{MIN2} = \frac{64 \times 3.4\ m\Omega}{500\ kHz} \times \frac{12V}{12V + 2} = 0.4\ \mu H \quad (18)$$

Whichever equation gives the higher value for inductance is the one which should be followed.

The second criterion for selecting an inductor is the peak current carrying capability. This is the level above which the inductor will saturate. In saturation the inductance drops off severely, often to 20% to 30% of the rated value. In a buck converter, peak current, I_{PK}, is equal to the maximum load current plus one half of the ripple current. For this example:

$$I_{PK} = 10A + 1.5A = 11.5A \quad (19)$$

Hence an inductor must be selected that has a peak current rating greater than 11.5A and an average current rating greater than 10A. To ensure a robust design, the inductor selected should maintain approximately 50% of its rated inductance during the worst-case peak current from an output short circuit. For a low-side current limit the peak current during an output short circuit can be estimated as I_{CL} plus $\Delta i_{(O\text{-}MAX)}$. $\Delta i_{(O\text{-}MAX)}$ is calculated by substituting zero for output voltage in the expression for Δi_O. Inductor core materials with soft saturation characteristics are preferred. One inductor that meets the peak current guidelines is an off-the-shelf 1.0 µH component that can handle a peak current of 18A and an average current of 14A. The inductor current ripple and peak inductor current should be recalculated for the selected inductance value, L_{ACTUAL}, by rearranging the equation for minimum inductance:

$$\Delta i_O = \frac{V_{IN(max)} - V_O}{f_{SW} \times L_{ACTUAL}} \times D$$

$$\Delta i_O = \frac{13.2V - 1.2V}{0.5\ MHz \times 1\ \mu H} \times 0.1 = 2.4A_{P\text{-}P}$$

$$I_{PK} = 10A + 2.4A/2 = 11.2A \quad (20)$$

OUTPUT CAPACITOR

The output capacitor in a switching regulator is selected on the basis of capacitance, equivalent series resistance (ESR), size, and cost. An important specification in switching converters is the output ripple voltage, Δv_O. At 500 kHz the impedance of most capacitors is very small compared to ESR, hence ESR becomes the main selection guide. In this design the load requires a 1% ripple, which results in a Δv_O of 10 $mV_{P\text{-}P}$. Maximum ESR is then:

$$ESR_{MAX} = \frac{\Delta V_O}{\Delta i_O} \quad (21)$$

ESR_{MAX} is 10 mΩ. Multi-layer ceramic, aluminum electrolytic, tantalum, solid aluminum, organic, and niobium capacitors are all popular in switching converters. Generally, by the time enough capacitors have been paralleled to obtain the desired ESR, the bulk capacitance is more than enough to supply the load current during a transient from no-load to full load. In this example the load could transition quickly from 0A to 5A, (or from 5A to 0A), so moderate bulk capacitance is needed. Two MLCC capacitors rated 100 µF, 6.3V each with ESR of 1.5 mΩ will work well.

VLIN5 DECOUPLING CAPACITOR

The VLIN5 pin should always be decoupled with a 2.2 µF, 10V-rated ceramic capacitor placed as close as possible to the VLIN5 and PGND pins of the LM3495. The decoupling capacitor should have a minimum X5R or X7R type dielectric to ensure that the capacitance remains stable over the expected voltage and temperature range.

INPUT CAPACITOR

The input capacitors to a buck regulator are used to smooth the large current pulses drawn by the inductor and load when the high-side FET is on. Due to this large AC stress, input capacitors are usually selected on the basis of their AC rms current rating rather than bulk capacitance. Low ESR is beneficial because it reduces the power dissipation in the capacitors. Although any of the capacitor types mentioned in the OUTPUT CAPACITOR section can be used, MLCCs are common because of their low ESR and because in general the input to a buck converter does not require as much bulk capacitance as the output. Input current, I_{rms}, can be calculated using the following equation:

$$I_{rms} = I_O \times \sqrt{D(1 - D)} \tag{22}$$

A good estimate for the maximum AC rms current is one-half of the maximum load current. For this example, the rms input current can be estimated as 3.5A. Regardless of the type and number of capacitors used, every design will benefit from the addition of a 0.1 µF to 1 µF ceramic capacitor placed as close as possible to the drain of the high-side FET and the source of the low-side FET.

In most applications for POL power supplies, the input voltage is the output of another switching converter. This output often has a lot of bulk capacitance. One 22 µF MLCC provides enough local smoothing and keeps the input impedance high enough to prevent power supply interaction from the source. For switching power supplies, the minimum quality dielectric that should be used is X5R. The preferred capacitor voltage rating for a 12V input voltage is 25V, due to the drop-off in capacitance of MLCCs under a DC bias. Capacitors with a 16V rating can still be used if size and cost are limiting factors. For this example the current rating of each of the capacitors should be at least 3Arms. The ESR of large-value ceramic caps is usually below 10 mΩ, which keeps the heating to a minimum.

CURRENT LIMIT

For this design, the trip point for the current limit circuitry should be below the peak current rating of the output inductor, which is 18A. To account for the tolerance of the internal current source, the change in the R_{DSON} of the low-side FET, and to prevent excessive heating of the inductor, a target of 15A has been chosen. A 3.8A margin exists between the expected 11.2A peak current and the current limit threshold to allow for line and load transients. Following the equation from the Applications Information section the value used for R_{LIM} should be 3.32 kΩ 1%.

CONTROL LOOP COMPENSATION

The LM3495 uses emulated peak current-mode PWM control to correct changes in output voltage due to line and load transients. This unique architecture combines the fast line transient response of peak current mode control with the ability to regulate at very low duty cycles. As a further advantage, the small signal characteristics of emulated peak current mode control are almost identical to those of traditional peak current mode control, and hence compensation can be selected using nearly identical calculations.

The control loop is comprised of two parts. The first is the power stage, which consists of the duty cycle modulator, output filter, and the load. The second part is the error amplifier, which is a transconductance (g_M) amplifier with a typical transconductance of 750 µmho and a typical output impedance of 72 MΩ. Figure 36 shows the regulator and voltage control loop components.

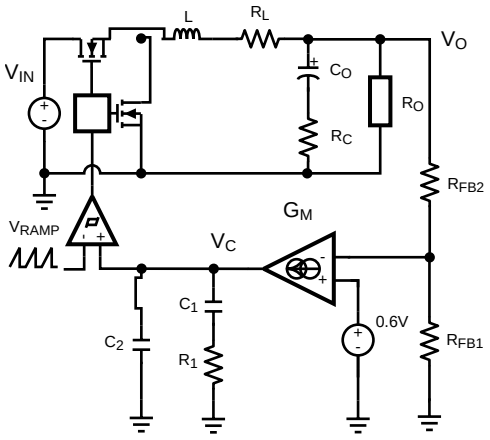


Figure 36. Power Stage and Error Amp

One popular method for selecting the compensation components is to create Bode plots of gain and phase for the power stage and error amplifier. Combined, they make the overall bandwidth and phase margin of the regulator easy to determine. Software tools such as Excel, MathCAD, and Matlab are useful for observing how changes in compensation or the power stage affect system gain and phase.

The power stage in an emulated peak current mode buck converter consists of the DC gain, A_{PS}, a low frequency pole, f_P, the ESR zero, f_Z, and a higher frequency pole, f_L, set by the ratio of the sensed current ramp to the emulated current ramp. The power stage transfer function (also called the Control-to-Output transfer function) can be written:

$$G_{PS} = A_{PS} \times \frac{1 + \frac{s}{\omega_Z}}{\left(1 + \frac{s}{\omega_P}\right)\left(1 + \frac{s}{\omega_L}\right)} \tag{23}$$

Where the DC gain is defined as:

$$A_{PS} = \frac{R_O}{G_I \times R_S} \times \frac{1}{1 + \frac{(R_O + R_L) \times (m_C - 0.5)}{L1 \times f_{SW}}}$$

where

- $R_S = R_{DSON\text{-}LO} + R_{SNS}$
- $m_C = S_e / S_n$
- $G_I = 4$

(24)

$$S_e = \left(\frac{V_{IN}}{16} + 0.125\right) \times f_{SW} \tag{25}$$

$$S_n = \frac{V_{IN} \times G_I \times R_S}{L1} \tag{26}$$

$$\omega_Z = \frac{1}{R_C \times C_O} \tag{27}$$

The low frequency pole is:

$$\omega_P = \frac{1}{R_O \times C_O} + \frac{m_C - 0.5}{L \times C_O \times f_{SW}} \tag{28}$$

And the higher frequency pole is:

$$\omega_L = \frac{f_{SW}}{m_C - 0.5} \tag{29}$$

In the equation for A_{PS}, the output resistance, R_O, is the output voltage divided by output current. DC gain is highest when output current is lowest. In order to design for the worst case, R_O should be calculated for the minimum load current. For this example, no minimum load has been specified, so a load of 100 mA will be used (R_O = 12Ω).

For this example, the value of DC gain is 24dB. The low frequency pole $f_P = \omega_P / 2\pi$ is at 2.7kHz, the ESR zero $f_Z = \omega_Z / 2\pi$ is at 1.06 MHz, and the higher frequency pole is at 48 kHz. Gain and phase plots for the power stage are shown in Figure 37.

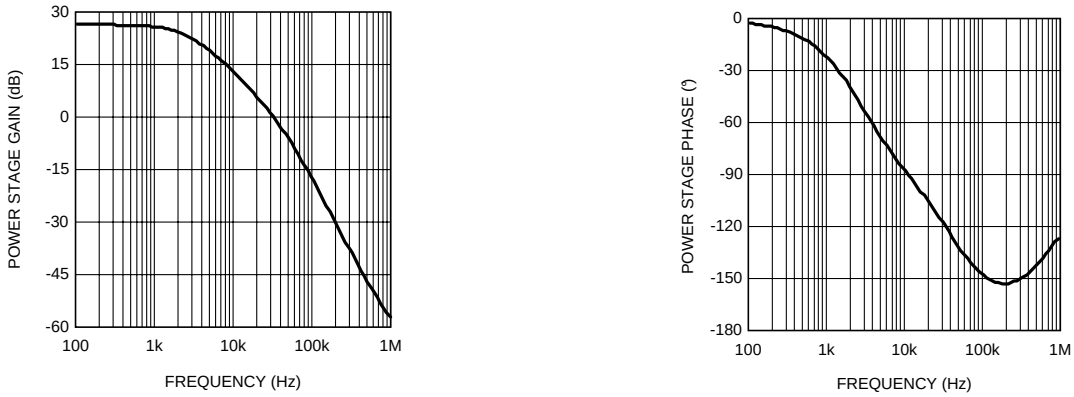


Figure 37. Power Stage Gain and Phase

The low frequency pole and higher frequency pole cause a roll-off in the gain of -20 dB/decade at lower frequency that increases to -40 dB/decade at higher frequency. The effect of the ESR zero is not seen because its frequency is beyond the switching frequency. If this loop were left uncompensated, the bandwidth would be 39 kHz and the phase margin 58°. This loop would be stable, but would suffer from poor regulation of the output voltage due to the low DC gain. In practice, this loop could change significantly due to the tolerances in the output inductor, output capacitor, changes in output current, or input voltage. Therefore, the loop is compensated using the error amplifier and a few passive components.

In general the goal of the compensation circuit is to give high DC gain, a bandwidth that is between one-fifth and one-tenth of the switching frequency, and at least 45° of phase margin. The majority of both peak current mode and emulated peak current mode buck regulators can be compensated with just two components, R_1 and C_1, as shown in the Typical Application Circuit. For power stages where the ESR zero frequency is below one-half of the switching frequency a second capacitor, C_2, may be needed to add another pole to the compensation. For power stages where the ESR zero frequency is beyond the control loop bandwidth, a compromise in bandwidth is needed to maintain good phase margin. The transfer function of the compensation block, G_{EA}, can be derived by multiplying the impedance $Z_C = (R_1 + 1/sC_1) \| (1/sC_2)$ times the DC gain of the error amp to give the following equation:

$$G_{EA} = g_m \times \frac{V_{FB}}{V_O} \times \frac{sR_1C_1 + 1}{s \times (sR_1C_1C_2 + C_1 + C_2)} \tag{30}$$

This transfer function provides one pole at the origin, one zero at $1/(2\pi R_1C_1)$, and another pole at approximately $1/(2\pi R_1C_2)$ if C_2 is used. If $\overline{C_2}$ is not used, a default value of 10 pF is substituted, representing the parasitic capacitance from the COMP/$\overline{SD}$ pin to ground.

The value for R_1 can be calculated using the following equation:

$$R_1 = \frac{B}{g_m} \tag{31}$$

The value, B, can be determined by evaluating the power stage transfer function at the desired cross-over frequency, or by reading the value graphically from the power stage gain plot. Setting B equal to the inverse of the linear gain will force the total loop gain to be 1 (0dB) at the cross-over frequency. For this example the desired cross-over frequency is 1/10 of the switching frequency, or 50 kHz. At 50 kHz the value of G_{PS} is approximately -4dB, or 0.63V/V. This indicates a system where the $f_Z \geq f_{SW}$. The value B should then be set to 1.58V/V and increased by 0.1V/V steps until the phase margin is at 45°. For this example, phase is 45° when B is 2.8V/V.

Once R_1 has been selected, C_1 is calculated based on the value of R_1 as shown in the following equation:

$$C_1 = \frac{1}{2\pi \times R_1 \times f_P} \tag{32}$$

R_1 = 3.73 kΩ, and C1 = 15.7 nF. The closest 1% value should be used for R_1 and the closest 10% value used for C_1, which gives:

R_1 = 3.74 kΩ 1%

C_1 = 15 nF 10%

The error amplifier of the LM3495 has a unity-gain bandwidth of 10 MHz. In order to model the effect of this limitation, the open-loop gain, OPG, can be calculated as:

$$OPG = \frac{2\pi \times 10\ MHz}{s + \frac{2\pi \times 10\ MHz}{g_m \times 72\ M\Omega}} \tag{33}$$

The new error amplifier transfer function taking into account unity-gain bandwidth is:

$$G_{EA\text{-}ACTUAL} = \frac{G_{EA} \times OPG}{1 + G_{EA} + OPG} \tag{34}$$

The gain and phase of the error amplifier are shown in Figure 38.

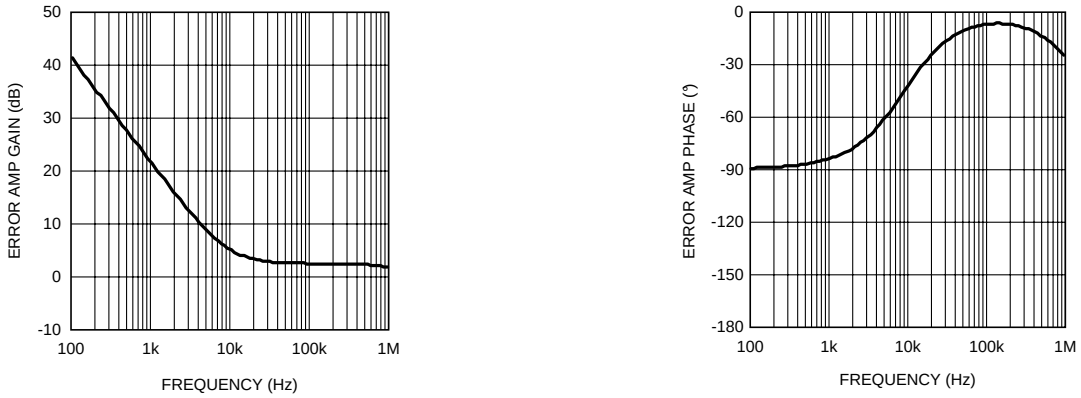


Figure 38. Error Amplifier Gain and Phase

The total control loop transfer function, H, is equal to the power stage transfer function multiplied by the error amplifier transfer function. The bandwidth and phase margin can be read graphically from Bode plots of H, shown in Figure 39.

$$H = G_{PS} \times G_{EA\text{-}ACTUAL} \tag{35}$$

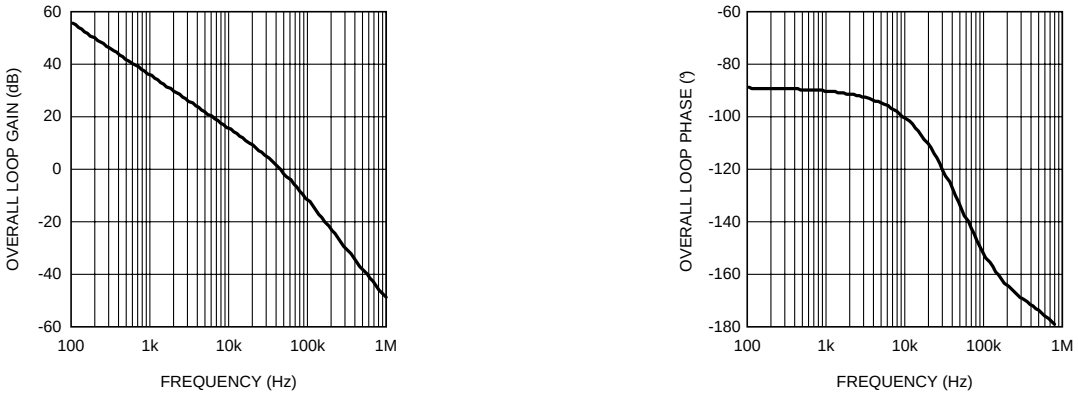


Figure 39. Overall Loop Gain and Phase

The bandwidth of this example circuit is 49 kHz, with a phase margin of 46°.

Efficiency Calculations

A reasonable estimation for the efficiency, η, of a buck regulator controlled by the LM3495 can be obtained by adding together the loss in each current carrying element, $P_{TOTAL-LOSS}$, and using the equation:

$$\eta = \frac{P_O}{P_O + P_{TOTAL-LOSS}} \quad (36)$$

The following shows an efficiency calculation to complement the Typical Application Circuit. Output power for this circuit is P_O = 1.2V x 10A = 12W. Input voltage is assumed to be 12V, and the calculations used assume that the converter runs in CCM.

Chip Operating Loss

This term accounts for the current drawn at the VIN pin. This current, I_{IN}, drives the logic circuitry and the power FETs. The gate driving loss term from the power FET section of Design Considerations is included in the chip operating loss. For the LM3495, I_{IN} is equal to the steady state operating current, I_Q, plus the FET driving current, I_{GC}. Power is lost as this I_{IN} passes through the internal linear regulator of the LM3495.

$$I_{GC} = (Q_{G-HI} + Q_{G-LO}) \times f_{OSC} \quad (37)$$

$$I_{GC} = (11nC + 33nC) \times 500\ kHz = 22\ mA \quad (38)$$

I_Q is typically 1.8 mA, taken from the Electrical Characteristics table. Chip Operating Loss is then:

$$P_Q = V_{IN} \times (I_Q + I_{GC}) \quad (39)$$

$$P_Q = 12V \times (1.8mA + 22mA) = 0.29W \quad (40)$$

High-Side FET Switching Loss

$$P_{SW} = 0.5 \times V_{IN} \times I_O \times (t_R + t_F) \times f_{SW} \quad (41)$$

$$P_{SW} = 0.5 \times 12V \times 10A \times (5\ ns + 8\ ns) \times 500\ kHz = 0.39W \quad (42)$$

FET Conduction Loss

$$P_C = D\ (I^2_O \times R_{DSON-HI} \times 1.3) \quad (43)$$

$$P_{C-HI} = 0.1 \times (100 \times 0.013) = 0.13W \quad (44)$$

$$P_C = (1 - D)\ (I^2_O \times R_{DSON-LO} \times 1.3) \quad (45)$$

$$P_{C-LO} = 0.9 \times (100 \times 0.0044) = 0.40W \quad (46)$$

R_{SNS} Loss (if used)

$$P_{SNS} = (1 - D)\ ((I_O)^2 \times R_{SNS}) \quad (47)$$

Not used in this example.

Input Capacitor Loss

This term represents the loss as input ripple current passes through the ESR of the input capacitor bank. In this equation 'n' is the number of capacitors in parallel.

$$P_{IN} = \frac{I^2_{rms\text{-}IN} \times ESR}{n}$$

$$I_{rms\text{-}IN} = I_O \times \sqrt{D(1 - D)}$$

$$I_{rms\text{-}IN} = 10 \times \sqrt{0.1(0.9)} = 3A \quad (48)$$

$$P_{IN} = (3A)^2 \times 2m\Omega) = 0.018W \quad (49)$$

Output Inductor Loss

$$P_{LOUT} = (I_O)^2 \times R_L \quad (50)$$

$$P_{LOUT} = (10A)^2 \times 3\ m\Omega = 0.3W \quad (51)$$

Total Loss

$$P_{LOSS} = 1.53W \quad (52)$$

Efficiency

$$n = 12W/(12W + 1.50W) = 88\% \quad (53)$$

Layout Considerations

To produce an optimal power solution with the LM3495, good layout and design of the PCB are as important as the component selection. The following are several guidelines to aid in creating a good layout.

KELVIN TRACES FOR SENSE LINES

The pins of the low-side FET should be connected as close as possible to the SW/CSH and CSL pins. Each pin should use a separate trace, and the traces should be run parallel to each other to give common mode rejection. Although it can be difficult in a compact design, these traces should stay away from the output inductor if possible, to avoid coupling stray flux.

The SNS pin should also be connected using a separate Kelvin trace, running from the positive pin/pad of the output cap to the pin itself. This trace should also be used to connect to the top of the feedback resistors. Keep this trace away from the switch node and from the output inductor.

SEPARATE PGND AND SGND

Good layout techniques include a dedicated ground plane, usually on an internal layer. Signal level components like the compensation and feedback resistors should be connected to a section of this internal plane, SGND. The SGND section of the plane should be connected to the power ground at only one point. The best place to connect the SGND and PGND is right at the SGND pin.

MINIMIZE THE SWITCH NODE

The plane that connects the power FETs and output inductor together radiates more EMI as it gets larger. Use just enough copper to give low impedance to the switching currents.

LOW IMPEDANCE POWER PATH

The power path includes the input capacitors, power FETs, output inductor, and output capacitors. Keep these components on the same side of the PCB and connect them with thick traces or copper planes (shapes) on the same layer. Vias add resistance and inductance to the power path, and have high impedance connections to internal planes than to the top of bottom layers of a PCB. If heavy switching currents must be routed through vias and/or internal planes, use multiple vias in parallel to reduce their resistance and inductance. The power components should be kept close together. The longer the paths that connect them, the more they act as antennas, radiating unwanted EMI.

Table 1. Bill of Materials for 6.0V to 18.0V Input, 1.0V Output, 7A, 500 kHz

ID	Part Number	Type	Size	Parameters	Qty	Vendor
U1	LM3495	Synchronous Controller	TSSOP-16		1	TI
Q1	Si4894DY	N-MOSFET	SO-8	30V, 15mΩ, 11.5nC	1	Vishay
Q2	Si4442DY	N-MOSFET	SO-8	30V, 4.1mΩ, 36nC	1	Vishay
D1	MBR0530	Schottky Diode	SMA	30V, 0.5A	1	Vishay
L1	RLF12545T-2R7N8R7	Inductor	12.5x12.8 x 4.7mm	2.7µH 8.7A 4.5mΩ	1	TDK
C_{IN1},C_{IN2}	C3225X5R1E106M	Capacitor	1210	22µF, 25V	2	TDK
C_{O1}	6TPD470M	Capacitor	7.3x4.3 x3.8	470µF 6.3V 10mΩ	1	Sanyo
C_F	C2012X7R1E105M	Capacitor	0805	1µF, 25V	1	TDK
C_{DD}	C2012X7R1C225M	Capacitor	0805	2.2µF 16V	1	TDK
C_B, C_{INX}	VJ0805Y104KXXAT	Capacitor	0805	100nF 10%	2	Vishay
C_{C1}	VJ0805Y822KXXAT	Capacitor	0805	8.2nF 10%	1	Vishay
C_{C2}	VJ0805A1012KXXAT	Capacitor	0805	100pF 10%	1	Vishay
R_{C1}	CRCW08055761F	Resistor	0805	5.76kΩ 1%	1	Vishay
R_{FB1}	CRCW080510502F	Resistor	0805	15kΩ 1%	1	Vishay
R_{FB2}	CRCW08051002F	Resistor	0805	10kΩ 1%	1	Vishay
R_{FRQ}	CRCW08055492F	Resistor	0805	54.9kΩ 1%	1	Vishay
R_{LIM}	CRCW08052671F	Resistor	0805	2.67kΩ 1%	1	Vishay

Table 2. Bill of Materials for 3.0V to 6.0V Input, 2.2V Output, 7A, 500 kHz

ID	Part Number	Type	Size	Parameters	Qty	Vendor
U1	LM3495	Synchronous Controller	TSSOP-16		1	TI
Q1	Si4866DY	N-MOSFET	SO-8	12V, 6.5mΩ, 21nC	1	Vishay
Q2	Si4838DY	N-MOSFET	SO-8	12V, 3.1mΩ, 40nC	1	Vishay
D1	MBR0530	Schottky Diode	SMA	30V, 0.5A	1	Vishay
L1	MSS1260–102NX	Inductor	12.3x12.3 x 6mm	1µH 8A 10mΩ	1	Coilcraft
C_{IN1}, C_{IN2}	C3225X5R1A226M	Capacitor	1210	22µF, 10V	2	TDK
C_{O1}	6TPD470M	Capacitor	7.3x4.3 x3.8	470µF 6.3V 10mΩ	2	Sanyo
C_F	C2012X7R1E105M	Capacitor	0805	1µF, 25V	1	TDK
C_{DD}	C2012X7R1C225M	Capacitor	0805	2.2µF 16V	1	TDK
C_B, C_{INX}	VJ0805Y104KXXAT	Capacitor	0805	100nF 10%	2	Vishay
C_{C1}	VJ0805Y472KXXAT	Capacitor	0805	4.7nF 10%	1	Vishay
R_{C1}	CRCW08051742F	Resistor	0805	17.4kΩ 1%	1	Vishay
R_{FB1}	CRCW08053741F	Resistor	0805	3.74kΩ 1%	1	Vishay
R_{FB2}	CRCW08051002F	Resistor	0805	10kΩ 1%	2	Vishay
R_{FRQ}	CRCW08055492F	Resistor	0805	54.9kΩ 1%	1	Vishay
R_{LIM}	CRCW08052051F	Resistor	0805	2.05kΩ 1%	1	Vishay

Table 3. Bill of Materials for Typical Application Circuit

ID	Part Number	Type	Size	Parameters	Qty	Vendor
U1	LM3495	Synchronous Controller	TSSOP-16		1	TI
Q1	HAT2198R	N-MOSFET	SO-8	30V, 9.6mΩ, 11nC	1	Renesas
Q2	HAT2165H	N-MOSFET	LFPAK	30V, 3.4mΩ, 33nC	1	Renesas
D1	MBR0530	Schottky Diode	SMA	30V, 0.5A	1	Vishay
L1	RLF12560T-1R0N140	Inductor	12.5x12.8 x 6mm	1µH 14A 3mΩ	1	TDK
C_{IN}	C3225X5R1E226M	Capacitor	1210	22µF, 25V	1	TDK
C_{O1}, C_{O2}	C3225X5R0J107M	Capacitor	1210	100µF 6.3V 1.5mΩ	2	TDK
C_F	C2012X7R1E105M	Capacitor	0805	1µF, 25V	1	TDK
C_{DD}	C2012X7R1C225M	Capacitor	0805	2.2µF 16V	1	TDK
C_B, C_{INX}	VJ0805Y104KXXAT	Capacitor	0805	100nF 10%	2	Vishay
C_{C1}	VJ0805Y103KXXAT	Capacitor	0805	10nF 10%	1	Vishay
R_{C1}	CRCW08051501F	Resistor	0805	1.5kΩ 1%	1	Vishay
R_{FB1}, R_{FB2}	CRCW08051002F	Resistor	0805	10kΩ 1%	2	Vishay
R_{FRQ}	CRCW08055492F	Resistor	0805	54.9kΩ 1%	1	Vishay
R_{LIM}	CRCW08053321F	Resistor	0805	3.32kΩ 1%	1	Vishay

REVISION HISTORY

Changes from Revision E (April 2013) to Revision F	Page
• Changed layout of National Data Sheet to TI format	29

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM3495MTC/NOPB	ACTIVE	TSSOP	PW	16	92	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LM3495 MTC	Samples
LM3495MTCX/NOPB	ACTIVE	TSSOP	PW	16	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LM3495 MTC	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

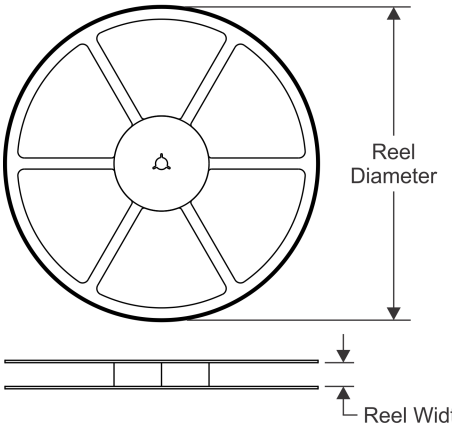
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

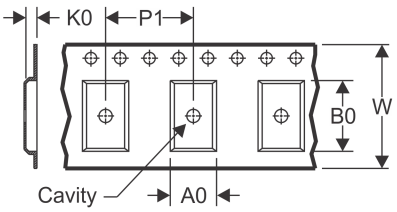
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

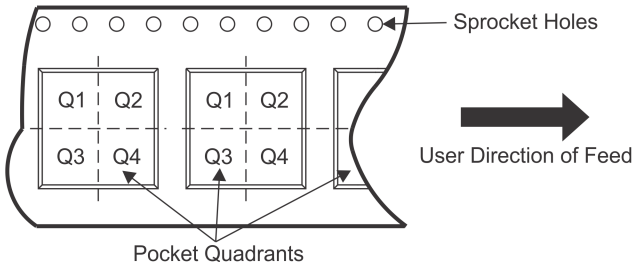


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

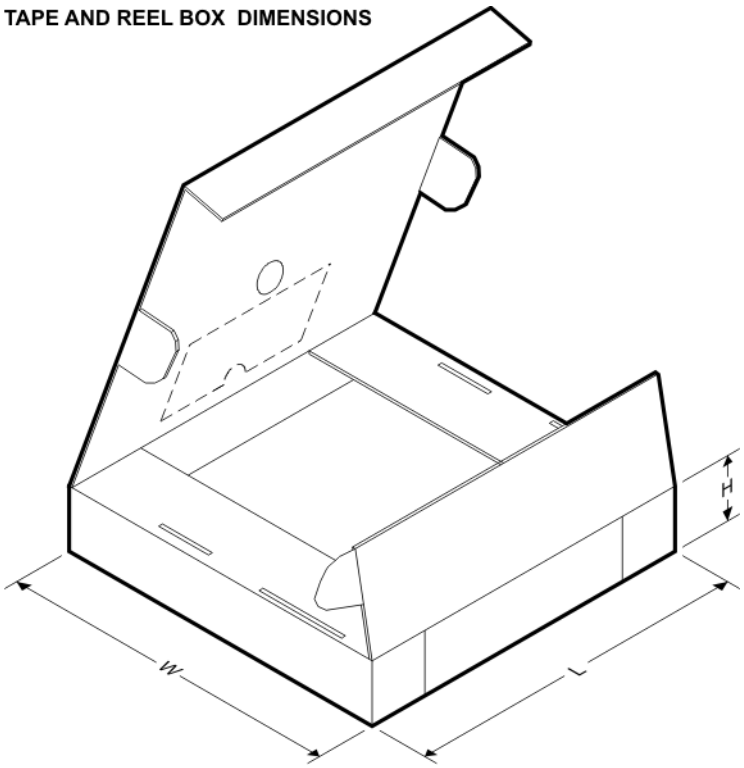
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3495MTCX/NOPB	TSSOP	PW	16	2500	330.0	12.4	6.95	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

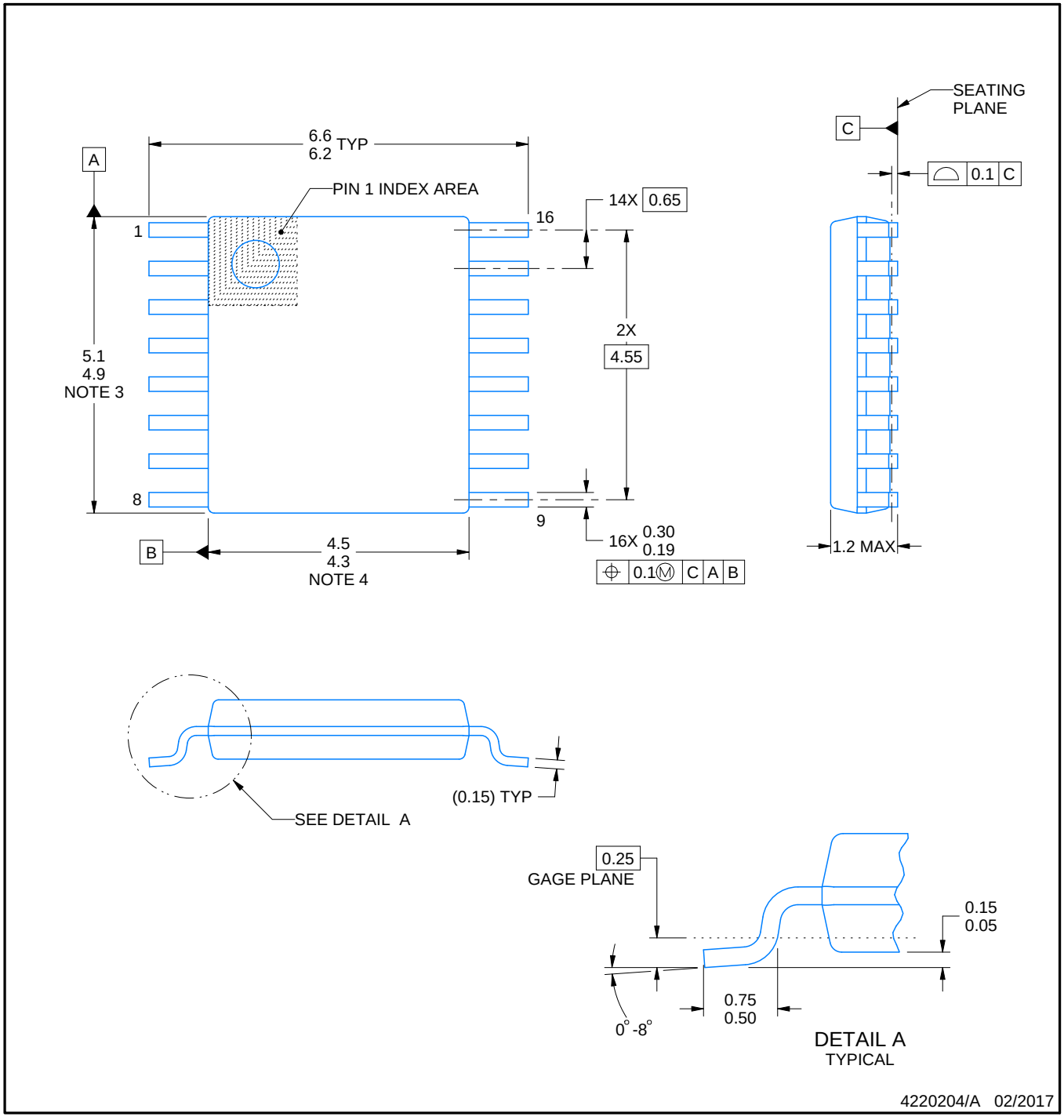
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3495MTCX/NOPB	TSSOP	PW	16	2500	367.0	367.0	35.0

PACKAGE OUTLINE

PW0016A

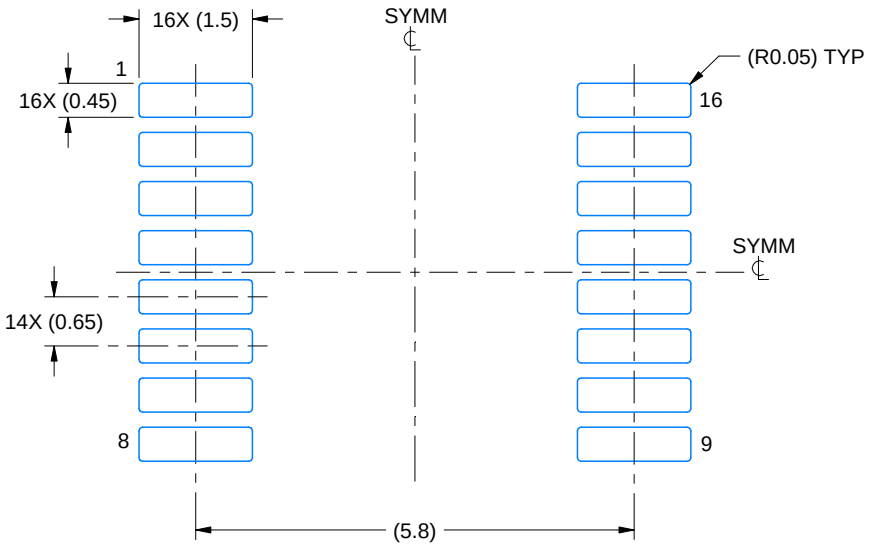
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

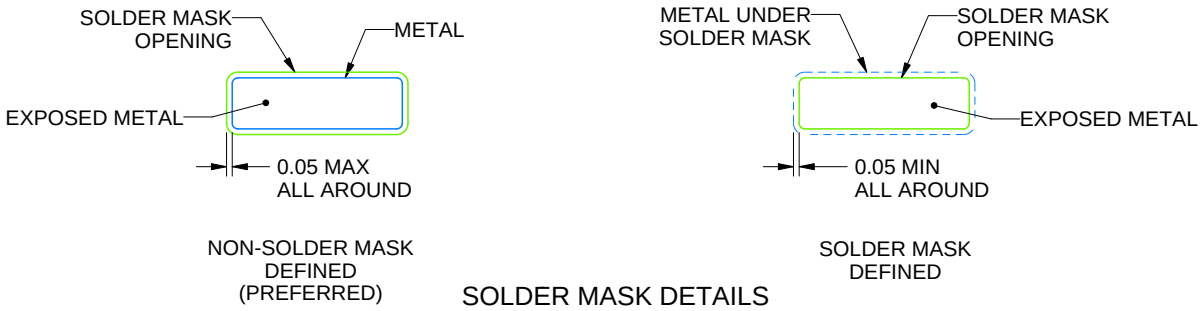


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

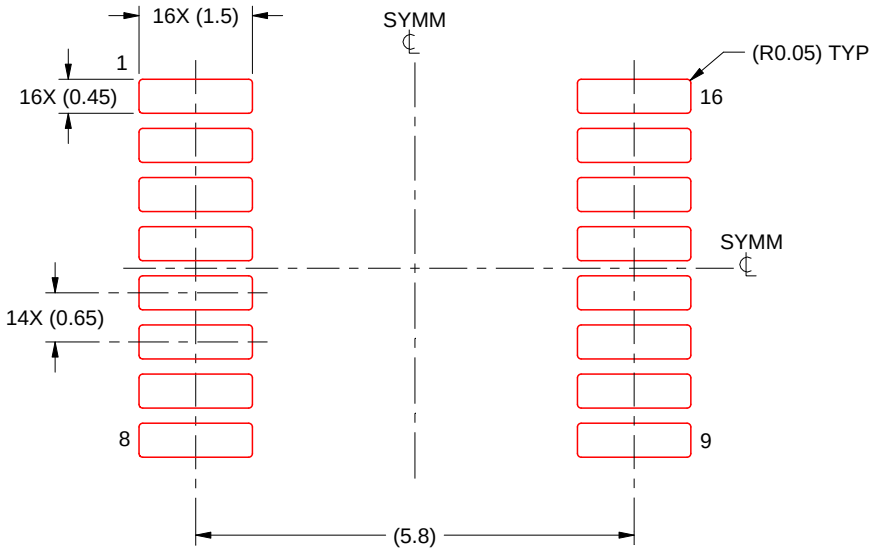


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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