



N-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY				
V _{DS} (V)	$R_{DS(on)}\left(\Omega\right)$	I _D (A)		
20	0.0055 at V _{GS} = 10 V	20		
	0.009 at V _{GS} = 4.5 V	16		

FEATURES

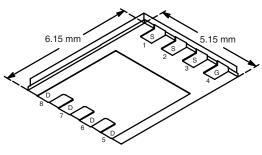
- · Halogen-free available
- TrenchFET[®] Power MOSFET
- Q_g Optimized



APPLICATIONS

• Synchronous Rectifier for DC/DC

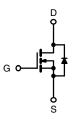
PowerPAK® SO-8



Bottom View

Ordering Information: Si7366DP-T1-E3 (Lead (Pb)-free)

Si7366DP-T1-GE3 (Lead (Pb)-free and Halogen-free)



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS T	$_{A} = 25 ^{\circ}$ C, unles	ss otherwise n	oted		
Parameter		Symbol	10 s	Steady State	Unit
Drain-Source Voltage		V_{DS}	20		٧
Gate-Source Voltage		V_{GS}	± 20		
Continuous Drain Current (T, = 150 °C) ^a	T _A = 25 °C	I_	20	13	
Continuous Diain Current (1) = 150 °C)	T _A = 70 °C	ID	17	10	Α
Pulsed Drain Current (10 µs Pulse Width)		I _{DM}	50		A
Continuous Source Current (Diode Conduction) ^a		I _S	4.1	1.4	
Maximum Dawar Dissipations	T _A = 25 °C	P _D	5	1.7	W
Maximum Power Dissipation ^a	T _A = 70 °C	י ט	3.2	1.1	VV
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150		°C
Soldering Recommendations (Peak Temperature)b,c		-	2	260	C

THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^a	t ≤ 10 s	R _{thJA}	20	25	°C/W	
Maximum Junction-to-Ambient	Steady State		53	70		
Maximum Junction-to-Case (Drain)	Steady State	R _{thJC}	3.4	4.5		

Notes:

- a. Surface Mounted on 1" x 1" FR4 board.
- b. See Solder Profile (http://www.vishay.com/ppg?73257). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- c. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components. .

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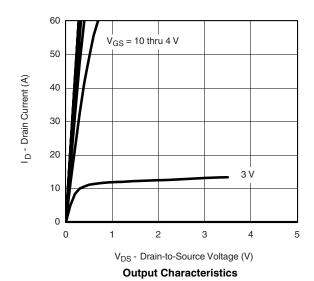
Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static							
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	1.0		3.0	V	
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA	
Zara Cata Valtaga Drain Current	I _{DSS}	V _{DS} = 20 V, V _{GS} = 0 V		1			
Zero Gate Voltage Drain Current		$V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55 ^{\circ}\text{C}$			5	μΑ	
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	30			Α	
	R _{DS(on)}	V _{GS} = 10 V, I _D = 20 A		0.0045	0.0055	Ω	
Drain-Source On-State Resistance ^a		$V_{GS} = 4.5 \text{ V}, I_D = 16 \text{ A}$		0.0072	0.009		
Forward Transconductance ^a	9 _{fs}	$V_{DS} = 6 \text{ V}, I_{D} = 20 \text{ A}$		48		S	
Diode Forward Voltage ^a	V_{SD}	I _S = 4.5 A, V _{GS} = 0 V		0.76	1.1	V	
Dynamic ^b			•				
Total Gate Charge	Q_g			16	25		
Gate-Source Charge	Q_{gs}	$V_{DS} = 10 \text{ V}, V_{GS} = 4.5 \text{ V}, I_{D} = 20 \text{ A}$		6		nC	
Gate-Drain Charge	Q_{gd}			5.2			
Gate Resistance	R_{g}			1.8		Ω	
Turn-On Delay Time	t _{d(on)}			21	32		
Rise Time	t _r	V_{DD} = 10 V, R_L = 10 Ω		16	25	ns	
Turn-Off Delay Time	t _{d(off)}	$I_D\cong$ 1 A, V_{GEN} = 10 V, R_G = 6 Ω		58	90		
Fall Time	t _f			15	23		
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 4.1 A, di/dt = 100 A/μs		40	80		

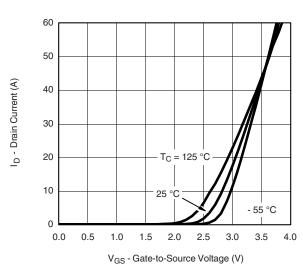
Notes:

- a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %.
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted





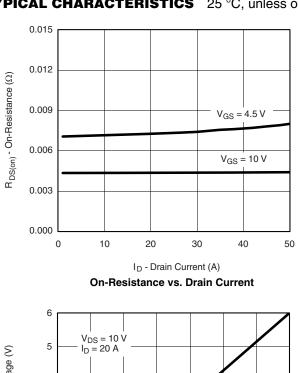
Transfer Characteristics

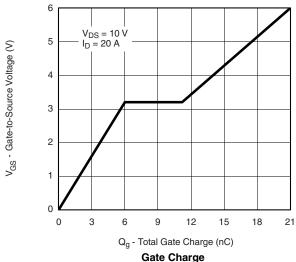


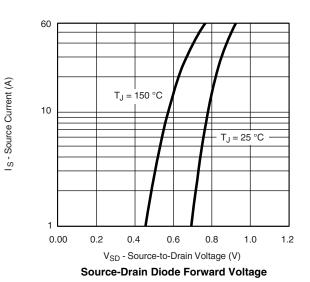


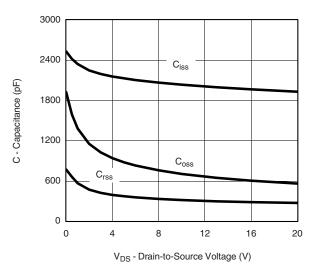


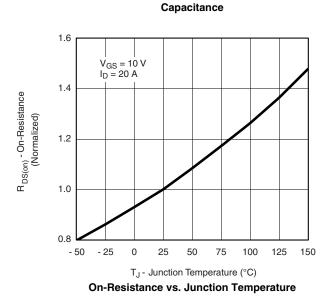
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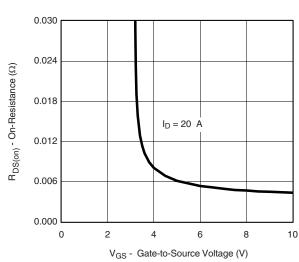










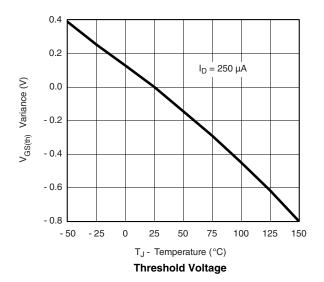


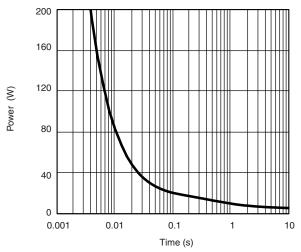
On-Resistance vs. Gate-to-Source Voltage

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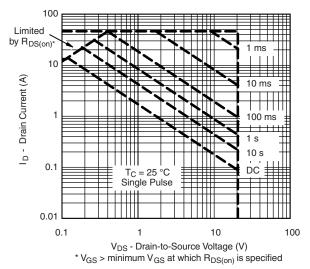
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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

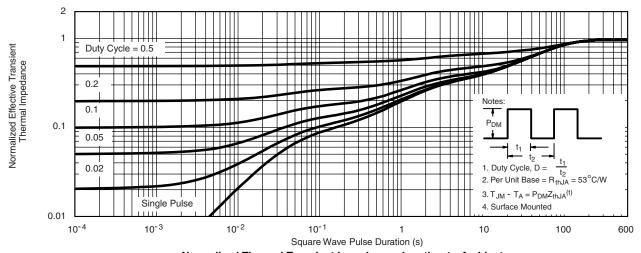








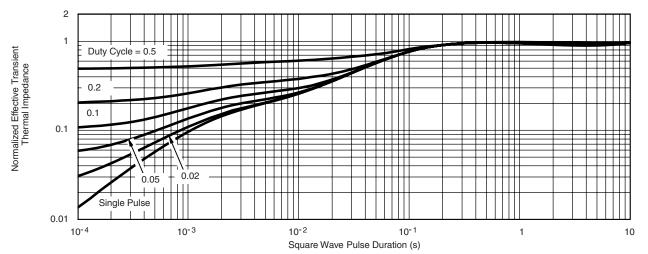
Safe Operating Area, Junction-to-Case



Normalized Thermal Transient Impedance, Junction-to-Ambient



TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Case

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