

# TPS65311-Q1 High-Voltage Power-Management IC for Automotive Applications

## 1 Features

- Qualified for Automotive Applications
- AEC-Q100 Test Guidance With the Following Results:
  - Device Temperature Grade 1:  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  Ambient Operating Temperature
  - Device HBM ESD Classification Level H1B
  - Device CDM ESD Classification Level C4B
- Input Voltage Range: 4 V to 40 V, Transients up to 60 V; 80 V When Using External PMOS-FET
- Single-Output Synchronous-Buck Controller
  - Peak Gate-Drive Current 0.6 A
  - 490-kHz Fixed Switching Frequency
  - Pseudo Random Frequency-Hopping Spread Spectrum or Triangular Mode
- Dual-Synchronous Buck Converter
  - Designed for Output Currents up to 2 A
  - Out of Phase Switching
  - Switching Frequency: 2.45 MHz
- Adjustable 350-mA Linear Regulator
- Adjustable Asynchronous-Boost Converter
  - 1-A Integrated Switch
  - Switching Frequency: 2.45 MHz
- Soft-Start Feature for All Regulator Outputs
- Independent Voltage Monitoring
- Undervoltage (UV) Detection and Overvoltage (OV) Protection
- Short Circuit, Overcurrent, and Thermal Protection on all supply output rails
- Serial-Peripheral Interface (SPI) for Control and Diagnostic
- Integrated Window Watchdog (WD)
- Reference Voltage Output
- High-Side (HS) Driver for Use with External PMOS-FET for driving an LED
- Input for External Temperature Sensor for Shutdown at  $T_A < -40^{\circ}\text{C}$
- Thermally Enhanced Packages With Exposed Thermal Pad
  - 56-Pin VQFN (RVJ) or 56-Pin VQFNP (RWE)

## 2 Applications

- Multi-Rail DC Power Distribution Systems
- Safety-Relevant Automotive Applications
  - Advanced Driver Assistance Systems

## 3 Description

The TPS65311-Q1 device is a power-management IC (PMIC), meeting the requirements of digital-signal-processor (DSP) controlled-automotive systems (for example, advanced driver-assistance systems). With the integration of commonly used supply rails and features, the TPS65311-Q1 device significantly reduces board space and system costs.

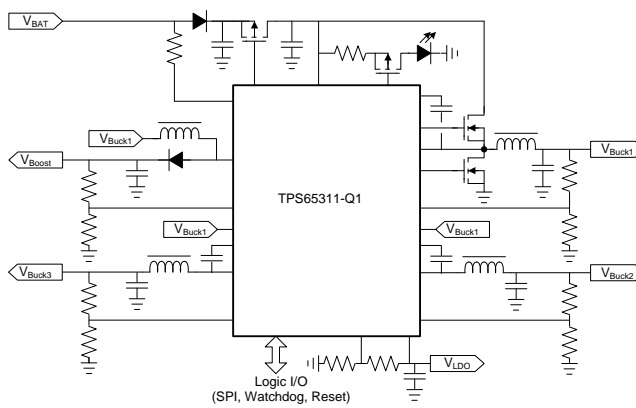
The device is capable of providing stable output voltages to the application, including a typical 5-V CAN-supply, from a varying input power supply (such as an automotive car battery) from 4 V to 40 V. The device includes one synchronous buck controller as a pre-regulator that offers flexible output power to the application. For post-regulation, the device includes two synchronous buck and one asynchronous boost converter, working at a switching frequency of 2.45 MHz to allow for a smaller inductor which requires less board space. The two buck converters also offer internal loop compensation which eliminates the need for external compensation components. Furthermore, the device includes a low-noise linear regulator.

### Device Information<sup>(1)</sup>

DEVICE NAME	PACKAGE	BODY SIZE
TPS65311-Q1	VQFN (56)	8.00 mm × 8.00 mm
	VQFNP (56)	8.00 mm × 8.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

### Simplified Schematic



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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (April 2014) to Revision C	Page
• Added the VQFN (RWE) package option to the data sheet .....	1
• Added pin descriptions for the S1 and S2 pins in the <i>Pin Functions</i> table .....	5
• Deleted the lead temperature (soldering, 10 sec), 260°C parameter from the <i>Absolute Maximum Ratings</i> table .....	8
• Changed the <i>Handling Ratings</i> table to <i>ESD Ratings</i> and moved storage temperature back to the <i>Absolute Maximum Ratings</i> table .....	8
• Changed all the thermal values for the RWE package in the <i>Thermal Information</i> table .....	8
• Added the <i>Receiving Notification of Documentation Updates</i> and <i>Community Resources</i> sections .....	55

Changes from Revision A (October 2013) to Revision B	Page
• Changed CDM ESD Classification Level from C3B to C4B in the <i>Features</i> list and ESD ratings .....	1
• Added device number to document title .....	1
• Added <i>Device Information</i> table to first page and <i>Table of Contents</i> to second page. Moved <i>Revision History</i> to second page also .....	1
• Added two new paragraphs following the first paragraph in the <i>Description</i> section .....	1
• Deleted simplified block diagram from first page and added new schematic image .....	1
• Moved the pin diagram and function table to before the electrical specifications and change it to the <i>Pin Configurations and Functions</i> section .....	4
• Added the word <i>range</i> to the <i>Absolute Maximum Ratings</i> .....	7
• Moved the electrical specifications tables into the <i>Specifications</i> section .....	7
• Moved the ESD ratings and storage temperature out of the <i>Absolute Maximum Ratings</i> table and into the <i>Handling Ratings</i> table. Also added the ESD HBM and CDM notes .....	8
• Changed both max values for $T_J$ from 125 to 150 in the RECOMMEND OPERATING CONDITIONS table .....	8
• Lowered all thermal values in the <i>Thermal Information</i> table .....	8
• Changed condition statement of <i>ELECTRICAL CHARACTERISTICS</i> table from $T_{J(max)} = 125^{\circ}C$ to $T_{J(max)} = 150^{\circ}C$ .....	9

• Added test condition for $I_{OUT} = 350 \text{ mA}$ , $T_J = 150^\circ\text{C}$ to the $V_{Dropout}$ parameter in the <i>ELECTRICAL CHARACTERISTICS</i> table .....	10
• Changed the min value for the $V_{HSSC\_HY}$ parameter from 1.5 to 1 and deleted the typ (2.5) and max (3.5) values .....	10
• Moved all timing specifications from the <i>Electrical Characteristics</i> table into the <i>Timing Requirements</i> table and added figure references to the timing diagram .....	13
• Changed the max value for the $t_{VSSENSE\_BLK}$ parameter from 20 to 35 .....	13
• Changed the MAX value for the WD filter time parameter from 0.5 $\mu\text{s}$ to 1.2 $\mu\text{s}$ in the <i>Timing Requirements</i> table .....	14
• Changed the min value for the $t_{GL\_BLK}$ parameter from 10 to 5 .....	14
• Moved all switching characteristics out of the <i>Electrical Characteristics</i> and into the new <i>Switching Characteristics</i> table .....	15
• Moved all but the first paragraph of the Description into the new <i>Overview</i> section in the <i>Detailed Description</i> section....	19
• Moved the block diagram into the <i>Detailed Description</i> section .....	20
• Deleted the <i>Operating Modes</i> table and <i>Normal Mode PWM Operation</i> section title for Buck Controller (BUCK1).....	21
• Changed the resistor name for the resistor next to $C_1$ from $R_1$ to $R_3$ and added $R_1$ and $R_2$ to the <i>Detailed Block Diagram of Buck 1 Controller</i> image .....	21
• Moved the component selection portion of the <i>Synchronous Buck Converters BUCK2 and BUCK3</i> section into the <i>Typical Applications</i> section .....	22
• Moved the component selection portion of the <i>BOOST Converter</i> section into the <i>Typical Applications</i> section .....	22
• Changed the voltage value that EXTSUP is connected to from 4.6 to 4.8 in the <i>Gate Driver Supply</i> section .....	23
• Moved the <i>SPI</i> section into a <i>Programming</i> section .....	34
• Added the <i>Design Parameters</i> tables for each of the <i>Typical Application</i> sections .....	42
• Added the <i>Adjusting the Output Voltage for the BUCK1 Controller</i> section to the <i>Buck Controller (BUCK1)</i> application section .....	42
• Moved the component selection portion of the <i>Buck Controller (BUCK1)</i> section into the <i>Typical Applications</i> section ...	42
• Changed $R_1$ to $R_3$ in the <i>Compensation of the Buck Controller</i> section .....	43
• Added the <i>Adjusting the Output Voltage for the BUCK2 and BUCK3 Converter</i> to the <i>Detailed Design Procedure</i> in the <i>Synchronous Buck Converters BUCK2 and BUCK3</i> section .....	45
• Changed the inductance, capacitance and FLC values from 3.3 $\mu\text{H}$ , 20 $\mu\text{F}$ , and 12.9 kHz to 1.5 $\mu\text{H}$ , 39 $\mu\text{F}$ , and 13.7 kHz (respectively) in the <i>For example:</i> section of the <i>Compensation of the BOOST Converter</i> section .....	49
• Added the <i>Linear Regulator</i> application section .....	50
• Added the <i>Device and Documentation Support and Mechanical, Packaging, and Orderable Information</i> sections. The <i>Device and Documentation Support</i> now includes the electrostatic discharge caution, trademark information, and a link to the TI Glossary.....	55

**Changes from Original (October 2013) to Revision A**
**Page**

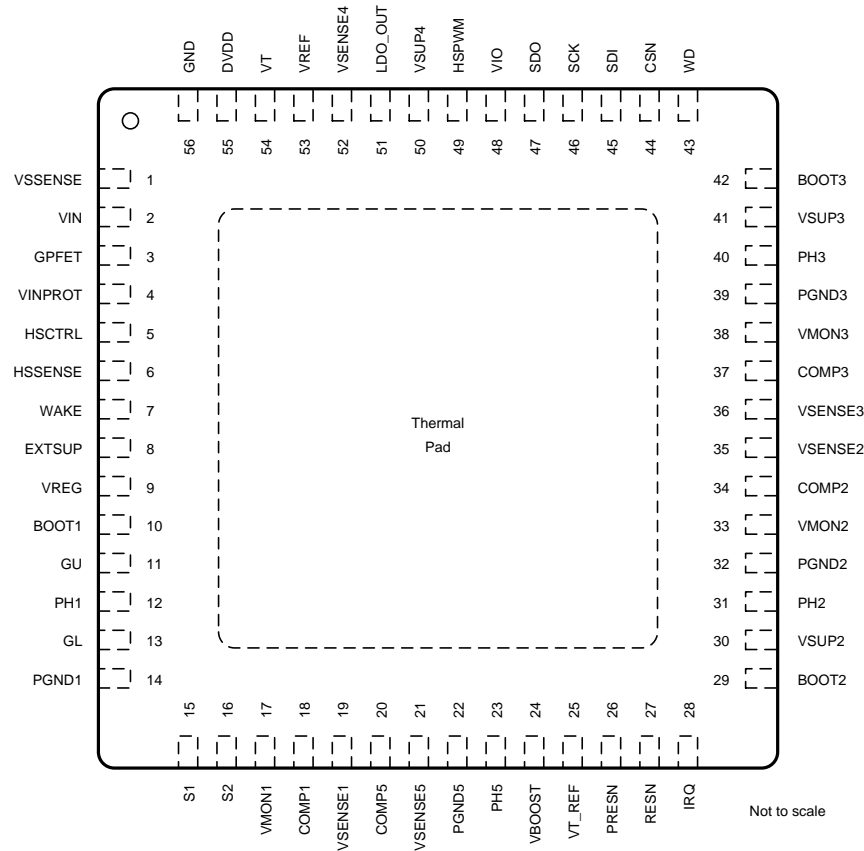
• Changed document status from <i>Product Preview</i> to <i>Production Data</i> .....	1
• Deleted both min values ( $-44^\circ\text{C}$ and $-55^\circ\text{C}$ ) for $T_J$ in the <i>RECOMMENDED OPERATING CONDITIONS</i> table.....	8
• Changed both max values for $T_J$ from $150^\circ\text{C}$ to $125^\circ\text{C}$ in the <i>RECOMMENDED OPERATING CONDITIONS</i> table.....	8
• Changed condition statement of <i>ELECTRICAL CHARACTERISTICS</i> table from $T_J$ temperature range to $T_{J(max)} = 125^\circ\text{C}$ . 9	
• Changed one test condition for the $V_{Dropout}$ parameter in the <i>ELECTRICAL CHARACTERISTICS</i> table from $T_J = 150^\circ\text{C}$ to $T_J = 125^\circ\text{C}$ .....	10
• Deleted the $T_J$ temperature range from SHUTDOWN COMPARATOR subheader row in the <i>ELECTRICAL CHARACTERISTICS</i> table .....	11
• Changed one test condition for the $I_{VT\_leak}$ parameter in the <i>ELECTRICAL CHARACTERISTICS</i> table from $T_J = -20^\circ\text{C}$ to $150^\circ\text{C}$ to $T_J = -20^\circ\text{C}$ to $125^\circ\text{C}$ .....	11
• Changed the $T_J$ temperature range to $T_{J(max)} = 125^\circ\text{C}$ for the INTERNAL VOLTAGE REGULATORS subheader row in the <i>ELECTRICAL CHARACTERISTICS</i> table .....	12

## 5 Description (continued)

To help support system safety, the device includes voltage monitoring on all supply rails and a window-watchdog to monitor the MCU and DSP. Other features include a high-side driver which drives a warning-lamp LED, a reference voltage which is used as ADC reference in the MCU, DSP, and a shutdown comparator which, in combination with external NTC-resistor, switches off the device at too-low ambient temperature.

## 6 Pin Configuration and Functions

**56-Pin VQFN and VQFN  
RVJ and RWE Package With Exposed Thermal Pad  
Top View**



### Pin Functions

PIN		TYPE <sup>(1)</sup>	PULLUP OR PULLDOWN	DESCRIPTION
NAME	NO.			
BOOT1	10	I	—	The capacitor on this pin acts as the voltage supply for the BUCK1 high-side MOSFET gate-drive circuitry.
BOOT2	29	I	—	The capacitor on this pin acts as the voltage supply for the BUCK2 high-side MOSFET gate drive circuitry.
BOOT3	42	I	—	The capacitor on this pin act as the voltage supply for the BUCK3 high-side MOSFET gate drive circuitry.
COMP1	18	O	—	Error amplifier output for the switching controller. External compensation network is connected to this pin.
COMP2	34	I	—	Compensation selection for the BUCK2 switching converter
COMP3	37	I	—	Compensation selection for the BUCK3 switching converter.
COMP5	20	O	—	Error amplifier output for the boost switching controller. External compensation network is connected to this pin.
CSN	44	I	Pullup	SPI – Chip select

(1) Description of pin type: I = Input; O = Output; OD = Open-drain output

**Pin Functions (continued)**

PIN		TYPE <sup>(1)</sup>	PULLUP OR PULLDOWN	DESCRIPTION
NAME	NO.			
DVDD	55	O	—	Internal DVDD output for decoupling
EXTSUP	8	I	—	Optional LV input for gate driver supply
GL	13	O	—	Gate driver – low-side FET
GND	56	O	—	Analog GND, digital GND and substrate connection
GPFET	3	O	—	Gate driver external protection PMOS FET.
GU	11	O	—	Gate driver – high-side FET
HSCTRL	5	O	—	High-side gate driver output
HSPWM	49	I	Pulldown	High side and LED PWM input
HSENSE	6	I	—	Sense input high side and LED
IRQ	28	OD	—	Low battery interrupt output in operating mode
LDO_OUT	51	O	—	Linear regulated output (connect a low ESR ceramic output capacitor to this pin)
PGND1	14	O	—	Ground for low-side FET driver
PGND2	32	O	—	Power ground of synchronous converter BUCK2
PGND3	39	O	—	Power ground of synchronous converter BUCK3
PGND5	22	O	—	Power ground boost converter
PH1	12	O	—	Switching node - BUCK1 (floating ground for high-side FET driver)
PH2	31	O	—	Switching node BUCK2
PH3	40	O	—	Switching node BUCK3
PH5	23	O	—	Switching node boost
PRESN	26	OD	—	Peripherals reset
RESN	27	OD	—	System reset
S1	15	I	—	Differential current sense input for BUCK1
S2	16	I	Pulldown	Differential current sense input for BUCK1, pulldown only active in RAMP and ACTIVE state
SCK	46	I	Pulldown	SPI – Clock
SDI	45	I	Pulldown	SPI – Master out, slave in
SDO	47	O	—	SPI – Master in, slave out - push-pull output supplied by VIO
VBOOST	24	I	—	Booster output voltage
VIN	2	I	—	Unprotected supply input for the base functionality and band-gap 1. Supplied blocks are: RESET, WD, wake, SPI, temp sensing, voltage monitoring and the logic block.
VINPROT	4	I	—	Main input supply (gate drivers and bandgap2)
VIO	48	I	—	Supply input for the digital interface to the MCU. Voltage on this input is monitored. If VIO falls below UV threshold a reset is generated and the part enters error mode.
VMON1	17	I	—	Input for the independent voltage monitor at BUCK1
VMON2	33	I	—	Input for the independent voltage monitor at BUCK2
VMON3	38	I	—	Input for the independent voltage monitor at BUCK3
VREF	53	O	—	Accurate reference voltage output for peripherals on the system (for example, ADC)
VREG	9	O	—	Internal regulator for gate driver supply (decoupling) and VREF
VSENSE1	19	I	—	Input for externally sensed voltage of the output using a resistor divider network from their respective output line to ground.
VSENSE2	35	I	—	Input for externally sensed voltage of the output using a resistor divider network from their respective output line to ground
VSENSE3	36	I	—	Input for externally sensed voltage of the output using a resistor divider network from their respective output line to ground
VSENSE4	52	I	—	Input for externally sensed voltage of the output using a resistor divider network from their respective output line to ground.
VSENSE5	21	I	—	Input for externally sensed voltage of the boost output using a resistor divider network from their respective output line to ground.
VSENSE	1	I	—	Input to monitor the battery line for undervoltage conditions. UV is indicated by the IRQ pin.
VSUP2	30	I	—	Input voltage supply for switch mode regulator BUCK2
VSUP3	41	I	—	Input voltage supply for switch mode regulator BUCK3
VSUP4	50	I	—	Input voltage supply for linear regulator LDO

**Pin Functions (continued)**

PIN		TYPE <sup>(1)</sup>	PULLUP OR PULLDOWN	DESCRIPTION
NAME	NO.			
VT	54	I	—	Input for the comparator with shutdown functionality. This input can be used to sense an external NTC resistor to shutdown the IC in case the ambient temperature is too high or too low. Tie to GND if not in use.
VT_REF	25	O	—	Shutdown comparator reference output. Internally connected to DVDD, current-limited. When not in use can be connected to DVDD or left open.
WAKE	7	I	Pulldown	Wake up input
WD	43	I	Pulldown	Watchdog input. WD is the trigger input coming from the MCU.

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Supply inputs	VIN	-0.3	80	V
	VINPROT	-0.3	60	
	VSUP2, 3 (BUCK2 and 3)	-0.3	20	
	VSUP4 (Linear Regulator)	-0.3	20	
	VBOOST	-0.3	20	
	EXTSUP	-0.3	13	
	VIO	-0.3	5.5	
Buck controller	PH1	-1 -2 for 100 ns	60	V
	VSENSE1	-0.3	20	
	COMP1	-0.3	20	
	GU-PH1, GL-PGND1, BOOT1-PH1	-0.3	8	
	S1, S2	-0.3	20	
	S1-S2	-2	2	
	BOOT1	-0.3	68	
Buck controller	VMON1	-0.3	20	V
	BOOT2, BOOT3	-1	20	
	PH2, PH3	-1 <sup>(2)</sup> -2 for 10 ns	20 <sup>(2)</sup>	
	VSENSE2, VSENSE3	-0.3	20	
	COMP2, COMP3	-0.3	20	
	VMON2, VMON3	-0.3	20	
Linear regulator	BOOTx – PHx	-0.3	8	V
	LDO_OUT	-0.3	8	
Boost converter	VSENSE4	-0.3	20	V
	VSENSE5	-0.3	20	
	PH5	-0.3	20	
Digital interface	COMP5	-0.3	20	V
	CSN, SCK, SDO, SDI, WD, HSPWM	-0.3	5.5	
Wake input	RESN, PRESN, IRQ	-0.3	20	V
Wake input	WAKE	-1 <sup>(3)</sup>	60	V
Protection FET	GPFET	-0.3	80	V
	VIN – GPFET	-0.3	20	
Battery sense input	VSENSE	-1 <sup>(3)</sup>	60 Transients up to 80 V <sup>(4)</sup>	V
Temperature sense	VT	-0.3	5.5	V
	VT_REF	-0.3	20	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) Maximum 3.5 A

(3)  $I_{max} = 100$  mA

(4) Internally clamped to 60-V, 20-k $\Omega$  external resistor required, current into pin limited to 1 mA.



## Absolute Maximum Ratings (continued)

 over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Reference voltage	VREF	-0.3	5.5	V
High-side and LED driver	HSENSE	-0.3	60	V
	HSCTRL	-0.3	60	
	VINPROT-HSENSE, VINPROT-HSCTRL	-0.3	20	
Driver supply decoupling	VREG	-0.3	8	V
Supply decoupling	DVDD	-0.3	3.6	V
Temperature ratings	Junction temperature range, $T_J$	-55	150	°C
	Operating temperature range, $T_A$	-55	125	
	Storage temperature, $T_{stg}$	-55	165	

## 7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 <sup>(1)</sup>		±1000	V
		VT pin	±150	
	Charged-device model (CDM), per AEC Q100-011	Corner pins (1, 14, 15, 28, 29, 42, 43, and 56)	±750	
		All other pins	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
Supply voltage at VIN, VINPROT, VSSENSE			4.8		40	V
$T_A$ Operating free air temperature	All electrical characteristics in specification		-40		125	°C
	Shutdown comparator and internal voltage regulators in specification		-55		125	
$T_J$ Operating virtual junction temperature	All electrical characteristics in specification				150	°C
	Shutdown comparator and internal voltage regulators in specification				150	

## 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TPS65311-Q1		UNIT
		RWE (VQFN)	RVJ (VQFN)	
		56 PINS	56 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	22.1	22.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	9.6	9.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	6.2	6.3	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	0.1	0.1	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	6.2	6.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.4	0.7	°C/W

 (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.



## 7.5 Electrical Characteristics

VIN = VINPROT 4.8 V to 40 V, VSUPx = 3 V to 5.5 V, EXTSUP = 0 V, T<sub>J(max)</sub> = 150°C, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>INPUT VOLTAGE-CURRENT CONSUMPTION</b>						
V <sub>IN</sub>	Device operating range	Buck regulator operating range, Voltage on VIN and VINPROT pins	4		50	V
V <sub>POR</sub>	Power-on reset threshold	Falling VIN	3.5	3.6	3.8	V
		Rising VIN	3.9	4.2	4.3	
V <sub>POR_hyst</sub>	Power-on reset hysteresis on VIN		0.47	0.6	0.73	V
I <sub>LPM0</sub>	LPM0 current consumption <sup>(1)(2)</sup>	All off, wake active, V <sub>IN</sub> = 13 V Total current into VSSENSE, VIN and VINPROT			44	μA
I <sub>LPM0</sub>	LPM0 current (commercial vehicle application) consumption <sup>(3)(2)</sup>	All off, wake active, V <sub>IN</sub> = 24.5 V Total current into VSSENSE, VIN and VINPROT			60	μA
I <sub>ACTIVE1</sub>	ACTIVE total current consumption <sup>(1)(4)</sup>	BUCK1 = on, V <sub>IN</sub> = 13 V, EXTSUP = 0 V, Q <sub>g</sub> of BUCK1 FETs = 15 nC. Total current into VSSENSE, VIN and VINPROT		32		mA
I <sub>ACTIVE123</sub>	ACTIVE total current consumption <sup>(1)(4)</sup>	BUCK1/2/3 = on, V <sub>IN</sub> = 13 V, Q <sub>g</sub> of BUCK1 FETs = 15 nC. Total current into VSSENSE, VIN and VINPROT		40		mA
I <sub>ACTIVE1235</sub>	ACTIVE current consumption <sup>(1)(4)</sup>	BUCK1/2/3, LDO, BOOST, high-side switch = on, V <sub>IN</sub> = 13 V, Q <sub>g</sub> of BUCK1 FETs = 15 nC. EXTSUP = 5 V from BOOST Total current into VSSENSE, VIN and VINPROT		31		mA
I <sub>ACTIVE1235_noEXT</sub>	ACTIVE current consumption <sup>(1)(4)</sup>	BUCK1/2/3, LDO, BOOST, high-side switch = on, V <sub>IN</sub> = 13 V, Q <sub>g</sub> of BUCK1 FETs = 15 nC, EXTSUP = open Total current into VSENSE, VIN and VINPROT		53		mA
<b>BUCK CONTROLLER (BUCK1)</b>						
V <sub>BUCK1</sub>	Adjustable output voltage range		3		11	V
V <sub>Sense1_NRM</sub>	Internal reference voltage in operating mode	VSENSE1 pin, load = 0 mA, Internal REF = 0.8 V	-1%		1%	
V <sub>S1-2</sub>	VS1-2 for forward OC in CCM	Maximum sense voltage VSENSE1 = 0.75 V (low duty cycle)	60	75	90	mV
		Minimum sense voltage VSENSE1 = 1 V (negative current limit)	-65	-37.5	-23	
A <sub>CS</sub>	Current sense voltage gain	ΔVCOMP1 / Δ(VS1 - VS2)	4	8	12	V/V
I <sub>Gpeak</sub>	Gate driver peak current	VREG = 5.8 V		0.6		A
R <sub>DSON_DRIVER</sub>	Source and sink driver	I <sub>G</sub> current for external MOSFET = 200 mA, VREG = 5.8 V, V <sub>BOOT1-PH1</sub> = 5.8 V		5	10	Ω
V <sub>DIO1</sub>	Bootstrap diode forward voltage	I <sub>BOOT1</sub> = -200 mA, VREG-BOOT1	0.8		1.1	V
<b>ERROR AMPLIFIER (OTA) FOR BUCK CONTROLLERS AND BOOST CONVERTER</b>						
g <sub>mEA</sub>	Forward transconductance	COMP1/2/3/5 = 0.8 V; source/sink = 5 μA, Test in feedback loop		0.9		mS
A <sub>EA</sub>	Error amplifier DC gain		60			dB
<b>SYNCHRONOUS BUCK CONVERTER BUCK2 AND BUCK3 (BUCK2/3)</b>						
VSUP2/3	Supply voltage		3		11	V
V <sub>BUCK2/3</sub>	Regulated output voltage range	I <sub>load</sub> = 0...2 A VSUPx = V <sub>BUCK2/3</sub> + I <sub>load</sub> × 0.2 Ω	0.8		5.5	V
R <sub>DSON-HS</sub>	R <sub>DSON</sub> high-side switch	V <sub>BOOTx -PHx</sub> = 5.8 V			0.20	Ω
R <sub>DSON-LS</sub>	R <sub>DSON</sub> low-side switch	VREG = 5.8 V			0.20	Ω
I <sub>HS-Limit</sub>	High-side switch current-limit	Static current limit test. In application L > 1 μH at I <sub>HS-Limit</sub> and I <sub>LS-Limit</sub> to limit di / dt	2.5	2.9	3.3	A
I <sub>LS-Limit</sub>	Low-side switch current-limit	Static current limit test. In application L > 1 μH at I <sub>HS-Limit</sub> and I <sub>LS-Limit</sub> to limit di / dt	2	2.5	3	A

(1) T<sub>A</sub> = 25°C

(2) Quiescent Current Specification does not include the current flow through the external feedback resistor divider. Quiescent Current is non-switching current, measured with no load on the output with V<sub>BAT</sub> = 13 V.

(3) T<sub>A</sub> = 130°C

(4) Total current consumption measured on EVM includes switching losses.

**Electrical Characteristics (continued)**

 VIN = VINPROT 4.8 V to 40 V, VSUPx = 3 V to 5.5 V, EXTSUP = 0 V, T<sub>J(max)</sub> = 150°C, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VSUP <sub>Lkg</sub>	VSUP leakage current	VSUP = 10 V for high side, controller disabled, T <sub>J</sub> = 100°C		1	2	μA
V <sub>Sense2/3</sub>	Feedback voltage	With respect to the 800-mV internal reference	-1%		1%	
COMP2/3 <sub>H</sub> TH	COMP2/3 Input threshold low		0.9		1.5	V
COMP2/3 <sub>L</sub> TH	COMP2/3 Input threshold high		VREG - 1.2		VREG - 0.3	V
R <sub>TIEOFF COMP23</sub>	COMP2/3 internal tie-off	BUCK2/3 enabled. Resistor to VREG and GND, each	70	100	130	kΩ
V <sub>DIO2 3</sub>	Bootstrap diode forward voltage	I <sub>BOOT1</sub> = -200 mA, VREG-BOOT2, VREG-BOOT3		1.1	1.2	V
<b>BOOST CONVERTER</b>						
V <sub>Boost</sub>	Boost adjustable output voltage range	Using 3.3-V input voltage, leak_switch ≤ 1 A	4.5		15	V
V <sub>Boost</sub>	Boost adjustable output voltage range	Using 3.3-V input voltage I <sub>loadmax</sub> = 20 mA, I <sub>peak_switch</sub> = 0.3 A	15		18.5	V
R <sub>DS-ON_BOOST</sub>	Internal switch on-resistance	VREG = 5.8 V		0.3	0.5	Ω
V <sub>Sense5</sub>	Feedback voltage	With respect to the 800-mV internal reference	-1%		1%	
I <sub>CLBOOST</sub>	Internal switch current-limit		1		1.5	A
<b>LINEAR REGULATOR LDO</b>						
VSUP4	Device operating range for LDO	Recommended operating range	3		7	V
V <sub>LDO</sub>	Regulated output range	I <sub>OUT</sub> = 1 mA to 350 mA	0.8		5.25	V
V <sub>RefLDO</sub>	DC output voltage tolerance at VSENSE4	VSENSE4 = 0.8 V (regulated at internal ref) VSUP4 = 3 V to 7 V, I <sub>OUT</sub> = 1 mA to 350 mA	-2%		2%	
V <sub>step1</sub>	Load step 1	VSENSE4 = 0.8 V (regulated at internal ref) I <sub>OUT</sub> = 1 mA to 101 mA, C <sub>LDO</sub> = 6 to 50 μF, t <sub>rise</sub> = 1 μs	-2%		2%	
V <sub>Sense4</sub>	Feedback voltage	With respect to the 800-mV internal reference	-1%		1%	
V <sub>Dropout</sub>	Drop out voltage	I <sub>OUT</sub> = 350 mA, T <sub>J</sub> = 25°C		127	143	mV
		I <sub>OUT</sub> = 350 mA, T <sub>J</sub> = 125°C		156	180	
		I <sub>OUT</sub> = 350 mA, T <sub>J</sub> = 150°C		275	335	
I <sub>OUT</sub>	Output current	V <sub>OUT</sub> in regulation	-350		-1	mA
I <sub>LDO-CL</sub>	Output current limit	V <sub>OUT</sub> = 0 V, VSUP4 = 3 V to 7 V	-1000		-400	mA
PSRR <sub>LDO</sub>	Power supply ripple rejection	V <sub>ripple</sub> = 0.5 V <sub>PP</sub> , I <sub>OUT</sub> = 300 mA, C <sub>LDO</sub> = 10 μF	Freq = 100 Hz		60	dB
			Freq = 4 kHz		50	
			Freq = 150 kHz		25	
LDOns <sub>10-100</sub>	Output noise 10 Hz – 100 Hz	10-μF output capacitance, V <sub>LDO</sub> = 2.5 V			20	μV/√(Hz)
LDOns <sub>100-1k</sub>	Output noise 100 Hz – 10 kHz	10-μF output capacitance, V <sub>LDO</sub> = 2.5 V			6	μV/√(Hz)
C <sub>LDO</sub>	Output capacitor	Ceramic capacitor with ESR range, C <sub>LDO_ESR</sub> = 0 to 100 mΩ	6		50	μF
<b>LED AND HIGH-SIDE SWITCH CONTROL</b>						
V <sub>HSENSE</sub>	Current sense voltage	VINPROT – HSENSE, high-side switch in current limit	370	400	430	mV
V <sub>CMHSENSE</sub>	Common mode range for current sensing	See VINPROT	4		60	V
V <sub>HSOL_TH</sub>	VINPROT – HSENSE open load threshold	Ramping negative	5	20	35	mV
		Ramping positive	26	38	50	
V <sub>HSOL_HY</sub>	Open load hysteresis		10	18	28	mV
V <sub>HS_SC</sub>	VINPROT – HSENSE load short detection threshold	Ramping positive	88%	92.5%	96%	V <sub>HSENSE</sub>
		Ramping negative from load short condition	87	90	93	% of V <sub>HSENSE</sub>
V <sub>HSSC_HY</sub>	VINPROT – HSENSE short circuit hysteresis		1			% of V <sub>HSENSE</sub>
V <sub>HSCTRL<sub>OFF</sub></sub>	Voltage at HSCTRL when OFF		VINPROT - 0.5		VINPROT	V
V <sub>GS</sub>	Clamp voltage between HSENSE – HSCTRL		6.1	7.7	8.5	V

## Electrical Characteristics (continued)

VIN = VINPROT 4.8 V to 40 V, VSUPx = 3 V to 5.5 V, EXTSUP = 0 V, T<sub>J(max)</sub> = 150°C, unless otherwise noted

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT			
V <sub>OS_HS</sub>	Overshoot during turn-on	V <sub>OS_HS</sub> = VINPROT - HSENSE			400	mV		
I <sub>CL_HSCTRL</sub>	HSCTRL current-limit	2	4.1	5	mA			
R <sub>PU_HSCTRL</sub>	Internal pullup resistors	Between VINPROT and HSCTRL			70	100	130	kΩ
R <sub>PU_HSCTRL-HSENSE</sub>		Between HSCTRL and HSENSE			70	100	130	
V <sub>I_high</sub>	High level input voltage	HSPWM, VIO = 3.3 V			2		V	
V <sub>I_low</sub>	Low level input voltage	HSPWM, VIO = 3.3 V				0.8	V	
V <sub>I_hys</sub>	Input voltage hysteresis	HSPWM, VIO = 3.3 V			150	500	mV	
R <sub>SENSE</sub>	External sense resistor	Design info, no device parameter			1.5	50	Ω	
C <sub>GS</sub>	External MOSFET gate source capacitance				100	2000	pF	
C <sub>GD</sub>	External MOSFET gate drain capacitance					500	pF	
<b>REFERENCE VOLTAGE</b>								
V <sub>REF</sub>	Reference voltage				3.3		V	
V <sub>REF-tol</sub>	Reference voltage tolerance	I <sub>VREF</sub> = 5 mA			-1%	1%		
I <sub>REFCL</sub>	Reference voltage current-limit				10	25	mA	
C <sub>VREF</sub>	Capacitive load				0.6	5	μF	
REFns10-100	Output noise 10 Hz–100 Hz	2.2 μF output capacitance, I <sub>VREF</sub> = 5 mA				20	μV/√(Hz)	
REFns100-1k	Output noise 100 Hz–10 kHz	2.2 μF output capacitance, I <sub>VREF</sub> = 5 mA				6	μV/√(Hz)	
V <sub>REF_OK</sub>	Reference voltage OK threshold	Threshold, V <sub>REF</sub> falling			2.91	3.07	3.12	V
		Hysteresis			14	70	140	mV
<b>SHUTDOWN COMPARATOR</b>								
V <sub>T_REF</sub>	Shutdown comparator reference voltage	I <sub>VT_REF</sub> = 20 μA. Measured as drop voltage with respect to VD <sub>VDD</sub>			10	17	500	mV
		I <sub>VT_REF</sub> = 600 μA. Measured as drop voltage with respect to VD <sub>VDD</sub> . No V <sub>T_REF</sub> short-circuit detection.			200	420	1100	
I <sub>VT_REFCL</sub>	Shutdown comparator reference current limit	V <sub>T_REF</sub> = 0			0.6	1	1.4	mA
V <sub>VT_REF SH</sub>	V <sub>T_REF</sub> short circuit detection	Threshold, V <sub>T_REF</sub> falling. Measured as drop voltage with respect to VD <sub>VDD</sub>			0.9	1.2	1.8	V
		Hysteresis				130		mV
V <sub>T_TH-H</sub>	Input voltage threshold on V <sub>T</sub> , rising edge triggers shutdown	This feature is specified by design to work down to -55°C.			0.48	0.50	0.52	V <sub>T_REF</sub>
V <sub>T_TH-L</sub>	Input voltage threshold on V <sub>T</sub> , falling voltage enables device operation	This feature is specified by design to work down to -55°C.			0.46	0.48	0.52	V <sub>T_REF</sub>
V <sub>T_TOL</sub>	Threshold variation	V <sub>T_TH-H</sub> - V <sub>T_REF</sub> / 2, V <sub>T_TH-L</sub> - V <sub>T_REF</sub> / 2			-20		20	mV
I <sub>VT_leak</sub>	Leakage current	T <sub>J</sub> : -20°C to 125°C			-400		-50	nA
		T <sub>J</sub> : -55°C to -20°C			-200		-50	
V <sub>T_REF_OV</sub>	V <sub>T_REF</sub> overvoltage threshold	Threshold, V <sub>T_REF</sub> rising. Measured as drop voltage with respect to VD <sub>VDD</sub>			0.42	0.9	1.2	V
		Hysteresis				100		mV
<b>WAKE INPUT</b>								
V <sub>WAKE_ON</sub>	Voltage threshold to enable device	WAKE pin is a level sensitive input			3.3		3.7	V
<b>VBAT UNDERVOLTAGE WARNING</b>								
V <sub>SSENSETH_L</sub>	V <sub>SENSE</sub> falling threshold low	SPI selectable, default after reset			4.3		4.7	V
V <sub>SSENSETH_H</sub>	V <sub>SENSE</sub> falling threshold high	SPI selectable			6.2		6.8	V
V <sub>SSENSE-HY</sub>	V <sub>SENSE</sub> hysteresis					0.2		V
I <sub>VSLEAK</sub>	Leakage current at V <sub>SENSE</sub>	LPM0 mode, V <sub>SENSE</sub> 55 V					1	μA
I <sub>VSLEAK60</sub>	Leakage current at V <sub>SENSE</sub>	LPM0 mode, V <sub>SENSE</sub> 60 V					100	μA
I <sub>VSLEAK80</sub>	Leakage current at V <sub>SENSE</sub>	LPM0 mode, V <sub>SENSE</sub> 80 V			5		25	mA

**Electrical Characteristics (continued)**

 VIN = VINPROT 4.8 V to 40 V, VSUPx = 3 V to 5.5 V, EXTSUP = 0 V, T<sub>J(max)</sub> = 150°C, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R <sub>VSSENSE</sub>	Internal resistance from VSSENSE to GND	VSSENSE = 14 V, disabled in LPM0 mode	0.7	1	1.3	MΩ
<b>VIN OVERVOLTAGE PROTECTION</b>						
V <sub>OVTH_H</sub>	VIN overvoltage shutdown threshold 1 (rising edge)	Selectable with SPI	50		60	V
V <sub>OVTH_L</sub>	VIN overvoltage shutdown threshold 2 (rising edge)	Selectable with SPI, default after reset	36		38	V
V <sub>OVHY</sub>	VIN overvoltage hysteresis	Threshold 1	0.2	1.7	3	V
		Threshold 2 - default after reset	1.5	2	2.5	
<b>WINDOW WATCHDOG</b>						
V <sub>I_high</sub>	High level input voltage	WD, VIO = 3.3 V	2			V
V <sub>I_low</sub>	Low level input voltage	WD, VIO = 3.3 V			0.8	V
V <sub>I_hys</sub>	Input voltage hysteresis	WD, VIO = 3.3 V	150		500	mV
<b>RESET AND IRQ BLOCK</b>						
V <sub>RESL</sub>	Low level output voltage at RESN, PRESN and IRQ	VIN ≥ 3 V, I <sub>xRESN</sub> = 2.5 mA	0		0.4	V
V <sub>RESL</sub>	Low level output voltage at RESN and PRESN	VIN = 0 V, VIO = 1.2 V, I <sub>xRESN</sub> = 1 mA	0		0.4	V
I <sub>RESLeak</sub>	Leakage current at RESN, PRESN and IRQ	V <sub>rest</sub> = 5.5 V			1	μA
N <sub>RES</sub>	Number of consecutive reset events for transfer to LPM0			7		
<b>EXTERNAL PROTECTION</b>						
VCLAMP	Gate to source clamp voltage	VIN - GPFET, 100 μA	14		20	V
IGPFET	Gate turn on current	VIN = 14 V, GPFET = 2 V	15		25	μA
RDSONGFET	Gate driver strength	VIN = 14 V, turn off			25	Ω
<b>THERMAL SHUTDOWN AND OVERTEMPERATURE PROTECTION</b>						
T <sub>SDTH</sub>	Thermal shutdown	Junction temperature	160	175		°C
T <sub>SDHY</sub>	Hysteresis			20		°C
T <sub>OTTH</sub>	Overtemperature flag	Overtemperature flag is implemented as local temp sensors and expected to trigger before the thermal shutdown	150	165		°C
T <sub>OTHY</sub>	Hysteresis			20		°C
<b>VOLTAGE MONITORS BUCK1/2/3, VIO, LDO, BOOSTER</b>						
V <sub>MONTH_L</sub>	Voltage monitor reference	REF = 0.8 V – falling edge	90%	92%	94%	
V <sub>MONTH_H</sub>	Voltage monitor reference	REF = 0.8 V – rising edge	106%	108%	110%	
V <sub>MON_HY</sub>	Voltage monitor hysteresis			2%		
V <sub>VIOMON_TH</sub>	Undervoltage monitoring at VIO – falling edge		3		3.13	V
V <sub>VIOMON_HY</sub>	UV_VIO hysteresis			0.05		V
<b>GND LOSS</b>						
V <sub>GLTH-low</sub>	GND loss threshold low	GND to PGNDx	-0.31	-0.25	-0.19	V
V <sub>GLTH-high</sub>	GND loss threshold high	GND to PGNDx	0.19	0.25	0.31	V
<b>INTERNAL VOLTAGE REGULATORS</b>						
V <sub>REG</sub>	Internal regulated supply	I <sub>VREG</sub> = 0 mA to 50 mA, VINPROT = 6.3 V to 40 V and EXTSUP = 6.3 V to 12 V	5.5	5.8	6.1	V
V <sub>EXTSUP-TH</sub>	Switch over voltage	I <sub>VREG</sub> = 0 mA to 50 mA and EXTSUP ramping positive, ACTIVE mode	4.4	4.6	4.8	V
V <sub>EXTSUP-HY</sub>	Switch over hysteresis		100	200	300	mV
V <sub>REGDROP</sub>	Drop out voltage on VREG	I <sub>VREG</sub> = 50 mA, EXTSUP = 5 V / VINPROT = 5 V and EXTSUP = 0 V / VINPROT = 4 V			200	mV
I <sub>REG_CL</sub>	Current limit on VREG	EXTSUP = 0 V, VREG = 0 V	-250		-50	mA
I <sub>REG_EXTSUP_CL</sub>		EXTSUP ≥ 4.8 V, VREG = 0 V	-250		-50	mA
C <sub>VREG</sub>	Capacitive load		1.2	2.2	3.3	μF

## Electrical Characteristics (continued)

VIN = VINPROT 4.8 V to 40 V, VSUPx = 3 V to 5.5 V, EXTSUP = 0 V, T<sub>J(max)</sub> = 150°C, unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>REG-OK</sub>	VREG undervoltage threshold	VREG rising	3.8	4	4.2	V
		Hysteresis	350	420	490	mV
VDVDD	Internal regulated low voltage supply		3.15	3.3	3.45	V
VDVDD UV	DVDD undervoltage threshold	DVDD falling	2.1			V
VDVDD OV	DVDD overvoltage threshold	DVDD rising			3.8	V
<b>SPI</b>						
V <sub>I,high</sub>	High level input voltage	CSN, SCK, SDI; VIO = 3.3 V	2			V
V <sub>I,low</sub>	Low level input voltage	CSN, SCK, SDI; VIO = 3.3 V			0.8	V
V <sub>I,hys</sub>	Input voltage hysteresis	CSN, SCK, SDI; VIO = 3.3 V	150		500	mV
V <sub>O,high</sub>	SDO output high voltage	VIO = 3.3 V I <sub>SDO</sub> = 1 mA	3			V
V <sub>O,low</sub>	SDO output low voltage	VIO = 3.3 V I <sub>SDO</sub> = 1 mA			0.2	V
CSDO	SDO capacitance				50	pF
<b>GLOBAL PARAMETERS</b>						
R <sub>PU</sub>	Internal pullup resistor at CSN pin		70	100	130	kΩ
R <sub>PD</sub>	Internal pulldown resistor at pins: HSPWM, SDI, SCK, WD, S2 <sup>(5)</sup>		70	100	130	kΩ
R <sub>PD-WAKE</sub>	Internal pulldown resistor at WAKE pin		140	200	260	kΩ
I <sub>LKG</sub>	Input pullup current at pins: - VSENSE1–5 - VMON1–3	V <sub>TEST</sub> = 0.8 V	–200	–100	–50	nA

(5) RAMP and ACTIVE only

## 7.6 Timing Requirements

		MIN	TYP	MAX	UNIT	
<b>BUCK CONTROLLER (BUCK1)</b>						
t <sub>OCBUCK1_BLK</sub>	RSTN and ERROR mode transition, when over current detected for > t <sub>OCBUCK1_BLK</sub>		1		ms	
<b>LED AND HIGH-SIDE SWITCH CONTROL</b>						
t <sub>HSOL_BLK</sub>	Open load blanking time	70	100	140	μs	
t <sub>HSS_CL</sub>	Net time in current limit to disable driver	4	5	6	ms	
t <sub>S_HS</sub>	Current-limit sampling interval		100		μs	
t <sub>ON</sub>	Turnon time	Time from rising HSPWM till high-side switch in current limitation, ±5% settling		30	μs	
		Time from rising HSPWM till high-side switch till voltage-clamp between HSENSE – HSCTRL active (within V <sub>GS</sub> limits)		30	60	μs
f <sub>HS_IN</sub>	HSPWM input frequency	Design information, no device parameter		100	500	Hz
<b>REFERENCE VOLTAGE</b>						
T <sub>REF_OK</sub>	Reference voltage OK deglitch time	10		20	μs	
<b>SHUTDOWN COMPARATOR</b>						
T <sub>VT_REF_FLT</sub>	VT_REF fault deglitch time	Overvoltage or short condition on VT_REF		10	20	μs
<b>WAKE INPUT</b>						
t <sub>WAKE</sub>	Min. pulse width at WAKE to enable device	V <sub>WAKE</sub> = 4 V to suppress short spikes at WAKE pin		10	20	μs
<b>VBAT UNDERVOLTAGE WARNING</b>						
t <sub>VSENSE_BLK</sub>	Blanking time	V <sub>VSENSE</sub> < V <sub>SSENSETH_xx</sub> → IRQ asserted		10	35	μs
<b>VIN OVERVOLTAGE PROTECTION</b>						
t <sub>OFF_BLK-H</sub>	OV delay time	VIN > V <sub>OVTH_H</sub> → GPFET off		1		μs
t <sub>OFF_BLK-L</sub>	OV blanking time	VIN > V <sub>OVTH_L</sub> → GPFET off		10	20	μs

**Timing Requirements (continued)**

		MIN	TYP	MAX	UNIT		
<b>WINDOW WATCHDOG</b>							
$t_{\text{timeout}}$	Timeout	230	300	370	ms		
$t_{\text{WD}}$	Watchdog window time	Spread spectrum disabled		18	20	22	ms
		Spread spectrum enable		19.8	22	24.2	
$t_{\text{WD\_FAIL}}$	Closed window time	$t_{\text{WD}} / 4$					
$t_{\text{WD\_BLK}}$	WD filter time				1.2	$\mu\text{s}$	
<b>RESET AND IRQ BLOCK</b>							
$t_{\text{RESHOLD}}$	RESN hold time	1.8	2	2.2	ms		
$t_{\text{IRQHOLD}}$	IRQ hold time	After $V_{\text{VSENSE}} < V_{\text{SSENSETH}}$ for $t_{\text{VSENSE\_BLK}}$		10	20	$\mu\text{s}$	
$t_{\text{DR\_IRQ\_PRESN}}$	Rising edge delay of IRQ to rising edge of PRESN				2	$\mu\text{s}$	
$t_{\text{DF\_RESN\_PRESN}}$	Falling edge delay of RESN to PRESN / IRQ				2	$\mu\text{s}$	
<b>THERMAL SHUTDOWN AND OVERTEMPERATURE PROTECTION</b>							
$t_{\text{SD\_BLK}}$	Blanking time before thermal shutdown	10			20	$\mu\text{s}$	
$t_{\text{OT\_BLK}}$	Blanking time before thermal over temperature	10			20	$\mu\text{s}$	
<b>VOLTAGE MONITORS BUCK1/2/3, VIO, LDO, BOOSTER</b>							
$t_{\text{VMON\_BLK}}$	Blanking time between UV/OV condition to RESN low	UV/OV: BUCK1/2/3 UV: VIO		10	20	$\mu\text{s}$	
$t_{\text{VMONTHL\_BLK}}$	Blanking time between undervoltage condition to ERROR mode transition or corresponding SPI bit	BUCK1/2/3 → ERROR mode LDO or BOOST → SPI bit set or turn off		1		ms	
$t_{\text{VMONTHL\_BLK1}}$	Blanking time between undervoltage condition to ERROR mode transition	VIO only		10	20	$\mu\text{s}$	
$t_{\text{VMONTHH\_BLK1}}$	Blanking time between overvoltage condition to ERROR mode transition	BUCK1/2/3 → ERROR mode VIO has no OV protection		10	20	$\mu\text{s}$	
$t_{\text{VMONTHH\_BLK2}}$	Blanking time LDO and BOOST overvoltage condition to corresponding SPI bit or ERROR mode	LDO or BOOST (ACTIVE mode) → SPI bit set or turn off LDO (VTCHECK or RAMP mode) → ERROR mode		20	40	$\mu\text{s}$	
<b>GND LOSS</b>							
$t_{\text{GL\_BLK}}$	Blanking time between GND loss condition and transition to ERROR state	5			20	$\mu\text{s}$	
<b>POWER-UP SEQUENCING</b>							
$t_{\text{START1}}$	Soft start time of BOOST	From start till exceeding $V_{\text{MONTH\_L}} + V_{\text{MON\_HY}}$ Level		0.7	2.7	ms	
$t_{\text{START2}}$	Soft start time of BUCK1/2/3 and LDO	From start till exceeding $V_{\text{MONTH\_L}} + V_{\text{MON\_HY}}$ Level		0.5	2	ms	
$t_{\text{START}}$	Startup DVDD regulator	From start till exceeding $V_{\text{MONTH\_L}} + V_{\text{MON\_HY}}$ Level		3		ms	
$t_{\text{SEQ2}}$	Sequencing time from start of BUCK1 to BUCK2 and BOOST	Internal SSDONE_BUCK1 signal		3		ms	
$t_{\text{WAKE-RES}}$	Startup time from entering TESTSTART to RESN high	GPFET = IRFR6215		14		ms	
$t_{\text{SEQ1}}$	Sequencing time from start of BOOST to BUCK3	Internal SSDONE_BOOST signal		1	4	ms	
<b>INTERNAL VOLTAGE REGULATORS</b>							
$t_{\text{DVDD\_OV}}$	Blanking time from DVDD overvoltage condition to shutdown mode transition	10			20	$\mu\text{s}$	
<b>SPI INTERFACE</b>							
$t_{\text{SPI}}$	SCK period	See <a href="#">Figure 1</a>		240		ns	
$t_{\text{SCKL}}$	SCK low time			100		ns	
$t_{\text{SCKH}}$	SCK high time			100		ns	
$t_{\text{FSIV}}$	Time between falling edge of CSN and SDO output valid (FSI bit)	Falling SDO < 0.8 V; Rising SDO > 2 V, See <a href="#">Figure 1</a>		80		ns	
$t_{\text{SDOV}}$	Time between rising edge of SCK and SDO data valid	Falling SDO < 0.8 V; Rising SDO > 2 V, See <a href="#">Figure 1</a>		55		ns	
$t_{\text{SDIS}}$	Setup time of SDI before falling edge of SCK	See <a href="#">Figure 1</a>		20		ns	
$t_{\text{SDOH}}$	Hold time of SDO after rising edge of SCK			5		ns	
$t_{\text{HCS}}$	Hold time of CSN after last falling edge of SCK			50		ns	
$t_{\text{SDOtri}}$	Delay between rising edge of CSN and SDO 3-state	See <a href="#">Figure 1</a>		80		ns	

### Timing Requirements (continued)

		MIN	TYP	MAX	UNIT
$t_{\min2SPI}$	Minimum time between two SPI commands	10			$\mu\text{s}$

### 7.7 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>BUCK CONTROLLER (BUCK1)</b>					
$f_{\text{SWBUCK1}}$	Switching frequency		$f_{\text{OSC}} / 10$		
DC	Duty cycle	High-side minimum on time	100		ns
		Maximum duty cycle	98.75%		
$t_{\text{DEAD\_BUCK1}}$	Shoot-through delay, blanking time		25		ns
<b>SYNCHRONOUS BUCK CONVERTER BUCK2/3</b>					
$f_{\text{SWLBUCK2/3}}$	Buck switching frequency		$f_{\text{OSC}} / 2$		
$\text{DC}_{\text{BUCK2/3}}$	Duty cycle	High-side minimum on time	50		ns
		Maximum duty cycle	99.8%		
$t_{\text{DEAD\_BUCK2/3}}$	Shoot-through delay		20		ns
<b>BOOST CONVERTER</b>					
$f_{\text{SWLBOOST}}$	Boost switching frequency		$f_{\text{OSC}} / 2$		
$\text{DC}_{\text{BOOST}}$	Maximum internal MOSFET duty cycle at $f_{\text{SWLBOOST}}$		75%		
<b>GLOBAL PARAMETERS</b>					
$f_{\text{OSC}}$	Internal oscillator used for Buck or Boost switching frequency	4.6	4.9	5.2	MHz
$f_{\text{spread}}$	Spread spectrum frequency range	$0.8 \times f_{\text{OSC}}$		$f_{\text{OSC}}$	

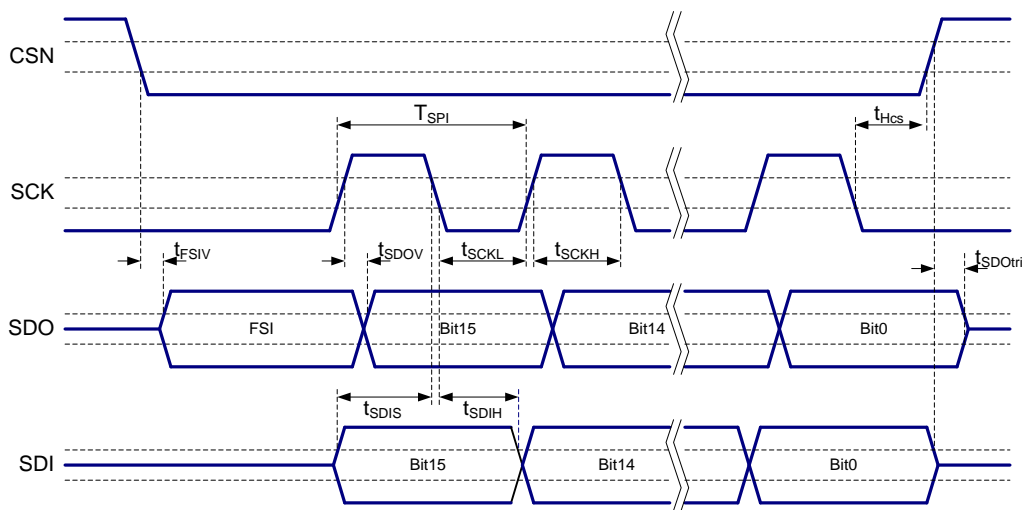


Figure 1. SPI Timing



## 7.8 Typical Characteristics

All parameters are measured on a TI EVM, unless otherwise specified.

### 7.8.1 BUCK 1 Characteristics

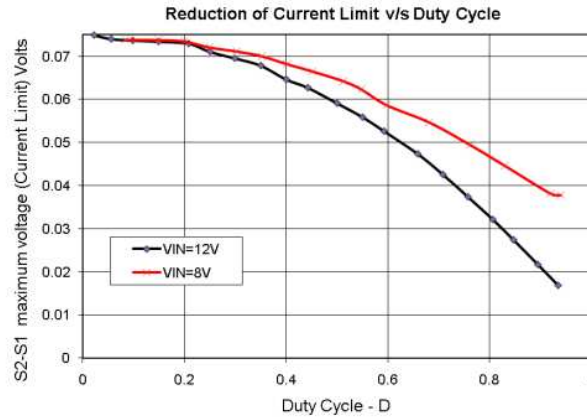
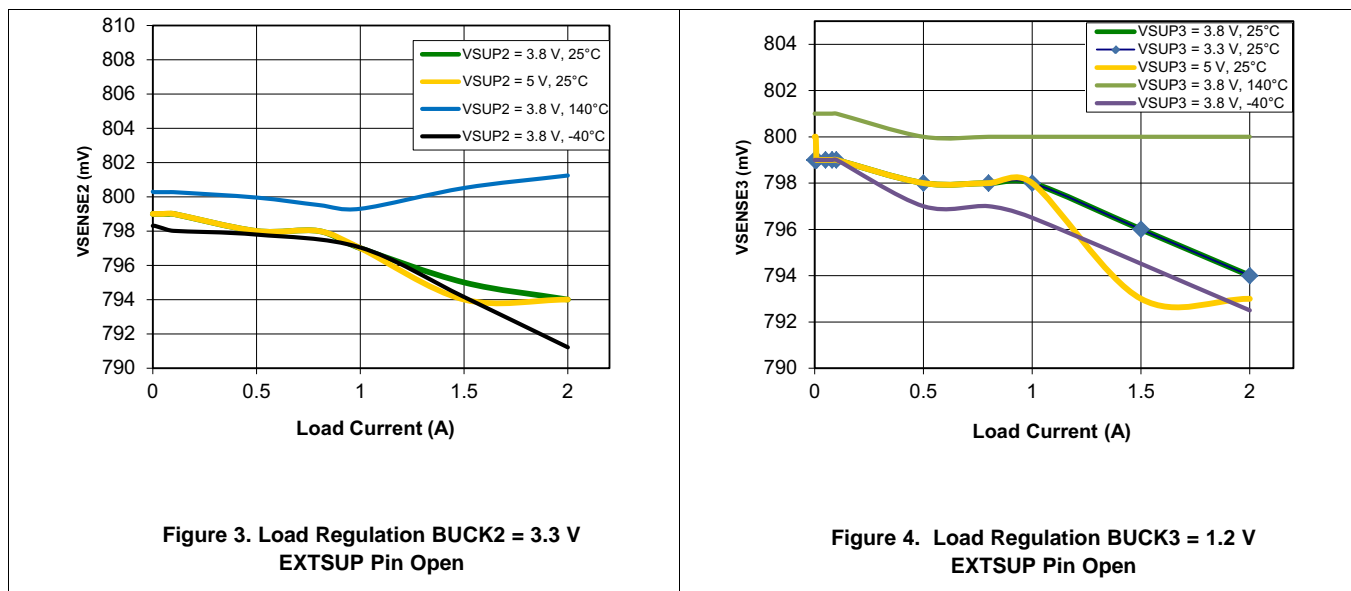
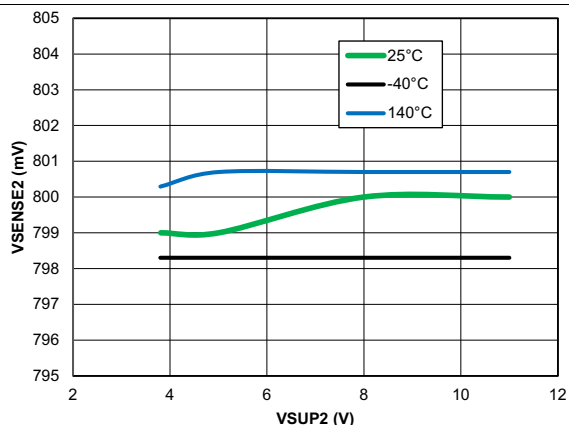


Figure 2. Reduction of Current-Limit vs Duty Cycle

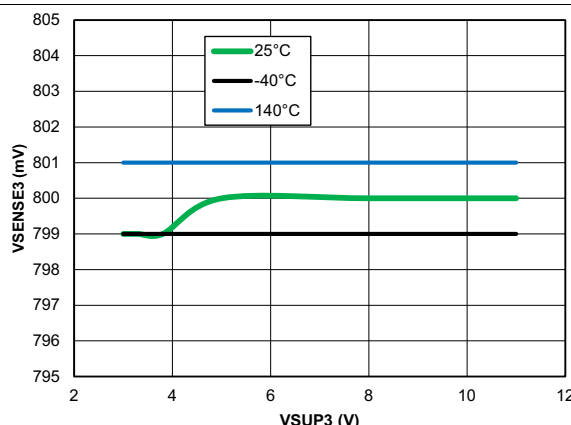
### 7.8.2 BUCK 2 and BUCK3 Characteristics



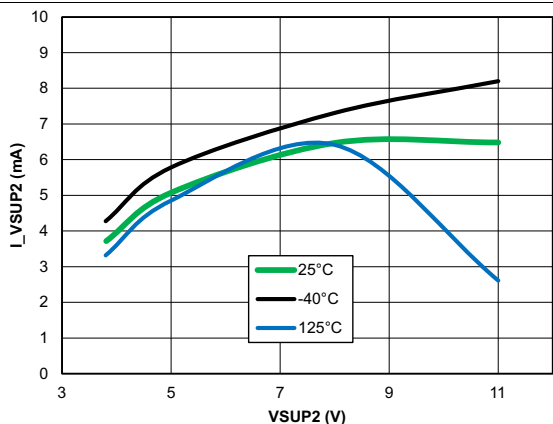
**BUCK 2 and BUCK3 Characteristics (continued)**



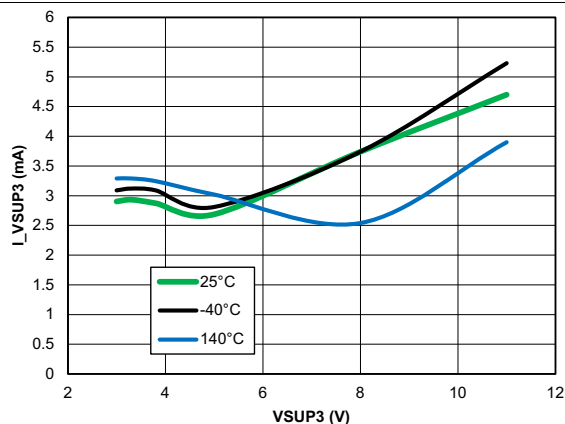
**Figure 5. Open-Load Line Regulation BUCK2 = 3.3 V  
EXTSUP Pin Open**



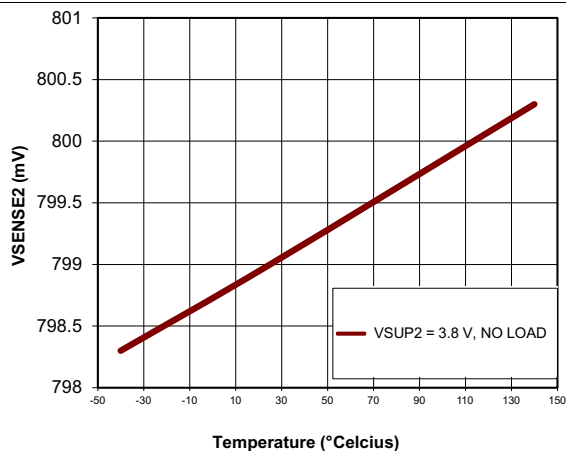
**Figure 6. Open-Load Line Regulation BUCK3 = 1.2 V  
EXTSUP Pin Open**



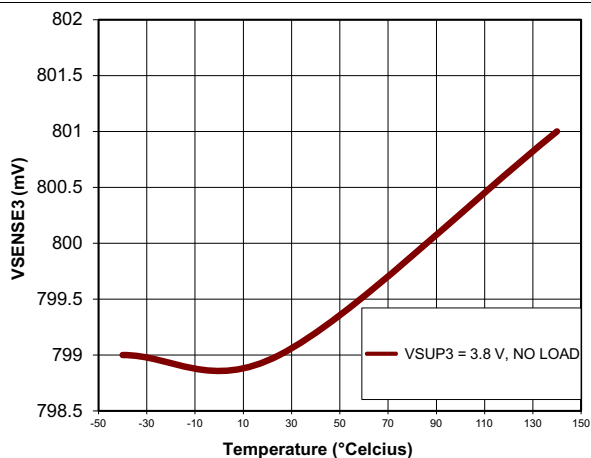
**Figure 7. Open-Load Supply Current BUCK2 = 3.3 V  
EXTSUP Pin Open**



**Figure 8. Open-Load Supply Current BUCK3 = 1.2 V  
EXTSUP Pin Open**

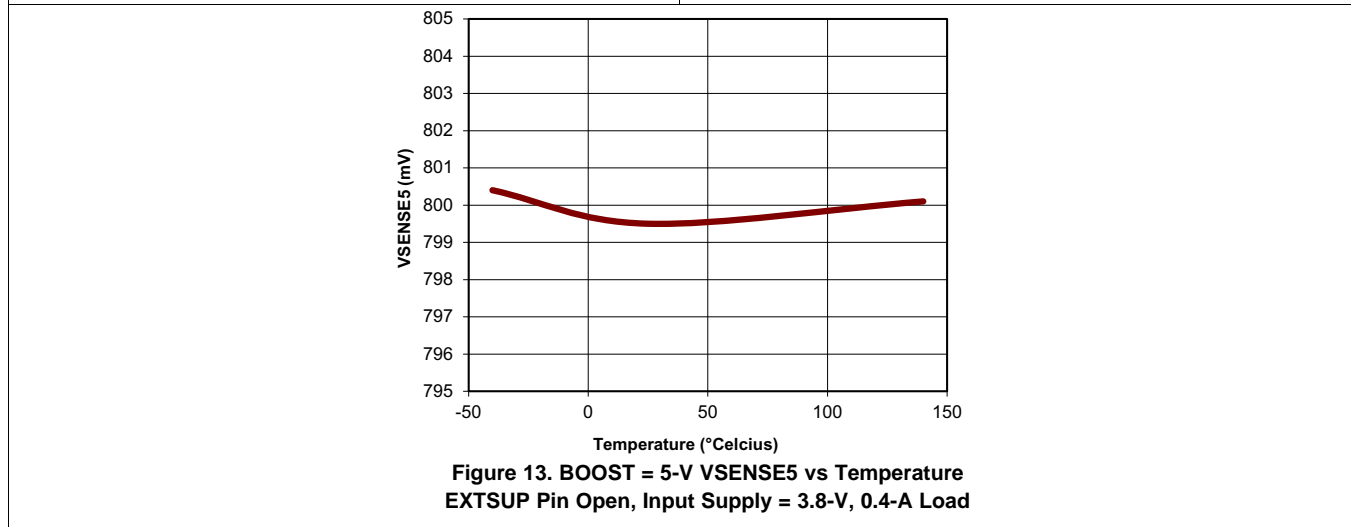
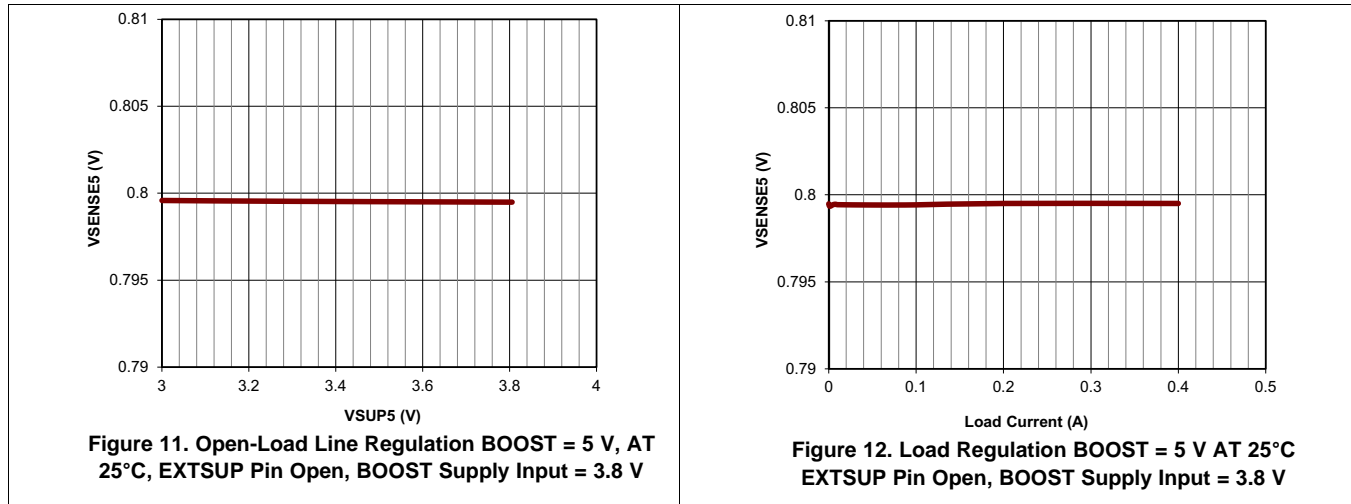


**Figure 9. BUCK2 = 3.3-V VSENSE2 vs Temperature  
EXTSUP Pin Open**



**Figure 10. BUCK3 = 1.2-V VSENSE3 vs Temperature  
EXTSUP Pin Open**

### 7.8.3 BOOST Characteristics



### 7.8.4 LDO Noise Characteristics

(2 × 3.3-μF output capacitance, LDO output = 2.5 V, VSUP4 = 3.8 V)

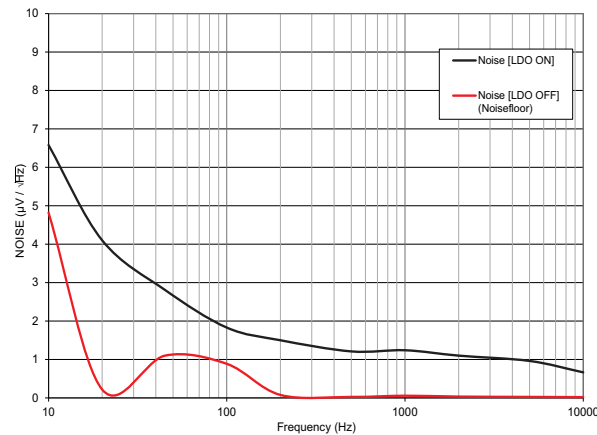


Figure 14. LDO Noise Density

## 8 Detailed Description

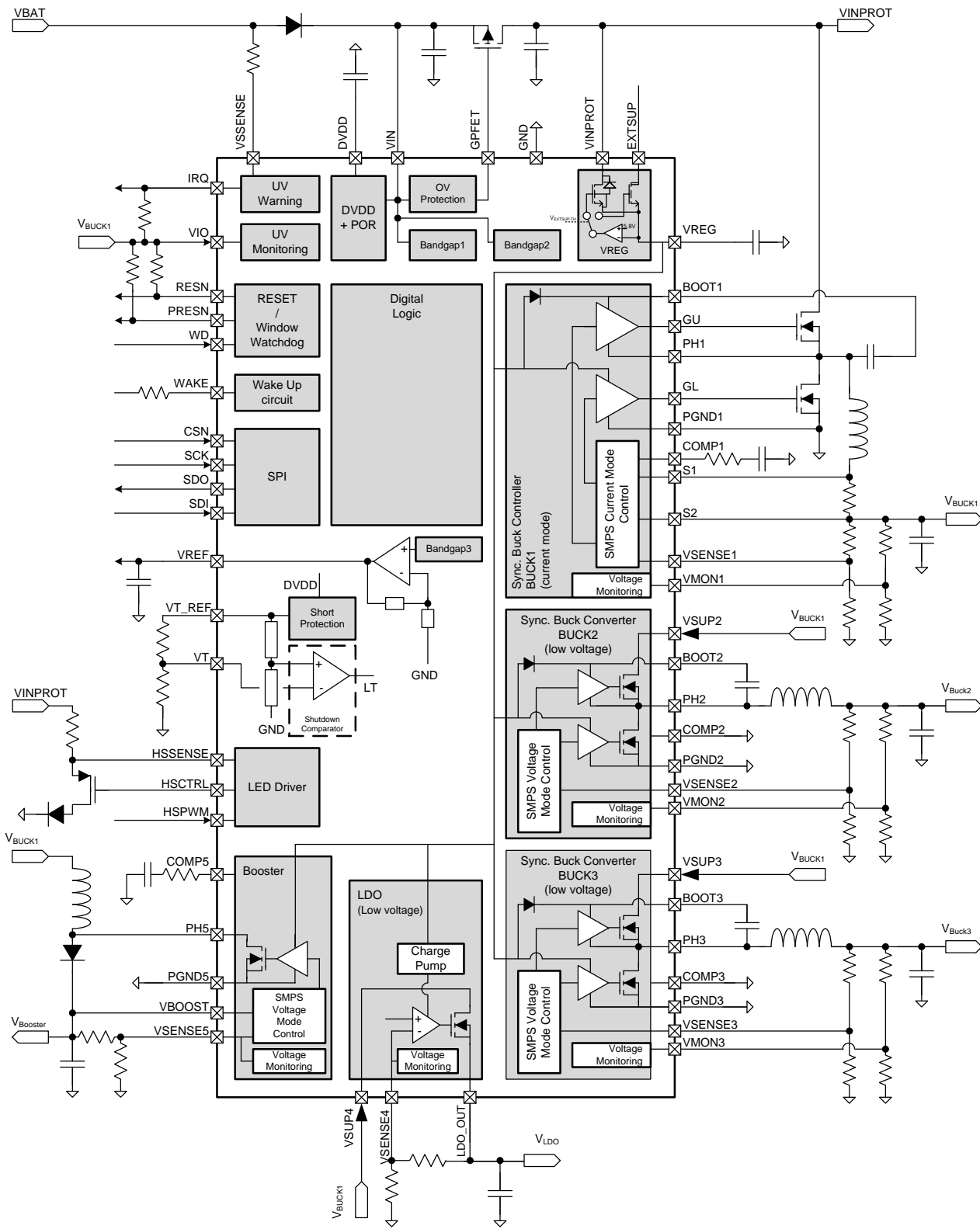
### 8.1 Overview

The device includes one high-voltage buck controller for pre-regulation combined with a two-buck and one-boost converter for post regulation. A further integrated low-dropout (LDO) regulator rounds up the power-supply concept and offers a flexible system design with five independent-voltage rails. The device offers a low power state (LPM0 with all rails off) to reduce current consumption in case the system is constantly connected to the battery line. All outputs are protected against overload and over temperature.

An external PMOS protection feature makes the device capable of sustaining voltage transients up to 80 V. This external PMOS is also used in safety-critical applications to protect the system in case one of the rails shows a malfunction (undervoltage, overvoltage, or overcurrent).

Internal soft-start ensures controlled startup for all supplies. Each power-supply output has an adjustable output voltage based on the external resistor-network settings.

## 8.2 Functional Block Diagram



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Figure 15. Detailed Block Diagram

## 8.3 Feature Description

### 8.3.1 Buck Controller (BUCK1)

The main buck controller operates using constant frequency peak current mode control. The output voltage is programmable with external resistors.

The switching frequency is set to a fixed value of  $f_{\text{SWBUCK1}}$ . Peak current-mode control regulates the peak current through the inductor such that the output voltage  $V_{\text{BUCK1}}$  is maintained to its set value. Current mode control allows superior line-transient response. The error between the feedback voltage  $V_{\text{SENSE1}}$  and the internal reference produces an error signal at the output of the error amplifier (COMP1) which serves as target for the peak inductor current. At S1–S2, the current through the inductor is sensed as a differential voltage and compared with this target during each cycle. A fall or rise in load current produces a rise or fall in voltage at  $V_{\text{SENSE1}}$ , which causes COMP1 to rise or fall respectively, thus increasing or decreasing the current through the inductor until the average current matches the load. In this way the output voltage  $V_{\text{BUCK1}}$  is maintained in regulation.

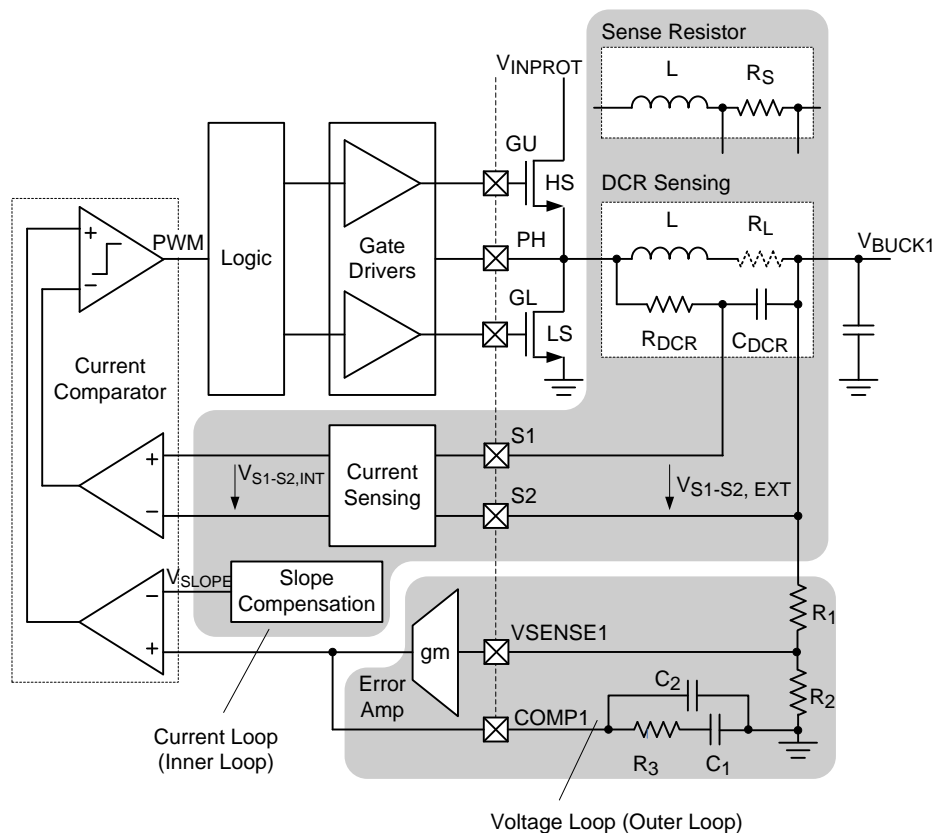


Figure 16. Detailed Block Diagram of Buck 1 Controller

The high-side N-channel MOSFET is turned on at the beginning of each clock cycle and kept on until the inductor current reaches its peak value as set by the voltage loop. Once the high external FET is turned OFF, and after a small delay (shoot-through delay), the lower N-channel MOSFET is turned on until the start of the next clock cycle. In dropout operation the high-side MOSFET stays on 100%. In every fourth period the duty cycle is limited to 95% in order to charge the bootstrap capacitor at BOOT1. This allows a maximum duty cycle of 98.75%.

The maximum value of COMP1 is clamped so that the maximum current through the inductor is limited to a specified value. The BUCK1 controller output voltage is monitored by a central independent voltage-monitoring circuit, which has an independent voltage-monitoring bandgap reference for safety reasons. In addition, BUCK1 is thermally protected with a dedicated temperature sensor.

## Feature Description (continued)

### 8.3.2 Synchronous Buck Converters BUCK2 and BUCK3

Both regulators are synchronous converters operating with a fixed switching frequency  $f_{sw} = 2.45$  MHz. For each buck converter, the output voltage is programmable with external resistors. The synchronous operation mode improves the overall efficiency. BUCK3 switches in phase with BUCK1, and BUCK2 switches at a 216-degree shift to BUCK3 to minimize input current ripple.

Each buck converter can provide a maximum current of 2 A and is protected against short circuits to ground. In case of a short circuit to ground, the integrated cycle-by-cycle current limit turns off the high-side FET when its current reaches  $I_{HS-Limit}$  and the low-side FET is turned on until the end of the given cycle. When the current limit is reached in the beginning of the cycle for five consecutive cycles, the pulse-width modulation (PWM) is forced low for sixteen cycles to prevent uncontrolled current build-up. In case the low-side current limit of  $I_{LS-Limit}$  is reached, for example, because of an output short to the VSUP2 and VSUP23 pins, the low-side FET is turned off until the end of the cycle. If this is detected shortly after the high-low PWM transition (immediately after the low-side overcurrent comparator blanking time), both FETs are turned off for sixteen cycles.

The output voltages of the BUCK2 and BUCK3 regulators are monitored by a central independent voltage-monitoring circuit, which has an independent voltage-monitoring bandgap reference for safety reasons. In addition BUCK2 and BUCK3 are thermally protected with a dedicated temperature sensor.

### 8.3.3 BOOST Converter

The BOOST converter is an asynchronous converter operating with a fixed switching frequency  $f_{sw} = 2.45$  MHz. It switches in phase with BUCK1. At low load, the boost regulator switches to pulse skipping.

The output voltage is programmable with external resistors.

The internal low-side switch can handle maximum 1-A current, and is protected with a current limit. In case of an overcurrent, the integrated cycle-by-cycle current limit turns off the low-side FET when its current reaches  $I_{CLBOOST}$  until the end of the given cycle. When the current limit is reached in the beginning of the cycle for five consecutive cycles, the PWM is forced low for sixteen cycles to prevent uncontrolled current build-up.

The BOOST converter output voltage is monitored by a central independent voltage-monitoring circuit, which has an independent voltage-monitoring bandgap reference for safety reasons. If the  $V_{MONTH\_L} > V_{SENSE5}$  or  $V_{SENSE5} > V_{MONTH\_H}$ , the output is switched off and the BOOST\_FAIL bit in the SPI PWR\_STAT register is set. The BOOST can be reactivated by setting BOOST\_EN bit in the PWR\_CONFIG register.

In addition, the BOOST converter is thermally protected with a dedicated temperature sensor. If  $T_J > T_{OTTH}$ , the BOOST converter is switched off and bit OT\_BOOST in PWR\_STAT register is set. Reactivation of the booster is only possible if the OT\_BOOST bit is 0, and the booster enable bit in the PWR\_CONFIG register is set to 1.

### 8.3.4 Frequency-Hopping Spread Spectrum

The TPS65311-Q1 features a frequency-hopping pseudo-random spectrum or triangular spreading architecture. The pseudo-random implementation uses a linear feedback shift register that changes the frequency of the internal oscillator based on a digital code. The shift register is designed in such a way that the frequency shifts only by one step at each cycle to avoid large jumps in the buck and boost switching frequencies. The triangular function uses an up-down counter. Whenever spread spectrum is enabled (SPI command), the internal oscillator frequency is varied from one BUCK1 cycle to the next within a band of  $0.8 \times f_{OSC} \dots f_{OSC}$  from a total of 16 different frequencies. This means that BUCK3 and BOOST also step through 16 frequencies. The internal oscillator can also change its frequency during the period of BUCK2, yielding a total of 31 frequencies for BUCK2.

### 8.3.5 Linear Regulator LDO

The LDO is a low drop out regulator with an adjustable output voltage through an external resistive divider network. The output has an internal current-limit protection in case of an output overload or short circuit to ground. In addition, the output is protected against overtemperature. If  $T_J > T_{OTTH}$ , the LDO is switched off and bit OT\_LDO in PWR\_STAT register is set. Reactivation of the LDO is only possible through the SPI by setting the LDO enable bit in the PWR\_CONFIG register to 1 if the OT\_LDO bit is 0.



## Feature Description (continued)

The LDO output voltage is monitored by a central independent voltage-monitoring circuit, which has an independent voltage-monitoring bandgap reference for safety reasons. If the  $V_{MONTH\_L} > V_{SENSE4}$  or  $V_{SENSE4} > V_{MONTH\_H}$ , the output is switched off and the LDO\_FAIL bit in the SPI PWR\_STAT register is set. The LDO can be reactivated through the SPI by setting the LDO\_EN bit in the PWR\_CONFIG register. In case of overvoltage in VTCHECK and RAMP mode, the GPFET is turned off and the device changes to ERROR mode.

### 8.3.6 Gate Driver Supply

The gate drivers of the BUCK1 controller, BUCK2 and BUCK3 converters and the BOOST converter are supplied from an internal linear regulator. The internal linear regulator output (5.8-V typical) is available at the VREG pin and must be decoupled using a typical 2.2- $\mu$ F ceramic capacitor. This pin has an internal current-limit protection and must not be used to power any other circuits.

The VREG linear regulator is powered from VINPROT by default when the EXTSUP voltage is less than 4.6 V (typical).

If the VINPROT is expected to go to high levels, there can be excessive power dissipation in this regulator when using large external MOSFETs. In this case, it is advantageous to power this regulator from the EXTSUP pin, which can be connected to a supply less than VINPROT but high enough to provide the gate drive. When EXTSUP is connected to a voltage greater than 4.8 V, the linear regulator automatically switches to EXTSUP as its input to provide this advantage. This automatic switch-over to EXTSUP can only happen once the TPS65311-Q1 device reaches ACTIVE mode. Efficiency improvements are possible when one of the switching regulator rails from the TPS65311-Q1, or any other voltage available in the system is used to power EXTSUP. The maximum voltage that must be applied to EXTSUP is 12 V.

### 8.3.7 RESET

RESN and PRESN are open drain outputs which are active if one or more of the conditions listed in [Table 1](#) are valid. RESN active (low) is extended for  $t_{RESN\text{HOLD}}$  after a reset is triggered. RESN is the main processor reset and also asserts PRESN as a slave signal.

PRESN is latched and is released when window trigger mode of the watchdog is enabled (first rising edge at the WD pin).

RESN and PRESN must keep the main processor and peripheral devices in a defined state during power up and power down in case of improper supply voltages or a critical failure condition. Therefore, for low supply voltages the topology of the reset outputs specify that RESN and PRESN are always held at a low level when RESN and PRESN are asserted, even if  $V_{IN}$  falls below  $V_{POR}$  or the device is in SHUTDOWN mode.

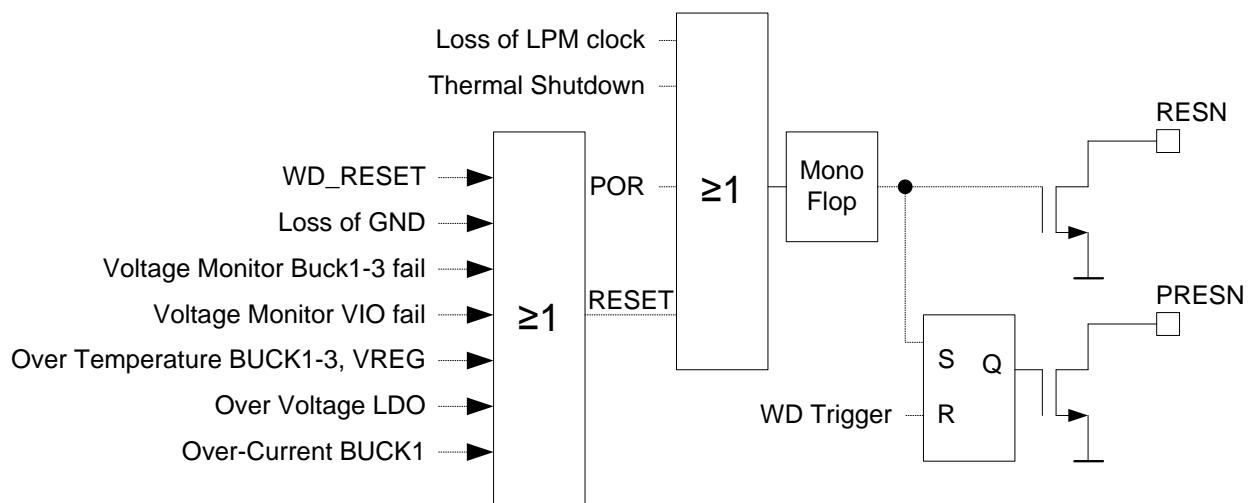


Figure 17. RESET Functionality

**Feature Description (continued)**
**Table 1. Reset Conditions**

RESET CONDITION	CONSEQUENCE FOR DEVICE
POR, Loss of LPM Clock, and Thermal Shutdown	The device reinitializes all registers with their default values. Error counter is cleared.
Voltage Monitor BUCK 1-3	Input voltage at $V_{MON1-3}$ pin out-of-bounds: $V_{VMON1-3} < V_{MONTH\_L}$ or $V_{VMON1-3} > V_{MONTH\_H}$
Over Voltage LDO	$V_{sense4} > V_{MONTH\_H}$
Voltage Monitor VIO	Input voltage at VIO pin out-of-bounds: $V_{VIO} < V_{VIOMON\_TH}$
Loss of GND	Open at PGNDx or GND pin
OT BUCK1, BUCK2, BUCK3, VREG	Overtemperature on BUCK1–3 or VREG
WD_RESET	Watchdog window violation

Any reset event (without POR, thermal shutdown, or loss of LPM clock) increments the error counter (EC) by one. After a reset is consecutively triggered  $N_{RES}$  times, the device transfers to the LPM0 state, and the EC is reset to 0. The counter is decremented by one if an SPI LPM0\_CMD is received. Alternatively, the device can be put in LOCK state once an SPI LOCK\_CMD is received. Once the device is locked, it cannot be activated again by a wake condition. The reset counter and lock function avoid cyclic start-up and shut-down of the device in case of a persistent fault condition. The reset counter content is cleared with a POR condition, a thermal shutdown or a loss of LPM clock. Once the device is locked, a voltage below  $V_{POR}$  at VIN pin or a thermal shutdown condition are the only ways to unlock the device.

**8.3.8 Soft Start**

The output voltage slopes of BUCK, BOOST and LDO regulators are limited during ramp-up (defined by  $t_{STARTX}$ ). During this period the target output voltage slowly settles to its final value, starting from 0 V. In consequence, regulators that offer low-side transistors (BUCK1, BUCK2 and BUCK3) actively discharge their output rails to the momentary ramp-value if previously charged to a higher value.

**8.3.9 Power-on Reset Flag**

The POR flag in the SYS\_STAT SPI register is set:

- When  $V_{IN}$  is below the  $V_{POR}$  threshold
- System is in thermal shutdown
- Over or undervoltage on DVDD
- Loss of low power clock

**8.3.10 WAKE Pin**

Only when the device is in LPM0 mode, it can be activated by a positive voltage on the WAKE pin with a minimum pulse width  $t_{WAKE}$ . A valid wake condition is latched. Normal deactivation of the device can only occur through the SPI Interface by sending an SPI command to enter LMP0. Once in LMP0, the device stays in LPM0 when the WAKE pin is low, or restarts to TESTSTART when the WAKE pin is high.

The WAKE pin has an internal pulldown resistance  $R_{PD-WAKE}$ , and the voltage on the pin is not allowed to exceed 60 V. A higher voltage compliance level in the application can be achieved by applying an external series resistor between the WAKE pin and the external wake-up signal.

The device cannot be re-enabled by toggling the WAKE pin when the device is in LOCKED state (by SPI command).

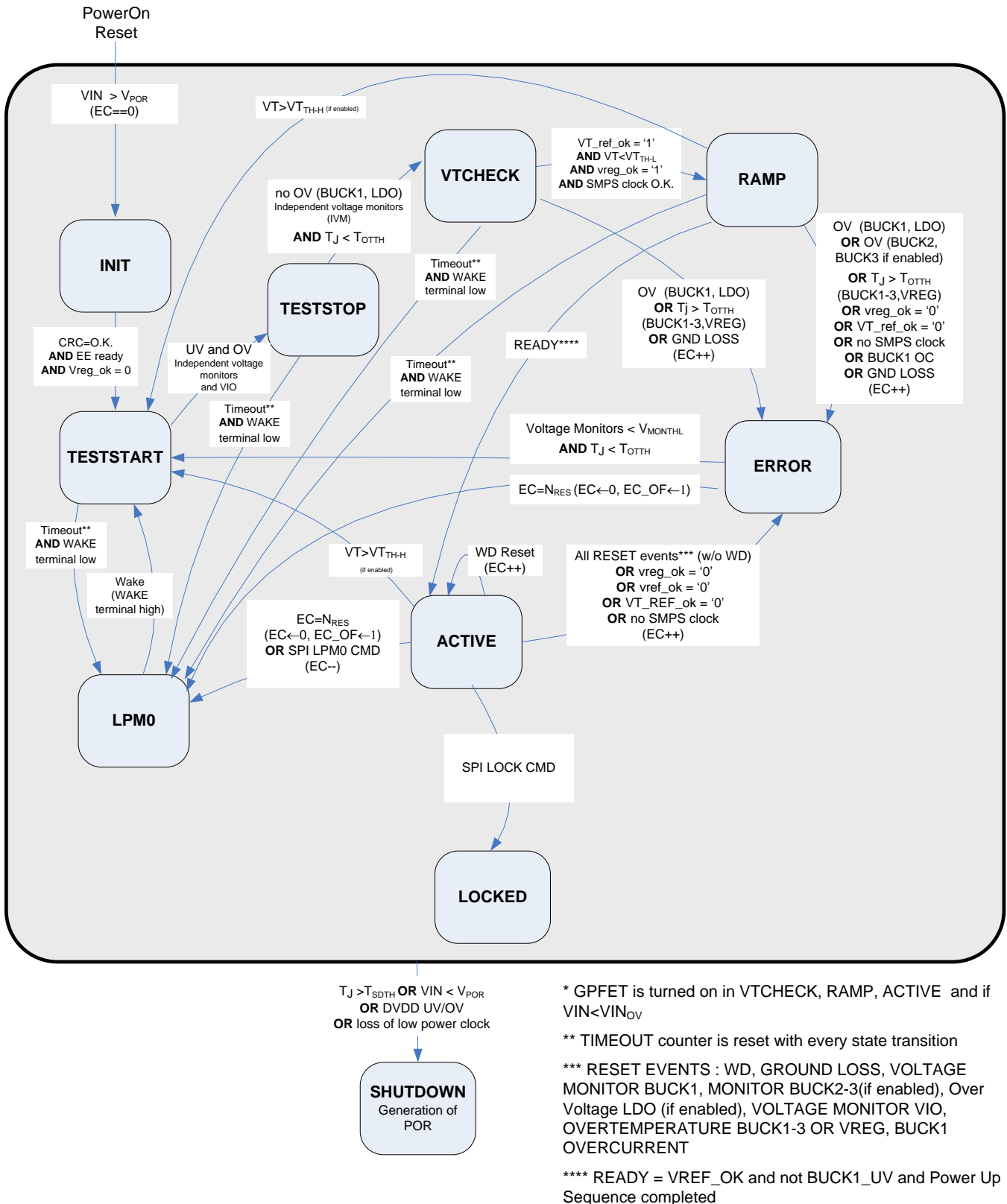


Figure 18. Operating Mode Transitions

### 8.3.11 IRQ Pin

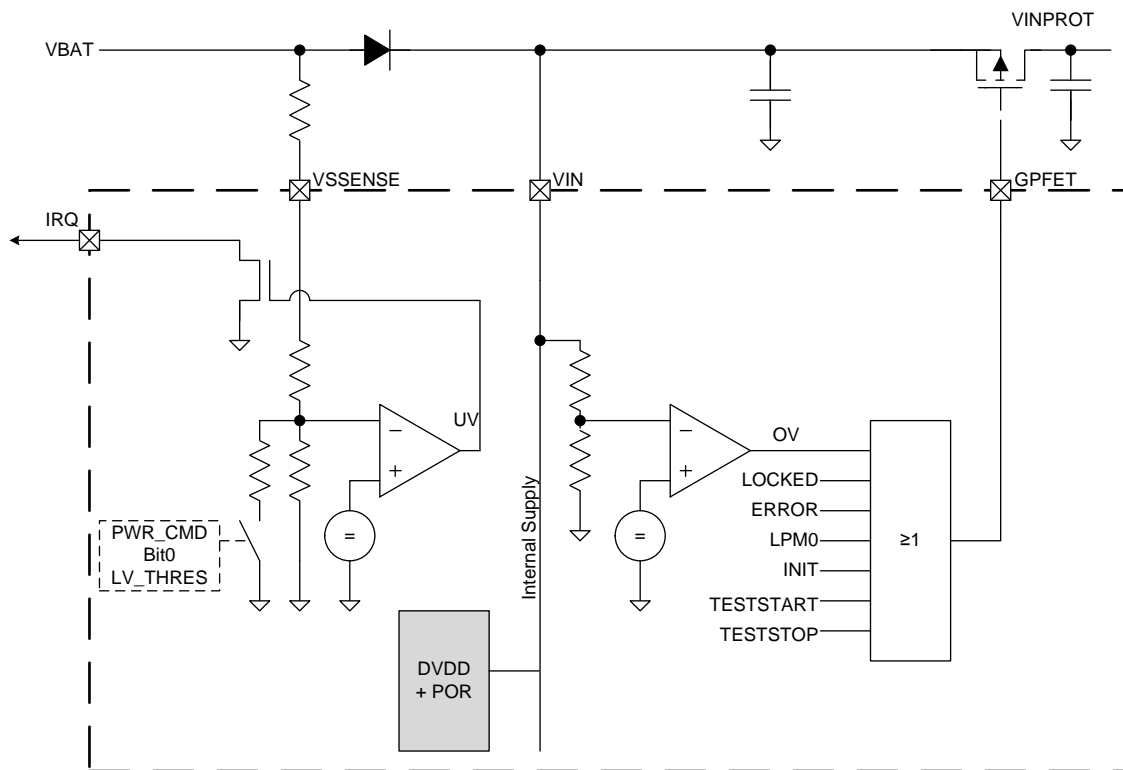
The IRQ pin has two different functions. In OPERATING mode, the pin is forced low when the voltage on the battery line is below the  $V_{SSENSETHX}$  threshold. The IRQ pin is low as long as PRESN is low. If PRESN goes high and the battery line is already below the  $V_{SSENSETHX}$  threshold, the IRQ pin is forced high for  $t_{VSSENSE\_BLK}$ .

### 8.3.12 VBAT Undervoltage Warning

- Low battery condition on VSSENSE asserts IRQ output (interrupt for  $\mu C$ , open drain output)
- Sense input can be directly connected to VBAT through the resistor
- Detection threshold for undervoltage warning can be selected through the SPI.
- An integrated filter time avoids false reaction due to spikes on the VBAT line.

### 8.3.13 VIN Over or Undervoltage Protection

- Undervoltage is monitored on the  $V_{IN}$  line, for POR generation.
- Two  $V_{IN}$  overvoltage shutdown thresholds ( $V_{OVTH}$ ) can be selected through the SPI. After POR, the lower threshold is enabled.
- During LPM0, only the POR condition is monitored.
- An integrated filter time avoids false reaction due to spikes on the  $V_{IN}$  line.
- In case of overvoltage, the external PMOS is switched off to protect the device. The BUCK1 controller is not switched off and it continues to run until the undervoltage on VREG or BUCK1 output is detected.



**Figure 19. Overvoltage or Undervoltage Detection Circuitry**

### 8.3.14 External Protection

The external PMOS switch is disabled if:

- The device detects  $V_{IN}$  overvoltage
- The device is in ERROR, LOCKED, POR, INIT, TESTSTART, TESTSTOP or LPM0 mode

#### NOTE

Depending on the application, the external PMOS may be omitted as long as  $V_{BAT} < 40\text{ V}$

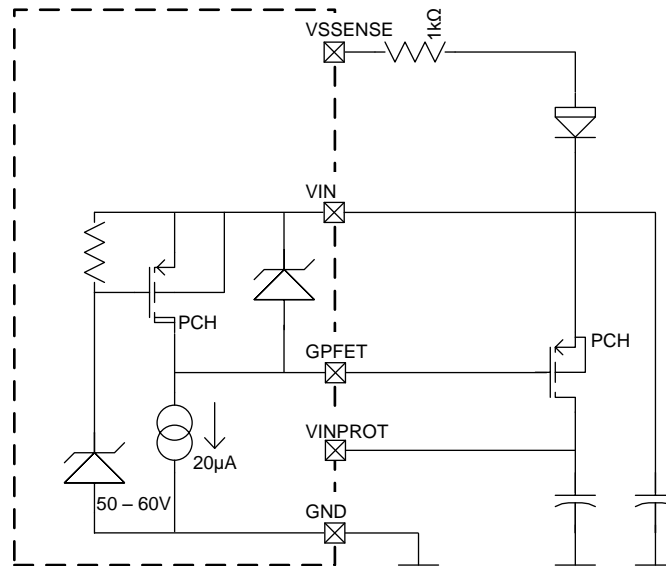


Figure 20. PMOS Control Circuitry

### 8.3.15 Overtemperature Detection and Shutdown

There are two levels of thermal protection for the device.

Overtemperature is monitored locally on each regulator.

**OT for BUCK1, BUCK2, and BUCK3** If a thermal monitor on the buck rails reaches a threshold higher than  $T_{OTTH}$ , the device enters ERROR mode. Leaving ERROR mode is only possible if the temperature is below  $T_{OTTH} - T_{OTHY}$ .

**OT for BOOST and LDO** If the temperature monitor of the boost or the LDO reaches the  $T_{OTTH}$  threshold, the corresponding regulator is switched off.

**Overtemperature Shutdown** is monitored on a central die position. In case the  $T_{SDTH}$  is reached, the device enters shutdown mode. It leaves shutdown when the TSD sensor is below  $T_{SDTH} - T_{SDHY}$ . This event internally generates a POR.

### 8.3.16 Independent Voltage Monitoring

The device contains independent voltage-monitoring circuits for BUCK1–3, LDO, VIO and BOOST. The reference voltage for the voltage monitoring unit is derived from an independent bandgap. BUCKs 1–3 use separate input pins for monitoring. The monitoring circuit is implemented as a window comparator with an upper and lower threshold.

If there is a violation of the upper (only LDO [RAMP, VTCHECK], or BUCK1–3) or lower threshold (only BUCK1–3, or VIO), the device enters ERROR mode, RESN and PRESN are asserted low, the external PMOS (main system switch) is switched off, and the EC is incremented.

In TESTSTART mode, a self-test of the independent voltage monitors is performed.

In case any of the supply rails for BUCK2, BUCK3, LDO or BOOST are not used in the application, the respective VMON2 and VMON3 or VSENSE4 and VSENSE5 pin of the unused supply must be connected to VMON1. Alternatively, the VSENSE4 pin can also be connected directly to ground in case the LDO is not used.

### 8.3.17 GND Loss Detection

All power grounds PGNDx are monitored. If the voltage difference to GND exceeds  $V_{GLTH-low}$  or  $V_{GLTH-high}$ , the device enters ERROR mode. RESN and PRESN are asserted low, the external PMOS (main system switch) is switched off, and the EC is incremented.

### 8.3.18 Reference Voltage

The device includes a precise voltage reference output to supply a system ADC. If this reference voltage is used in the application, a decoupling capacitor between 0.6 and 5  $\mu$ F must be used. If this reference voltage is not used in the application, this decoupling capacitor can be left out. The VREF output is enabled in RAMP state. The output is protected against a short to GND.

### 8.3.19 Shutdown Comparator

An auxiliary, short circuit protected output supplied from DVDD is provided at the VT\_REF pin. This output is used as a reference for an external resistive divider to the VT pin. In case a voltage  $> VT_{TH}$  is detected on the VT pin, the main switch (external PMOS driven by GPFET) is switched off. This functionality can be used to monitor over and under temperature (using a NTC resistor) to avoid operation below or above device specifications.

If the voltage at VT\_REF falls below  $V_{VT\_REF\_SH}$  while the shutdown comparator is enabled, an ERROR transition occurs. The shutdown comparator is enabled in VTCHECK state, and can be turned off by SPI. Disabling the comparator saves power by also disabling the VT\_REF output.

### 8.3.20 LED and High-Side Switch Control

This module controls an external PMOS in current-limited high-side switch.

The current levels can be adjusted with an external sense resistor. Enable and disable is done with the HS\_EN bit. The switch is controlled by the HSPWM input pin. Driving HSPWM high turns on the external FET.

The device offers an open load diagnostic indicated by the HS\_OL flag in the SPI register PWR\_STAT. Open load is also indicated in case the voltage on VINPROT–VSENSE does not drop below the threshold when PWM is low (self-test).

A counter monitors the overcurrent condition to detect the risk of overheating. While HSPWM = high and HS\_EN = high the counter is incremented during overcurrent conditions, and decremented if the current is below the overcurrent threshold at a sampling interval of  $t_{S\_HS}$  (see [Figure 22](#)). When reaching a net current limit time of  $t_{HSS\_CL}$ , the driver is turned off and the HS\_EN bit is cleared. This feature can be disabled by SPI bit HS\_CLDIS. When HS\_EN is cleared, the counter is reset.

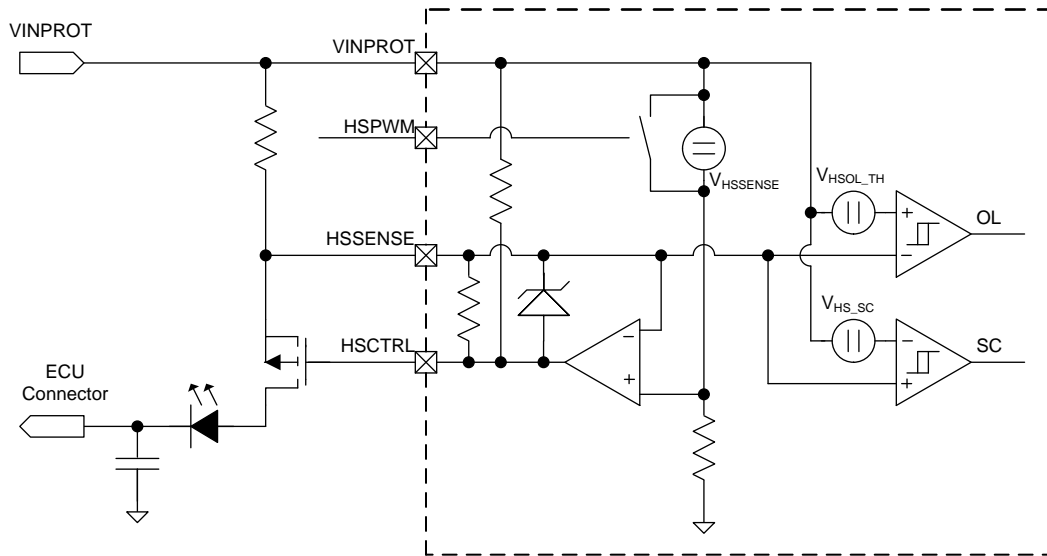


Figure 21. High-Side Control Circuit

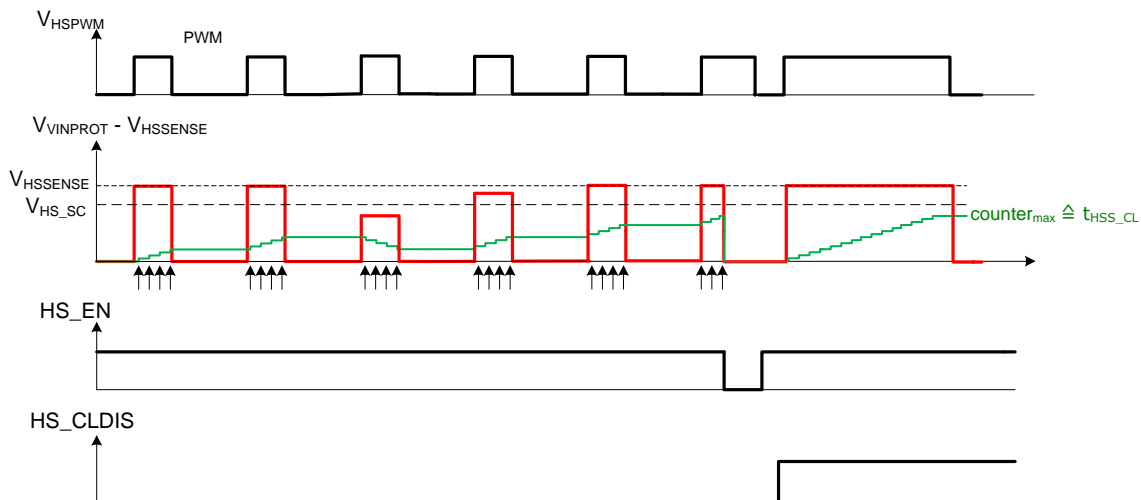


Figure 22. HS Overcurrent Counter

**NOTE**

In case the LED or high-side switch control is not used in the application, HSSense must be connected to VINPROT.

**8.3.21 Window Watchdog**

The WD is used to detect a malfunction of the MCU and DSP. Description:

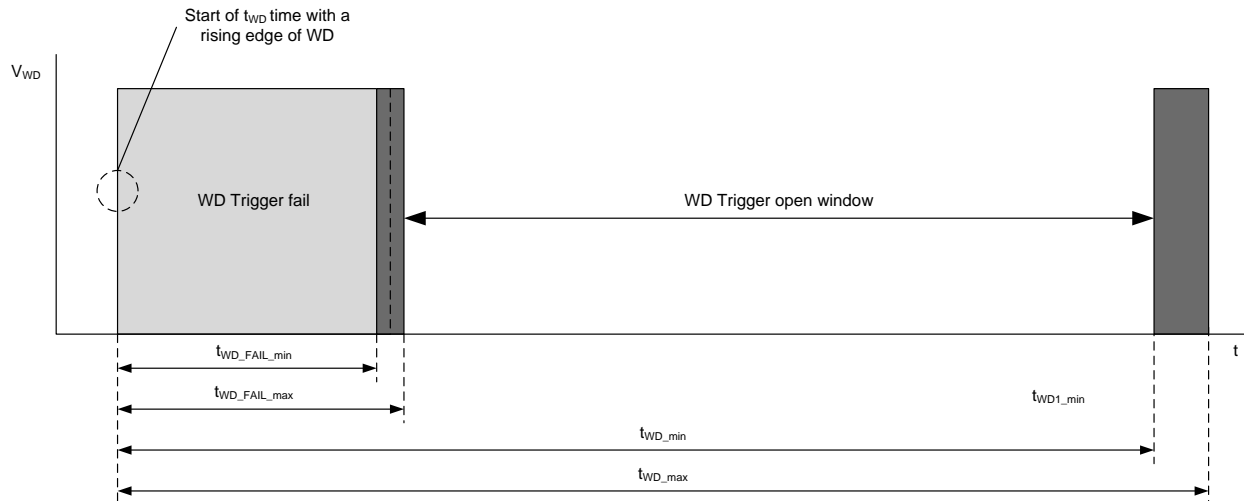
- Timeout trigger mode with long timing starts on the rising edge at RESN
- Window trigger mode with fixed timing after the first and each subsequent rising edge at the WD pin
- Watchdog is triggered by rising edge at the WD pin

A watchdog reset happens by:

- A trigger pulse outside the WD trigger open window
- No trigger pulse during window time



After the RESN pin is released (rising edge) the DSP and MCU must trigger the WD by a rising edge on the WD pin within a fixed time  $t_{\text{timeout}}$ . With this first trigger, the window watchdog functionality is released.



**Figure 23. WD Window Description**

### 8.3.22 Timeout in Start-Up Modes

A timer is used to limit the time during which the device can stay in each of the start-up modes: TESTSTART, TESTSTOP, VTCHECK and RAMP. If the device enters one of these start-up modes and  $V_{IN}$  or  $V_T$  is not in a proper range, the part enters LPM0 after  $t_{\text{timeout}}$  is elapsed and the WAKE pin is low.

## 8.4 Device Functional Modes

### 8.4.1 Operating Modes

#### 8.4.1.1 INIT

Coming from a power-on reset the device enters INIT mode. The configuration data from the EEPROM is loaded in this mode. If the checksum is valid and the internal VREG monitor is indicating an undervoltage condition (self-test VREG comparator), the device enters TESTSTART.

#### 8.4.1.2 TESTSTART

TESTSTART mode is entered:

- After the INIT state (coming from power on)
- After detecting that  $V_T > V_{T_{TH-H}}$
- After ERROR mode and the fail condition is gone
- After a wake command in LPM0

In this mode the OV and UV comparators of BUCK1, BUCK2, BUCK3, BOOST, LDO and VIO are tested. The test is implemented in such a way that during this mode all comparators have to deliver a 1 (fail condition). If this is the case the device enters TESTSTOP mode.

If this is not the case, the device stays in TESTSTART. If the WAKE pin is low, the device enters LPM0 after  $t_{\text{timeout}}$ . If the pin WAKE is high, the part stays in TESTSTART.

#### 8.4.1.3 TESTSTOP

In this mode the OV and UV comparators are switched to normal operation. It is expected that only the UV comparators give a fail signal. In case there is an OV condition on any rail or one of the rails has an overtemperature the device stays in TESTSTOP. If the WAKE pin is low the device enters LPM0 mode after  $t_{\text{timeout}}$ . If the WAKE pin is high, the part stays in TESTSTOP. If there is no overvoltage and overtemperature detected, the part enters VTCHECK mode.

## Device Functional Modes (continued)

### 8.4.1.4 VTCHECK

VTCHECK mode is used to:

1. Switch on external GPFET in case  $V_{IN} < V_{OVTH\_L}$
2. Turn on VREG regulator and VT\_REF
3. Check if voltage on pin VT  $< V_{T_{TH-L}}$
4. Check if SMPS clock is running correctly
5. Check if VREG, VT\_REF exceed the minimum voltage

If all checks are valid the part enters the RAMP state. In case the device is indicating a malfunction and the WAKE pin is low, the device enters LPM0 after  $t_{timeout}$  to reduce current consumption.

In case the voltage monitors detect an overvoltage condition on BUCK1, BUCK2, BUCK3, or LDO, a loss of GND or an overtemperature condition on BUCK1, BUCK2, BUCK3, or VREG the device enters ERROR mode and the error counter is increased.

### 8.4.1.5 RAMP

In this mode the device runs through the power-up sequencing of the SMPS rails (see [Figure 24](#)).

#### 8.4.1.5.1 Power-Up Sequencing

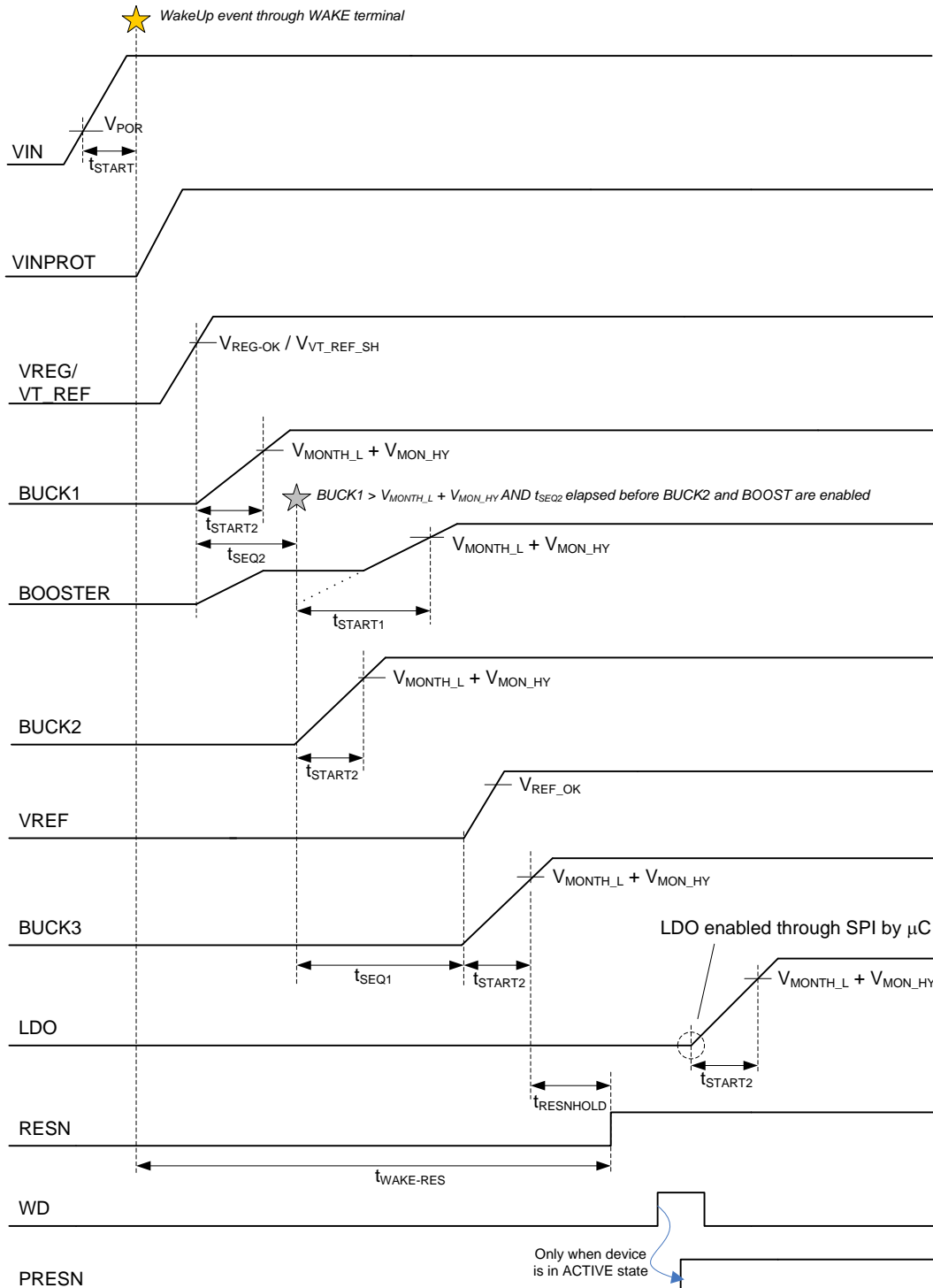
After the power-up sequence (see [Figure 24](#)), all blocks are fully functional. BUCK1 starts first. After  $t_{SEQ2}$  elapses and BUCK1 is above the undervoltage threshold, BUCK2 and BOOST start. BUCK3 and VREF start one  $t_{SEQ1}$  after BUCK2. After the release of RESN pin, the  $\mu C$  can enable the LDO per SPI by setting bit 4 LDO\_EN in PWR\_CONFIG register to 1 (per default, this LDO\_EN is set to 0 after each reset to the  $\mu C$ ).

In case any of the following conditions occur during power-up sequencing, the device enters ERROR mode and the error counter (EC) is increased:

- Overtemperature on BUCK1, BUCK2, BUCK3 or VREG
- Overvoltage on BUCK1, BUCK2, BUCK3 or LDO
- Overcurrent on BUCK1
- SMPS clock fail
- VT\_REF and VREG undervoltage
- Loss of GND

In case  $V_T > V_{T_{TH-H}}$ , the device transitions to TESTSTART.

Device Functional Modes (continued)



★ In case of permanent supply with the device in LPM0 mode, the start point of VREG-VT\_REF is with the rising edge of WAKE. In case of non-permanent supply, the rising edge of the VSSENSE and VIN terminals initiates the start-up sequence

Figure 24. Power-up Sequencing

## Device Functional Modes (continued)

After the power-up sequence is completed (except LDO) without detecting an error condition, the device enters ACTIVE mode.

### 8.4.1.5.2 Power-Down Sequencing

There is no dedicated power-down sequencing. All rails are switched off at the same time. The external FETs of BUCK1 are switched off and the outputs of BUCK2, BUCK3, BOOST (PHx) and the LDO are switched in a high-impedance state.

### 8.4.1.6 ACTIVE

This is the normal operating mode of the device. Transitions to other modes:

#### → ERROR

The device is forced to go to ERROR in case of:

- Any RESET event (without watchdog reset)
- VREG, VREF, or VT\_REF below undervoltage threshold
- SMPS clock fail

During the transition to ERROR mode the EC is incremented.

#### → LOCKED

In case a dedicated SPI command (SPI\_LOCK\_CMD) is issued.

#### → TESTSTART

The device moves to TESTSTART after detecting that  $V_T < V_{T_{TH-L}}$ .

#### → LPM0

The device can be forced to enter LPM0 with a SPI LPM0 command. During this transition the EC is decremented.

If the EC reaches the  $N_{RES}$  value, the device transitions to LPM0 mode and EC is cleared. Depending on the state of the WAKE pin, the device remains in LPM0 (WAKE pin low) or restart to TESTSTART (WAKE pin high). To indicate the device entered LPM0 after EC reached  $N_{RES}$  value, a status bit EC\_OF (error counter overflow, SYS\_STAT bit 3) is set. The EC\_OF bit is cleared on read access to the SYS\_STAT register.

A watchdog reset in ACTIVE mode only increases the EC, but it does not change the device mode.

### 8.4.1.7 ERROR

In this mode all power stages and the GPFET are switched off. The devices leave ERROR mode and enter TESTSTART if:

- All rails indicate an undervoltage condition
- No GND loss is detected
- No overtemperature condition is detected

When the EC reaches the  $N_{RES}$  value, the device transitions to LPM0 and the EC is cleared. To indicate the device entered LPM0 after EC reached  $N_{RES}$ , a status bit EC\_OF (error counter overflow, SYS\_STAT bit 3) is set. The EC\_OF bit is cleared on read access to the SYS\_STAT register.

### 8.4.1.8 LOCKED

Entering this mode disables the device. The only way to leave this mode is through a power-on reset, thermal shutdown, or the loss of an LPM clock.

### 8.4.1.9 LPM0

Low-power mode 0 is used to reduce the quiescent current of the system when no functionality is needed. In this mode the GPFET and all power rails except for DVDD are switched off.

## Device Functional Modes (continued)

In case a voltage  $> V_{WAKE\_ON}$  longer than  $t_{WAKE}$  is detected on the WAKE pin, the part switches to TESTSTART mode.

### 8.4.1.10 SHUTDOWN

The device enters and stays in this mode, as long as  $T_J > T_{SDTH} - T_{SDHY}$  or  $V_{IN} < V_{POR}$  or DVDD under or overvoltage, or loss of low power clock is detected. Leaving this mode and entering INIT mode generates an internal POR.

## 8.5 Programming

### 8.5.1 SPI

The SPI provides a communication channel between the TPS65311-Q1 and a controller. The TPS65311-Q1 is always the slave. The controller is always the master. The SPI master selects the TPS65311-Q1 by setting CSN (chip select) to low. SDI (slave in) is the data input, SDO (slave out) is the data output, and SCK (serial clock input) is the SPI clock provided by the master. If chip select is not active (high), the data output SDO is high impedance. Each communication consist of 16 bits.

1 bit parity (odd) (parity is built over all bits including: R/W, CMD\_ID[5:0], DATA[7:0])

1 bit R/W; read = 0 and write = 1

6 bits CMD identifier

8 bits data

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Parity	R/W	CMD_ID5	CMD_ID4	CMD_ID3	CMD_ID2	CMD_ID1	CMD_ID0	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

**Figure 25. SPI Bit-Frame**

Each command is valid if:

- A valid CMD\_ID is sent
- The parity bit (odd) is correct
- Exactly 16 SPI clocks are counted between falling and rising edge of CSN

The response to each master command is given in the following SPI cycle. The response address is the CMD\_ID of the previous sent message and the corresponding data byte. The response data is latched with the previous cycle such that a response to a write command is the status of the register before the write access. (Same response as a read access.) The response to an invalid command is the original command with the correct parity bit. The response to an invalid number of SPI clock cycles is a SPI\_SCK\_FAIL communication (CMD\_ID = 0x03). Write access to a read-only register is not reported as an SPI error and is treated as a read access. The initial answer after the first SPI command sent is: CMD\_ID[5:0] = 0x3F and Data[7:0] 0x5A.

#### 8.5.1.1 FSI Bit

The slave transmits an FSI bit between the falling edge of CSN and the rising edge of SCK. If the SDO line is high during this time, a failure occurred in the system and the MCU must use the PWR\_STAT to get the root cause. A low level of SDO indicates normal operation of the device.

The FSI bit is set when: PWR\_STAT  $\neq$  0x00, or (SYS\_STAT and 0x98)  $\neq$  0x00, or SPI\_STAT  $\neq$  0x00. The FSI is cleared when all status flags are cleared.

## 8.6 Register Map

CMD_ID	NAME	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0x00	NOP	0x00							
0x03	SPL_SCK_FAIL	1	0	0	SCK_OF	SCK[3]	SCK[2]	SCK[1]	SCK[0]
0x11	LPM0_CMD	0xAA							
0x12	LOCK_CMD	0x55							
0x21	PWR_STAT	BUCK_FAIL	VREG_FAIL	OT_BUCK	OT_LDO	OT_BOOST	LDO_FAIL	BOOST_FAIL	HS_OL
0x22	SYS_STAT	WD	POR	TestMode	SMPCLK_FAIL	EC_OF	EC2	EC1	EC0
0x23	SPI_STAT						CLOCK_FAIL	CMD_ID FAIL	PARITY FAIL
0x24	COMP_STAT					BUCK3-1	BUCK3-0	BUCK2-1	BUCK2-0
0x29	Serial Nr 1	Bit [7:0]							
0x2A	Serial Nr 2	Bit [15:8]							
0x2B	Serial Nr 3	Bit [23:16]							
0x2C	Serial Nr 4	Bit [31:24]							
0x2D	Serial Nr 5	Bit [39:32]							
0x2E	Serial Nr 6	Bit [47:40]							
0x2F	DEV_REV	Major3	Major2	Major1	Major0	Minor3	Minor2	Minor1	Minor0
0x31	PWR_CONFIG		BUCK2_EN	BUCK3_EN	LDO_EN	BOOST_EN	HS_EN	GPFET_OV_HIGH	IRQ_THRES
0x32	DEV_CONFIG					HL_CLDIS	VT_EN	RSV	RSV
0x33	CLOCK_CONFIG	F_EN	SS_EN	SS_MODE	F4	F3	F2	F1	F0

### 8.6.1 Register Description

NOP 0x00									
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
After RESET	0	0	0	0	0	0	0	0	0
Read	0	0	0	0	0	0	0	0	0
Write	d.c.	d.c.	d.c.	d.c.	d.c.	d.c.	d.c.	d.c.	d.c.

SPI_SCK_FAIL 0x03									
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
Default after RESET	1	0	0	0	0	0	0	0	0
Read	1	0	0	SCK_OF	SCK[3]	SCK[2]	SCK[1]	SCK[0]	
Write	d.c.	d.c.	d.c.	d.c.	d.c.	d.c.	d.c.	d.c.	d.c.

BIT NAME	BIT NO.	DESCRIPTION
SCK_OF	4	Between a falling and a rising edge of CSN, the number of SCK was greater than 16. 0: 1: Number of SCK cycles was > 16
Comment: This flag is cleared after its content is transmitted to the master.		

BIT NAME	BIT NO.	DESCRIPTION
SCK[3:0]	3:0	The number of rising edges on SCK between a falling and a rising edge of CSN minus 1. Saturates at 0xF if 16 or more edges are received.
Comment: This flag is cleared after its content is transmitted to the master.		

LPM0_CMD 0x11									
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
After RESET	0	0	0	0	0	0	0	0	0
Read	0	0	0	0	0	0	0	0	0
Write	0xAA								
This command is used to send the device into LPM0 mode.									

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LOCK_CMD 0x12								
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
After RESET	0	0	0	0	0	0	0	0
Read	0	0	0	0	0	0	0	0
Write	0x55							

Sending a lock command (0x55) brings the device into LOCK mode. Only a POR brings the device out of this state.

PWR_STAT 0x21								
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Default after POR	0	0	0	0	0	0	0	0
Read	BUCK_FAIL	VREG_FAIL	OT_BUCK	OT_LDO	OT_BOOST	LDO_FAIL	BOOST_FAIL	HS_OL
Write	d.c.	d.c.	d.c.	d.c.	d.c.	d.c.	d.c.	d.c.

BIT NAME	BIT NO.	DESCRIPTION
BUCK_FAIL	7	BUCK power fail flag 0: 1: Power stages shutdown detected caused by OC BUCK1, UV, OV, loss of GND (BOOST + all bucks)

BUCK\_FAIL flag is cleared in case the fail condition is not present anymore and the flag is transmitted to the master.

BIT NAME	BIT NO.	DESCRIPTION
VREG_FAIL	6	Internal voltage regulator too low 0: 1: VREG fail

VREG\_FAIL flag is cleared in case the fail condition is not present anymore and the flag is transmitted to the master.

BIT NAME	BIT NO.	DESCRIPTION
OT_BUCK	5	BUCK1-3 overtemperature flag 0: 1: IC power stages shutdown due to overtemperature

OT flag is cleared in case the fail condition is not present anymore and the flag is transmitted to the master.

BIT NAME	BIT NO.	DESCRIPTION
OT_LDO	4	LDO overtemperature flag 0: 1: LDO shutdown due to overtemperature

OT flag is cleared in case the fail condition is not present anymore and the flag is transmitted to the master.

BIT NAME	BIT NO.	DESCRIPTION
OT_BOOST	3	Boost overtemperature flag 0: 1: BOOST shutdown due to overtemperature

OT flag is cleared in case the fail condition is not present anymore and the flag is transmitted to the master.

BIT NAME	BIT NO.	DESCRIPTION
LDO_FAIL	2	LDO under or overvoltage flag 0: 1: LDO out of regulation

LDO\_FAIL flag is cleared if there is no undervoltage and no overvoltage and the flag is transmitted to the master.

BIT NAME	BIT NO.	DESCRIPTION
BOOST_FAIL	1	Booster under or overvoltage flag or loss of GND 0: 1: Booster out of regulation
BOOST_FAIL flag is cleared if there is no undervoltage and no overvoltage and the flag was transmitted to the master.		

BIT NAME	BIT NO.	DESCRIPTION
HS_OL	0	High-side switch open load condition 0: 1: Open load at high side
Bit indicates current OL condition of high side (no flag)		

SYS_STAT 0x22								
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Default after POR	0	0	0	0	0	0	0	1
Read	WD	POR	Testmode	SMPCLK_FAIL	0	EC2	EC1	EC0
Write	d.c.	d.c.	d.c.	d.c.	d.c.	d.c.	d.c.	d.c.

BIT NAME	BIT NO.	DESCRIPTION
WD	7	Watchdog reset flag 0: 1: Last reset caused by watchdog
Comment: This flag is cleared after its content is transmitted to the master.		

BIT NAME	BIT NO.	DESCRIPTION
POR	6	Power-on reset flag 0: 1: Last reset caused by a POR condition
Comment: This flag is cleared after its content is transmitted to the master.		

BIT NAME	BIT NO.	DESCRIPTION
Testmode	5	If this bit is set, the device entered test mode 0: 1: Device in Testmode
Comment: This flag is cleared after its content is transmitted to the master and the device left the test mode.		

BIT NAME	BIT NO.	DESCRIPTION
SMPCLK_FAIL	4	If this bit is set, the clock of the switch mode power supplies is too low. 0: Clock OK 1: Clock fail
Comment: This flag is cleared after its content is transmitted to the master.		

BIT NAME	BIT NO.	DESCRIPTION
EC [2:0]	0-2	Actual error flag counter 0: - 1: -
*Error Counter is only deleted with a POR		



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SPI_STAT 0x23								
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Default after RESET	0	0	0	0	0	0	0	0
Read	0	0	0	0	0	CLOCK_FAIL	CMD_ID FAIL	PARITY FAIL
Write	d.c.	d.c.	d.c.	d.c.	d.c.	d.c.	d.c.	d.c.

BIT NAME	BIT NO.	DESCRIPTION
CLOCK_FAIL	2	Between a falling and a rising edge of CSN, the number of SCK does not equal 16 0: 1: Wrong SCK

Comment: This flag is cleared after its content is transmitted to the master.

BIT NAME	BIT NO.	DESCRIPTION
CMD_ID FAIL	1	Last received CMD_ID in a reserved area 0: 1: Wrong CMD_ID

Comment: This flag is cleared after its content is transmitted to the master and is not set if the number of SCK cycles is incorrect.

BIT NAME	BIT NO.	DESCRIPTION
PARITY_FAIL	0	Last received command has a parity bit failure 0: 1: Parity bit error

Comment: This flag is cleared after its content is transmitted to the master and is not set if the number of SCK cycles is incorrect.

COMP_STAT 0x24								
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Default after RESET	0	0	0	0	0	1	1	0
Read	0	0	0	0	BUCK3-1	BUCK3-0	BUCK2-1	BUCK2-0
Write	d.c.	d.c.	d.c.	d.c.	d.c.	d.c.	d.c.	d.c.

Register to read back the actual BUCK2/3 compensation settings on COMP2/3. 0x1 ≥ 0 V 0 x 2 ≥ VREG 0 x 3 ≥ open

DEV_REV 0x2F								
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
After RESET	Major3	Major2	Major1	Major0	Minor3	Minor2	Minor1	Minor0
Read	Major3	Major2	Major1	Major0	Minor3	Minor2	Minor1	Minor0
Write	d.c.	d.c.	d.c.	d.c.	d.c.	d.c.	d.c.	d.c.

Hard coded device revision can be read from this register

PWR_CONFIG 0x31								
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Default after RESET	0	1	1	0	1	0	0	0
Read	0	BUCK2_EN	BUCK3_EN	LDO_EN	BOOST_EN	HS_EN	GP_FET_OV_HIGH	IRQ_THRES
Write	0	BUCK2_EN	BUCK3_EN	LDO_EN	BOOST_EN	HS_EN	GP_FET_OV_HIGH	IRQ_THRES

This register contains all power rail enable bits.

BIT NAME	BIT NO.	DESCRIPTION
BUCK2_EN	6	BUCK2 enable flag 0: 1: Enable BUCK2
After reset, BUCK2 is enabled		

BIT NAME	BIT NO.	DESCRIPTION
BUCK3_EN	5	BUCK3 enable flag 0: 1: Enable BUCK3
After reset, BUCK3 is enabled		

BIT NAME	BIT NO.	DESCRIPTION
LDO_EN	4	LDO enable flag 0: 1: LDO enabled
After reset, LDO is disabled		

BIT NAME	BIT NO.	DESCRIPTION
BOOST_EN	3	BOOST enable 0: 1: BOOST enabled
After reset, BOOST is enabled		

BIT NAME	BIT NO.	DESCRIPTION
HS_EN	2	LED and high-side switch enable 0: High side disabled 1: High side enabled
After reset, high side is disabled		

BIT NAME	BIT NO.	DESCRIPTION
GPFET_OV_HIGH	1	Protection FET overvoltage shutdown 0: Protection FET switches off at $V_{IN} > V_{OVTH-L}$ 1: Protection FET switches off at $V_{IN} > V_{OVTH-H}$
After reset, the lower VIN protection threshold is enabled		

BIT NAME	BIT NO.	DESCRIPTION
IRQ_THRES	0	VSSENSE IRQ low voltage interrupt threshold select 0: Low threshold selected ( $V_{SSENSETH-L}$ ) 1: High threshold selected ( $V_{SSENSETH-H}$ )
After reset, the lower VBAT monitoring threshold is enabled		

DEV_CONFIG 0x32								
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Default after RESET	0	0	0	0	0	1	1	0
Read	0	0	0	0	0	VT_EN	RSV	RSV
Write	d.c.	d.c.	d.c.	d.c.	d.c.	VT_EN	1	0

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BIT NAME	BIT NO.	DESCRIPTION
HS_CLDIS	3	LED and high-side switch current limit counter disable bit 0: LED and high-side switch current limit counter enabled 1: LED and high-side switch current limit counter disabled

BIT NAME	BIT NO.	DESCRIPTION
VT_EN	2	VT enable bit 0: VT monitor disabled 1: VT monitor enabled

The VT monitor cannot be turned on after it was turned off. Turn on only happens during power up in the VTCHECK state.

BIT NAME	BIT NO.	DESCRIPTION
RSV	1	Voltage reference enable bit 0: not recommended setting 1: default setting

BIT NAME	BIT NO.	DESCRIPTION
RSV	0	Reserved - keep this bit at 1 0: default setting 1: not recommended setting

CLOCK_CONFIG 0x33								
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Default after RESET	0	0	0	1	0	0	0	0
Read	F_EN	SS_EN	SS_MODE	F4	F3	F2	F1	F0
Write	F_EN	SS_EN	SS_MODE	F4	F3	F2	F1	F0

BIT NAME	BIT NO.	DESCRIPTION
F_EN	7	Frequency tuning enable register 0: Off – Setting of Bit4...Bit0 are not effective, setting of Bit6 and Bit5 become effective 1: On – Setting of Bit4...Bit0 become effective, setting of Bit6 and Bit5 are not effective

BIT NAME	BIT NO.	DESCRIPTION
SS_EN	6	Spread spectrum mode enable 0: Spread spectrum option for all switching regulators disabled 1: Spread spectrum option for all switching regulators enabled (only when F_EN = 0)

When enabled, the switching frequency of BUCK1/2/3 and BOOST is modulated between  $0.8 \times f_{osc}$  and  $f_{osc}$ .

BIT NAME	BIT NO.	DESCRIPTION
SS_MODE	5	Spread spectrum mode select (effective only when F_EN = 0) 0: Pseudo random 1: Triangular

BIT NAME	BIT NO.	DESCRIPTION
F4, F3, F2, F1, F0	4-0	Frequency tuning register (effective only when F_EN = 1)

0x10 is default value, trim range is 25% for 0x00 setting to –20% for 0x1F setting. Frequency tuning influences the switching frequency of BUCK1/2/3 and BOOST as well as the watchdog timing.

## 9 Application and Implementation

### NOTE

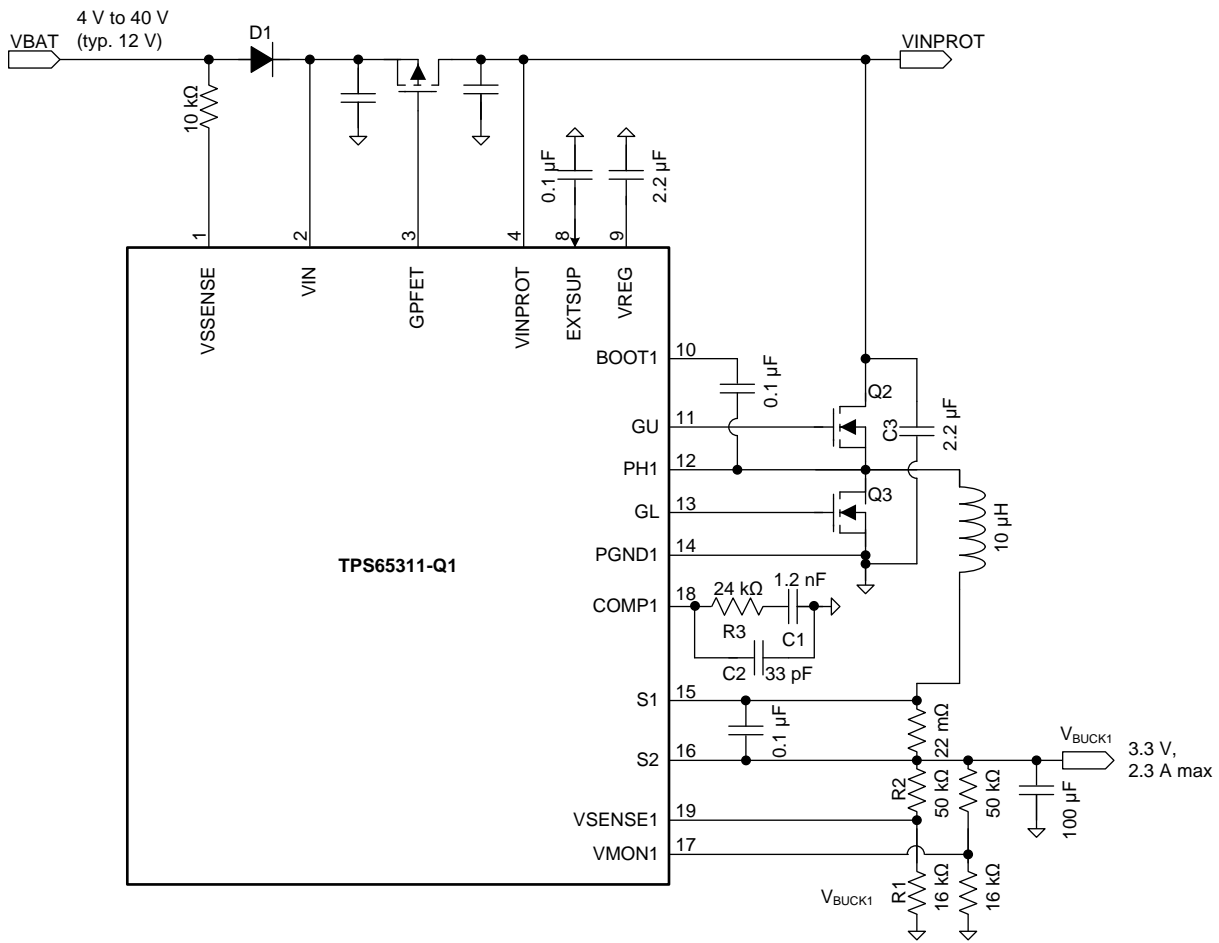
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The TPS65311-Q1 device is a multi-rail power supply including one buck controller, two buck converters, one boost converter and one linear regulator (LDO). The buck controller is typically used to convert a higher car battery voltage to a lower DC voltage which is then used as pre-regulated input supply for the buck converters, boost converter, and the linear regulator. Use the following design procedure and application example to select component values for the TPS65311-Q1 device.

### 9.2 Typical Applications

#### 9.2.1 Buck Controller (BUCK1)



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Figure 26. Buck Controller Schematic

## Typical Applications (continued)

### 9.2.1.1 Design Requirements

For this design example, use the parameters listed in [Table 2](#).

**Table 2. Design Parameters**

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	12 V
Output voltage ( $V_{\text{BUCK1}}$ )	3.3 V
Maximum output current ( $I_{\text{max\_peak\_coil}}$ )	2.3 A
Load Step $\Delta I_{\text{OUT}}$	1 A
Output current ripple $I_{\text{L\_ripple}}$	500 mA
Output voltage ripple	3 mV
Allowed voltage step on output $\Delta V_{\text{OUT}}$	0.198 (or 6%)
Switching frequency ( $f_{\text{SWBUCK1}}$ )	490 kHz
Bandwidth ( $F_{\text{BW}}$ )	≈ 60 kHz

### 9.2.1.2 Detailed Design Procedure

#### 9.2.1.2.1 Adjusting the Output Voltage for the BUCK1 Controller

A resistor divider from the output node to the VSENSE1 pin sets the output voltage. TI recommends using 1% tolerance or better divider resistors. Start with 16 k $\Omega$  for the R1 resistor and use [Equation 1](#) to calculate R2 (see [Figure 26](#)).

$$R_2 = \frac{R_1 \times (V_{\text{BUCK1}} - 0.8 \text{ V})}{0.8 \text{ V}} \quad (1)$$

Therefore, for the value of  $V_{\text{BUCK1}}$  to equal to 3.3 V, the value of R2 must be 50 k $\Omega$ .

For voltage monitoring of the BUCK1 output voltage, placing an additional resistive divider with the exact same values from the output node to the VMON1 pin is recommended for safety reasons (see [Figure 26](#)). If no safety standard must be fulfilled in the application, the VMON1 pin can be directly connected to VSENSE1 pin without the need for this additional resistive divider.

#### 9.2.1.2.2 Output Inductor, Sense Resistor, and Capacitor Selection for the BUCK1 Controller

An external resistor senses the current through the inductor. The current sense resistor pins (S1 and S2) are fed into an internal differential amplifier which supports the range of  $V_{\text{BUCK1}}$  voltages. The sense resistor  $R_S$  must be chosen so that the maximum forward peak current in the inductor generates a voltage of 75 mV across the sense pins. This specified typical value is for low duty cycles only. At typical duty-cycle conditions around 28% (assuming 3.3-V output and 12-V input), 50 mV is a more reasonable value, considering tolerances and mismatches. The typical characteristics (see [Figure 2](#)) provide a guide for using the correct current-limit sense voltage.

$$R_S = \frac{60 \text{ mV}}{I_{\text{max\_peak}}} \quad (2)$$

Optimal slope compensation which is adaptive to changes in input voltage and duty cycle allows stable operation at all conditions. In order to specify optimal performance of this circuit, the following condition must be satisfied in the choice of inductor and sense resistor:

$$L = 410 \times R_S$$

where

- L = inductor in  $\mu\text{H}$
  - $R_S$  = sense resistor in  $\Omega$
- (3)

The current sense pins S1 and S2 are high impedance pins with low leakage across the entire  $V_{\text{BUCK1}}$  range. This allows DCR current sensing (see [Figure 16](#)) using the DC resistance of the inductor for better efficiency.

For selecting the output capacitance and its ESR resistance, the following set of equations can be used:

$$C_{OUT} > \frac{2 \times \Delta I_{OUT}}{f_{SW} \times \Delta V_{OUT}}$$

$$C_{OUT} > \frac{1}{8 \times f_{SW}} \times \frac{I_{L\_ripple}}{V_{o\_ripple}}$$

$$R_{ESR} < \frac{V_{o\_ripple}}{I_{L\_ripple}}$$

where

- $f_{sw}$  is the 490-kHz switching frequency
- $\Delta I_{OUT}$  is the worst-case load step from the application
- $\Delta V_{OUT}$  is the allowed voltage step on the output
- $V_{o\_ripple}$  is the allowed output voltage ripple
- $I_{L\_ripple}$  is the ripple current in the coil

(4)

### 9.2.1.2.3 Compensation of the Buck Controller

The main buck controller requires external type 2 compensation on pin COMP1 for normal mode operation. The components can be calculated as follows.

1. Select a value for the bandwidth,  $F_{BW}$ , to be between  $f_{SWBUCK1} / 6$  (faster response) and  $f_{SWBUCK1} / 10$  (more conservative)
2. Use Equation 5 to select a value for R3 (see Figure 16).

$$R3 = \frac{2\pi \times F_{BW} \times V_{OUT1} \times C_{OUT1}}{gm \times K_{CFB} \times V_{refBUCK}}$$

where

- $C_{OUT1}$  is the load capacitance of BUCK1
- $gm$  is the error amplifier transconductance
- $K_{CFB} = 0.125 / R_s$
- $V_{refBUCK}$  is the internal reference voltage

(5)

3. Use Equation 6 to select a value for C1 (in series with R3, see Figure 16) to set the zero frequency close to  $F_{BW} / 10$ .

$$C1 = \frac{10}{2\pi \times R3 \times F_{BW}}$$

(6)

4. Use Equation 7 to select a value for C2 (parallel with R3, C1, see Figure 16) to set the second pole below  $f_{SWBUCK1} / 2$

$$C2 = \frac{1}{2\pi \times R3 \times F_{BW} \times 3}$$

(7)

For example:

$$f_{SWBUCK1} = 490 \text{ kHz}, V_{refBUCK} = 0.8 \text{ V}, F_{BW} = 60 \text{ kHz}$$

$$V_{OUT1} = 3.3 \text{ V}, C_{OUT1} = 100 \text{ }\mu\text{F}, R_s = 22 \text{ m}\Omega$$

$$\text{Selected values: } R3 = 24 \text{ k}\Omega, C1 = 1.2 \text{ nF}, C2 = 33 \text{ pF}$$

$$\text{Resulting in } F_{BW}: 58 \text{ kHz}$$

$$\text{Resulting in zero frequency: } 5.5 \text{ kHz}$$

$$\text{Resulting in second pole frequency: } 201 \text{ kHz}$$

Stability and load step response must be verified in measurements to fine tune the values of the compensation components.

9.2.1.2.4 Bootstrap Capacitor for the BUCK1 Controller

The BUCK1 controller requires a bootstrap capacitor. This bootstrap capacitor must be 0.1 μF. The bootstrap capacitor is located between the PH1 pin and the BOOT1 pin (see Figure 26). The bootstrap capacitor must be a high-quality ceramic type with X7R or X5R grade dielectric for temperature stability.

9.2.1.3 BUCK 1 Application Curve

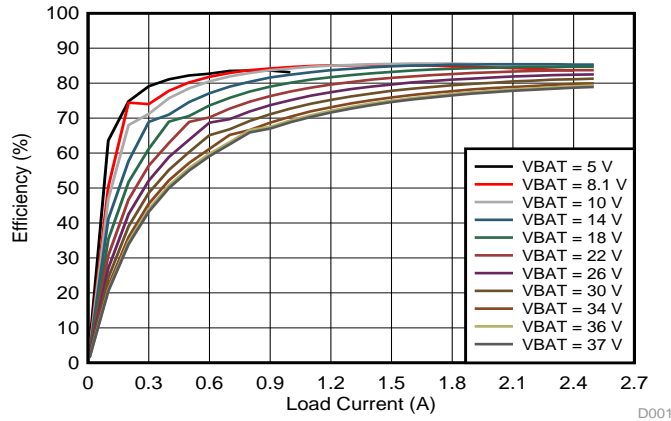
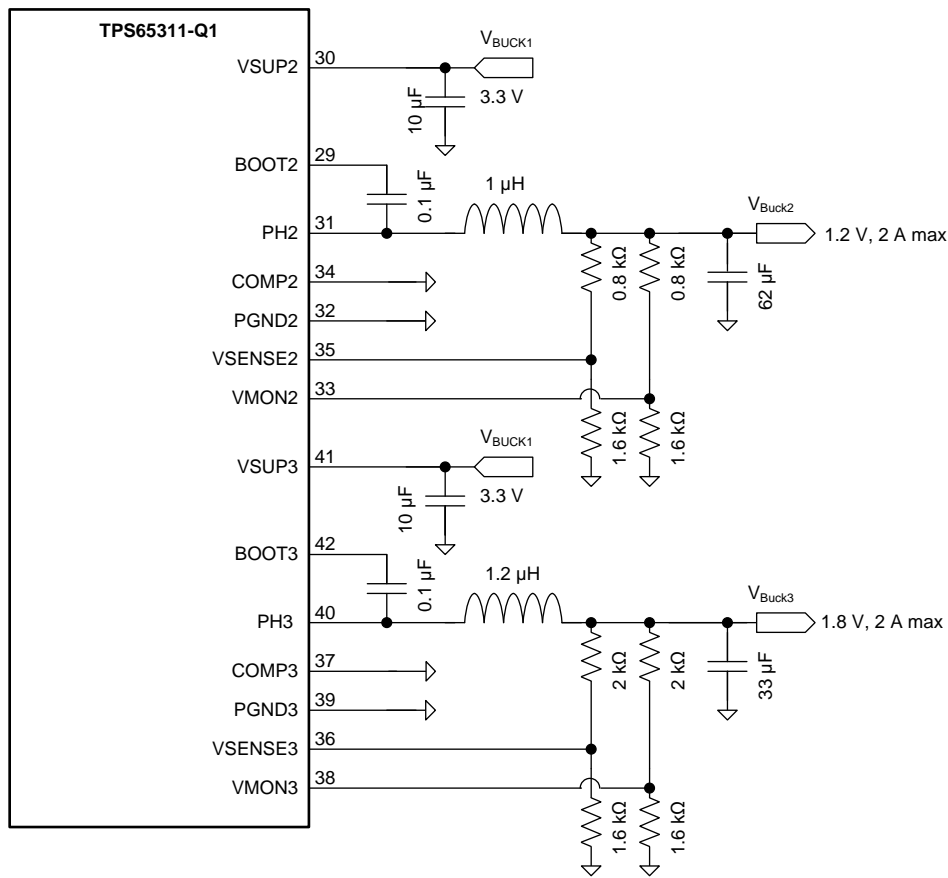


Figure 27. Efficiency Results of Buck1

9.2.2 Synchronous Buck Converters BUCK2 and BUCK3



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Figure 28. Synchronous Buck Converter Schematic

### 9.2.2.1 Design Requirements

For this design example, use the parameters listed in [Table 3](#).

**Table 3. Design Parameters**

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	3.3 V
Output voltage ( $V_{\text{BUCK2/3}}$ )	1.2 V 1.8 V
Maximum output current ( $I_{\text{max\_peak}}$ )	2 A
Output current ripple $\Delta I_{\text{L\_PP}}$	300 mA
Switching frequency ( $f_{\text{SWBUCK2/3}}$ )	2.45 MHz

### 9.2.2.2 Detailed Design Procedure

#### 9.2.2.2.1 Adjusting the Output Voltage for the BUCK2 and BUCK3 Converter

A resistor divider from the output node to the VSENSE2 to ground respectively between the VSENSE3 to ground pin sets the output voltage (see [Figure 28](#)). TI recommends using 1% tolerance or better divider resistors. Start by selecting 1.6 k $\Omega$  for the value of the  $R_x$  resistor between the VSENSE2 to ground respectively between the VSENSE3 to ground pin VSENSE3 pin and use [Equation 8](#) to calculate the value for the  $R_y$  resistor between BUCK2 and BUCK3 output and the VSENSE2 to ground respectively between the VSENSE3 to ground pin.

$$R_y = \frac{R_x \times (V_{\text{BUCK2/3}} - 0.8 \text{ V})}{0.8 \text{ V}} \quad (8)$$

Therefore, for  $V_{\text{BUCK2}}$  to equal to 1.2 V, the value of  $R_y$  must be 0.8 k $\Omega$ . For  $V_{\text{BUCK3}}$  to equal to 1.8 V, the value of  $R_y$  must be 2 k $\Omega$ .

For voltage monitoring of the BUCK2 and BUCK3 output voltage, placing an additional resistive divider with exact same values from the output node to the VMON2 and VMON3 pins is recommended for safety reasons (see [Figure 28](#)). If no safety standard must be fulfilled in the application, the VMON2 and VMON3 pins can be directly connected to VSENSE2 and VSENSE3 pins without the need for this additional resistive divider.

#### 9.2.2.2.2 Output Inductor Selection for the BUCK2 and BUCK3 Converter

The inductor value  $L$  depends on the allowed ripple current  $\Delta I_{\text{L\_PP}}$  in the coil at chosen input voltage  $V_{\text{IN}}$  and output voltage  $V_{\text{OUT}}$ , and given switching frequency  $f_{\text{sw}}$ :

$$L = \frac{V_{\text{OUT}} \times (V_{\text{IN}} - V_{\text{OUT}})}{\Delta I_{\text{L\_PP}} \times V_{\text{IN}} \times f_{\text{sw}}} \quad (9)$$

For example:

$$\begin{aligned} V_{\text{IN}} &= 3.3 \text{ V (from BUCK1)} \\ V_{\text{OUT}} &= 1.2 \text{ V} \\ \Delta I_{\text{L\_PP}} &= 300 \text{ mA} \\ f_{\text{sw}} &= 2.45 \text{ MHz} \\ \rightarrow L &\approx 1 \mu\text{H} \end{aligned}$$



9.2.2.2.3 Compensation of the BUCK2 and BUCK3 Converters

The regulators operate in forced continuous mode, and have internal frequency compensation. The frequency response can be adjusted to the selected LC filter by setting the COMP2 and COMP3 pin low, high, or floating. After selecting the output inductor value as previously described, the output capacitor must be chosen so that the  $L \times C_{OUT} \times V_{BUCK2/3}$  product is equal to or less than one of the three values, as listed in Table 4.

Table 4. Compensation Settings

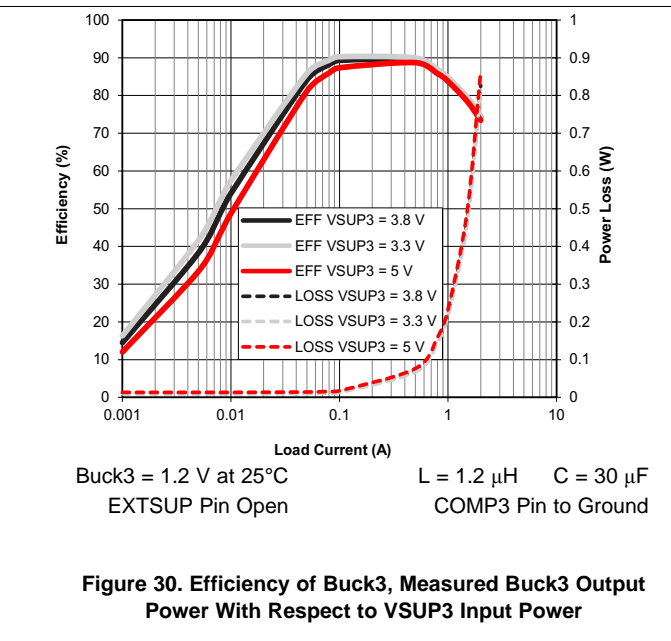
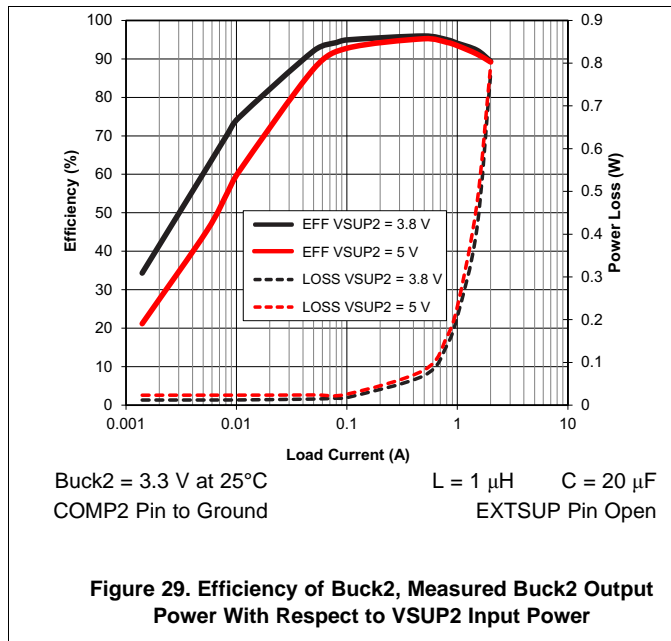
COMP 2/3	$L \times C_{OUT} \times V_{BUCK2/3}$	EXAMPLE COMPONENTS
= 0 V	$80 \mu\text{F} \times \mu\text{H} \times \text{V}$	$30 \mu\text{F} \times 2.2 \mu\text{H} \times 1.2 \text{V}$
= OPEN	$160 \mu\text{F} \times \mu\text{H} \times \text{V}$	$50 \mu\text{F} \times 1.8 \mu\text{H} \times 1.8 \text{V}$
= VREG	$320 \mu\text{F} \times \mu\text{H} \times \text{V}$	$150 \mu\text{F} \times 2.2 \mu\text{H} \times 1.2 \text{V}$

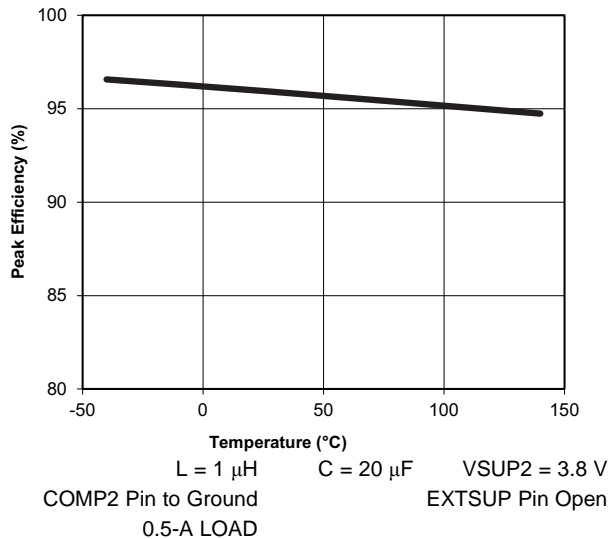
Larger output capacitors can be used if a feed-forward capacitor is placed across the upper resistance,  $R_y$ , of the feedback divider. This works effectively for output voltages  $> 2 \text{V}$ . With an RC product greater than  $10 \mu\text{s}$ , the effective  $V_{BUCK2/3}$  at higher frequencies can be assumed as  $0.8 \text{V}$ , thus allowing an output capacitor increase by a factor equal to the ratio of the output voltage to  $0.8 \text{V}$ .

9.2.2.2.4 Bootstrap Capacitor for the BUCK2/3 Converters

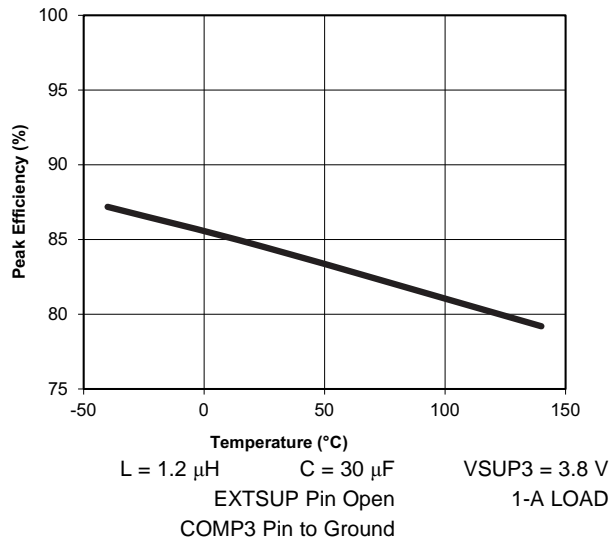
The BUCK2 and BUCK3 converters require a bootstrap capacitor. This bootstrap capacitor must be  $0.1 \mu\text{F}$ . The bootstrap capacitor is located between the PH2 pin and the BOOT2 pin and between the PH3 pin and the BOOT3 pin (see Figure 28). The bootstrap capacitor must be a high-quality ceramic type with X7R or X5R grade dielectric for temperature stability.

9.2.2.3 BUCK2 and BUCK3 Application Curves

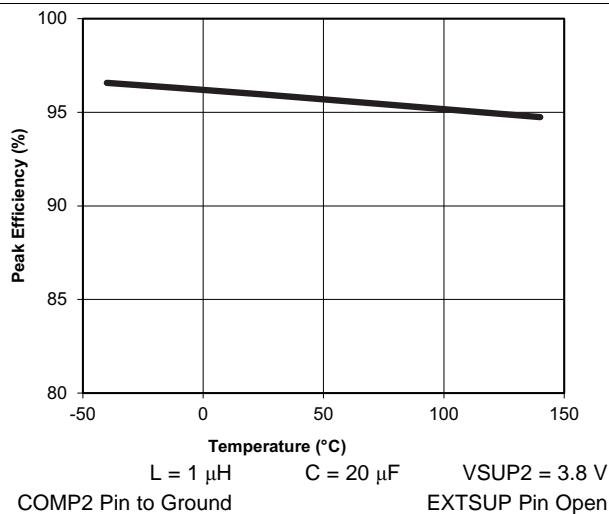




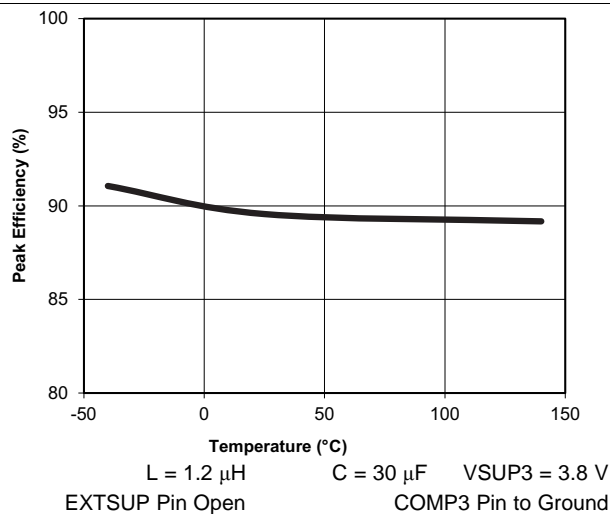
**Figure 31. Buck2 = 3.3-V Efficiency at 0.5 A Versus Temperature, Measured Buck2 Output Power With Respect to VSUP2 Input Power**



**Figure 32. Buck3 = 1.2-V Efficiency at 1 A Versus Temperature, Measured Buck3 Output Power With Respect to VSUP3 Input Power**

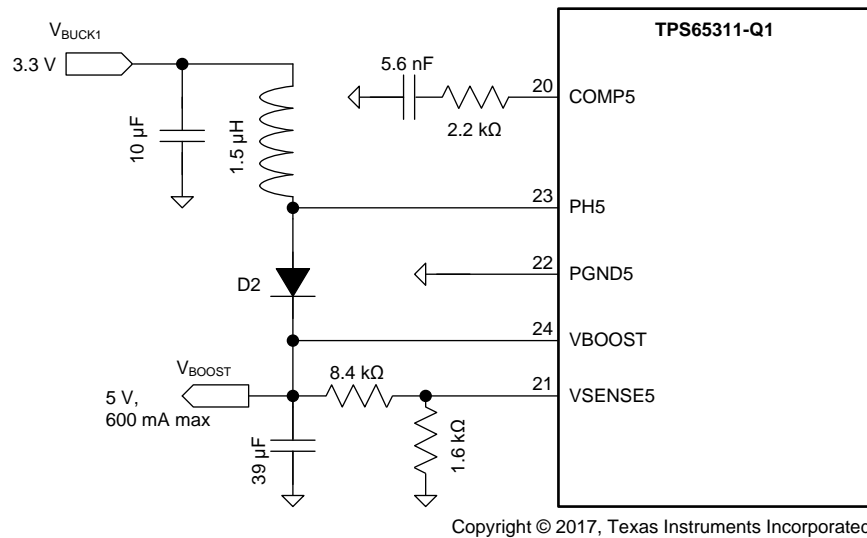


**Figure 33. Buck2 = 3.3-V Peak Efficiency Versus Temperature, Measured Buck2 Output Power With Respect to VSUP2 Input Power**



**Figure 34. Buck3 = 1.2-V Peak Efficiency Versus Temperature, Measured Buck3 Output Power With Respect to VSUP3 Input Power**

## 9.2.3 BOOST Converter



**Figure 35. BOOST Converter Schematic**

### 9.2.3.1 Design Requirements

For this design example, use the parameters listed in [Table 5](#).

**Table 5. Design Parameters**

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	3.3 V
Output voltage ( $V_{\text{BOOST}}$ )	5 V
Peak coil current ( $I_{\text{peak\_coil}}$ )	1 A
Maximum output current $I_{\text{OUT}}$	≈ 600 mA
Output current ripple $\Delta I_{\text{L\_PP}}$	300 mA
Switching frequency ( $f_{\text{SWBOOST}}$ )	2.45 MHz

### 9.2.3.2 Detailed Design Procedure

#### 9.2.3.2.1 Adjusting the Output Voltage for the Boost Converter

A resistor divider from the output node to the VSENSE5 pin sets the output voltage. TI recommends using 1% tolerance or better divider resistors. Start with a value of 1.6 kΩ for the  $R_x$  resistor and use [Equation 10](#) to calculate  $R_y$  (see [Figure 35](#)).

$$R_y = \frac{R_x \times (V_{\text{BOOST}} - 0.8 \text{ V})}{0.8 \text{ V}} \quad (10)$$

Therefore, for the value of  $V_{\text{BOOST}}$  to equal to 5 V, the value of  $R_y$  must be 8.4 kΩ.

#### 9.2.3.2.2 Output Inductor and Capacitor Selection for the BOOST Converter

The inductor value  $L$  depends on the allowed ripple current  $\Delta I_{\text{L\_PP}}$  in the coil at chosen input voltage  $V_{\text{IN}}$  and output voltage  $V_{\text{OUT}}$ , and given switching frequency  $f_{\text{sw}}$ :

$$L = \frac{V_{\text{IN}} \times (V_{\text{OUT}} - V_{\text{IN}})}{\Delta I_{\text{L\_PP}} \times V_{\text{OUT}} \times f_{\text{sw}}} \quad (11)$$

For example:

$$V_{\text{IN}} = 3.3 \text{ V (from BUCK1)}$$

$$V_{\text{OUT}} = 5 \text{ V}$$

$$\begin{aligned}\Delta I_{L\_PP} &= 300 \text{ mA (30\% of 1-A peak current)} \\ f_{SW} &= 2.45 \text{ MHz} \\ \rightarrow L &\approx 1.5 \text{ }\mu\text{H}\end{aligned}$$

The capacitor value  $C_{OUT}$  must be selected such that the L-C double-pole frequency  $F_{LC}$  is in the range of 10 kHz–15 kHz. The  $F_{LC}$  is given by [Equation 12](#):

$$F_{LC} = \frac{V_{IN}}{2 \times \pi \times V_{OUT} \times \sqrt{L \times C_{OUT}}} \quad (12)$$

The right half-plane zero  $F_{RHPZ}$ , as given in [Equation 13](#), must be  $> 200$  kHz:

$$F_{RHPZ} = \frac{V_{IN}^2}{2 \times \pi \times L \times I_{OUT} \times V_{OUT}} > 200 \text{ kHz}$$

where

- $I_{OUT}$  represents the load current (13)

If the condition  $F_{RHPZ} > 200$  kHz is not satisfied, L and therefore  $C_{OUT}$  have to be recalculated.

### 9.2.3.2.3 Compensation of the BOOST Converter

The BOOST converter requires an external R-C network for compensation (see [Figure 15](#), COMP5). The components can be calculated using [Equation 14](#) and [Equation 15](#):

$$R = 120 \times V_{IN} \times \left( \frac{F_{BW}}{F_{LC}} \right)^2 \quad (14)$$

$$C = \frac{1}{2 \times \pi \times R \times F_{LC}}$$

where

- $F_{BW}$  represents the bandwidth of the regulation loop, and must be set to 30 kHz
- $F_{LC}$  represents the L-C double-pole frequency, as mentioned previously (15)

For example:

$$\begin{aligned}V_{IN} &= 3.3 \text{ V (from BUCK1)} \\ V_{OUT} &= 5 \text{ V} \\ L &= 1.5 \text{ }\mu\text{H} \\ C &= 39 \text{ }\mu\text{F} \\ \rightarrow F_{LC} &= 13.7 \text{ kHz} \\ F_{BW} &= 30 \text{ kHz} \\ \rightarrow R &\approx 2.2 \text{ k}\Omega \\ \rightarrow C &\approx 5.6 \text{ nF}\end{aligned}$$

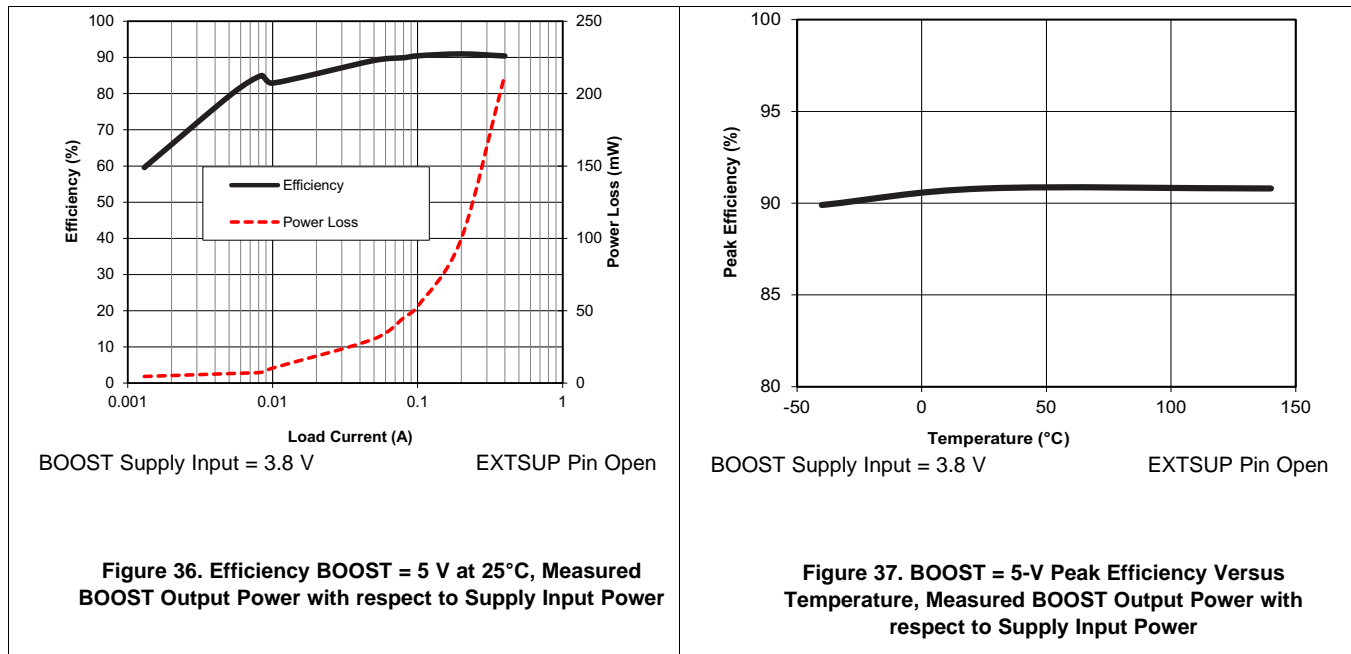
Stability and load step response must be verified in measurements to fine tune the values of the compensation components.

### 9.2.3.2.4 Output Diode for the BOOST Converter

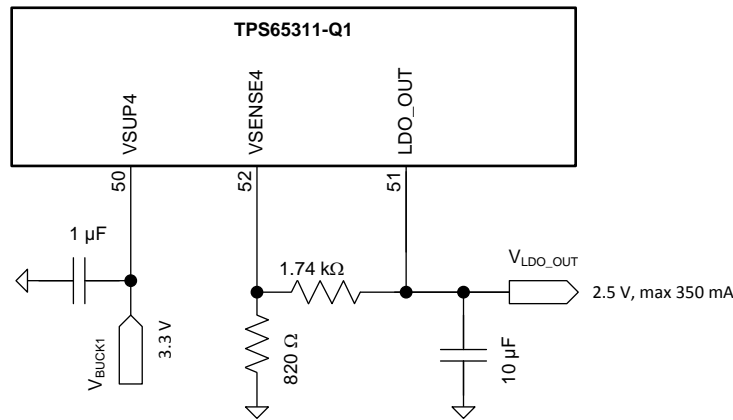
The BOOST converter requires an external output diode between the PH5 pin and VBOOST pin (see [Figure 35](#), component D2). The selected diode must have a reverse voltage rating equal to or greater than the  $V_{BOOST}$  output voltage. The peak current rating of the diode must be greater than the maximum inductor current. The diode must also have a low forward voltage in order to reduce the power losses. Therefore, Schottky diodes are typically a good choice for the catch diode.

Also, select a diode with an appropriate power rating, because the diode conducts the output current during the off-time of the internal power switch.

### 9.2.3.3 BOOST Converter Application Curves



### 9.2.4 Linear Regulator



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**Figure 38. Linear Regulator Schematic**

#### 9.2.4.1 Design Requirements

For this design example, use the parameters listed in [Table 6](#).

**Table 6. Design Parameters**

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	3.3 V
Output voltage ( $V_{LDO\_OUT}$ )	2.5 V
Maximum output current ( $I_{OUT}$ )	350 mA

### 9.2.4.2 Detailed Design Procedure

#### 9.2.4.2.1 Adjusting the Output Voltage for the Linear Regulator

A resistor divider from the output node to the VSENSE4 pin sets the output voltage. TI recommends using 1% tolerance or better divider resistors. In order to get the minimum required load current of 1 mA for the linear regulator, start with a value of 820 Ω for the R<sub>x</sub> resistor and use Equation 16 to calculate R<sub>y</sub> (see Figure 38).

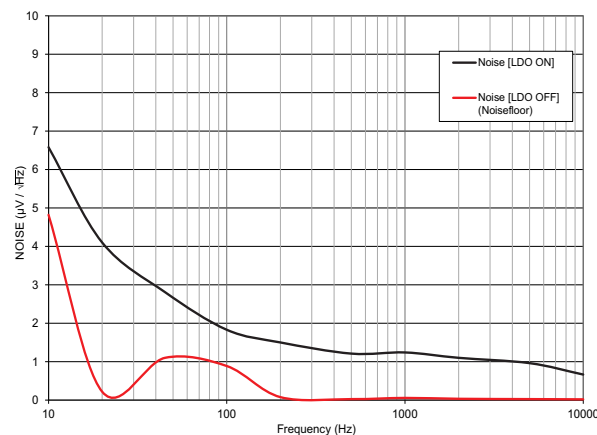
$$R_y = \frac{R_x \times (V_{LDO\_OUT} - 0.8 \text{ V})}{0.8 \text{ V}} \tag{16}$$

Therefore, for the value of V<sub>LDO\_OUT</sub> to equal to 2.5 V, the value of R<sub>y</sub> must be 1.74 kΩ.

#### 9.2.4.2.2 Output Capacitance for the Linear Regulator

The linear regulator requires an external output capacitance with a value between 6 μF and 50 μF.

#### 9.2.4.3 Linear Regulator Application Curve



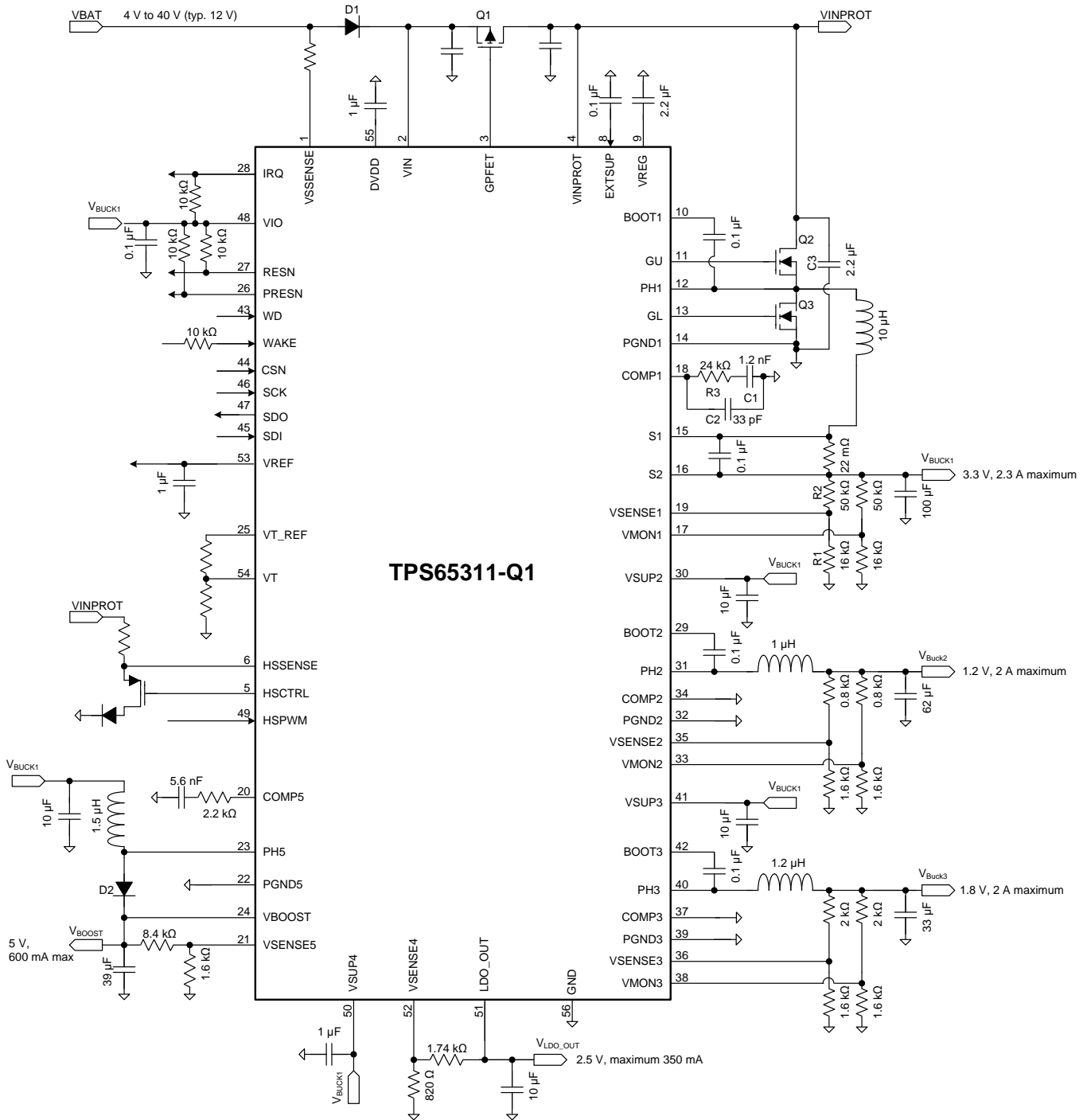
**Figure 39. LDO Noise Density**

## 10 Power Supply Recommendations

The device is designed to operate from an input voltage supply range between 4 V and 40 V (see Figure 40 for reference). This input supply must be well regulated. In case the supply voltage in the application is likely to exceed 40 V, the external PMOS protection device as explained in External Protection must be applied between VIN and VINPROT pins. Furthermore, if the supply voltage in the application is likely to reach negative voltage (for example, reverse battery), a forward diode must be placed between the VSSENSE and VIN pins. A ceramic bypass capacitor with a value of 100 μF (typical) is recommended to be placed close to the VINPROT pin. For the VIN pin, a small ceramic capacitor of typical 1 μF is recommended. Also place 1-μF (typical) bypass capacitors to the DVDD and VREF pins, and 100-nF (typical) bypass capacitors to VIO pin. Furthermore, the VREG pin requires a bypass capacitor of 2.2 μF (typical).

The BUCK1 output voltage is the recommended input supply for the BUCK2, BUCK3, and BOOST regulators. Place local, 10-μF (typical) bypass capacitors at the VSUP2 and VSUP3 pins and at the supply input of the BOOST in front of the BOOST-inductor. Also place a local, 1-μF (typical) bypass capacitor at the VSUP4 pin.

The EXTSUP pin can be used to improve efficiency. For the EXTSUP pin to improve efficiency, a voltage of more than 4.8 V is required in order to have VREG regulator supplied from EXTSUP pin. If the EXSUP pin is not used, the VINPROT pin supplies the VREG regulator. The EXTSUP pin requires a 100-nF (typical) bypass capacitor.



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Figure 40. Typical Application Schematic

## 11 Layout

### 11.1 Layout Guidelines

#### 11.1.1 Buck Controller

- Connect a local decoupling capacitor between the drain of Q3 and the source of Q2. The length of this trace loop should be short.
- The Kelvin-current sensing for the shunt resistor should have traces with minimum spacing, routed in parallel with each other. Place any filtering capacitor for noise near the S1-S2 pins.
- The resistor divider for sensing the output voltage connects between the positive pin of the output capacitor and the GND pin (IC signal ground). Do not locate these components and their traces near any switching nodes or high-current traces. The resistor divider for monitoring the output voltage is to be placed as close as possible to the sensing resistor divider, and should be connected to same traces.
- Connect the boot-strap capacitance between the PH1 and BOOT1 pins, and keep the length of these trace loops as short as possible.
- Connect the compensation network between the COMP1 pin and GND pin (IC signal ground).
- Connect a local decoupling capacitor between the VREG and PGND1 pin, and between the EXTSUP and PGND1 pin. The length of this trace loop should be short.

#### 11.1.2 Buck Converter

- Connect a local decoupling capacitor between VSUP2 and PGND2 respectively VSUP3 and PGND3 pins. The length of this trace loop should be short.
- The resistor divider for sensing the output voltage connects between the positive pin of the output capacitor and the GND pin (IC signal ground). Do not locate these components and their traces near any switching nodes or high-current traces. The resistor divider for monitoring the output voltage is to be placed as close as possible to the sensing resistor divider, and should be connected to same traces.
- Connect the boot-strap capacitance between the PH2 and BOOT2 respectively PH3 and BOOT3 pins, and keep the length of this trace loop as short as possible.
- If COMP2 and/or COMP3 are chosen to be connected to ground, use the signal ground trace connected to GND pin for this.

#### 11.1.3 Boost Converter

- The path formed from the input capacitor to the inductor and the PH5 pin should have short trace length. The same applies for the trace from the inductor to Schottky diode D2 to the output capacitor and the VBOOST pin. Connect the negative pin of the input capacitor and the PGND5 pin together with short trace lengths.
- The resistor divider for sensing the output voltage connects between the positive pin of the output capacitor and the GND pin (IC signal ground). Do not locate these components and their traces near any switching nodes or high-current traces.
- Connect the compensation network between the COMP5 pin and GND pin (IC signal ground).

#### 11.1.4 Linear Regulator

- Connect a local decoupling capacitor between VSUP4 and GND (IC signal ground) pins. The length of this trace loop should be short.
- The resistor divider for sensing the output voltage connects between the positive pin of the output capacitor and the GND pin (IC signal ground). Do not locate these components and their traces near any switching nodes or high-current traces.

#### 11.1.5 Other Considerations

- Short PGNDx and GND to the thermal pad.
- Use a star ground configuration if connecting to a non-ground plane system. Use tie-ins for the compensation-network ground, voltage-sense feedback ground, and local biasing bypass capacitor ground networks to this star ground.



## 11.2 Layout Example

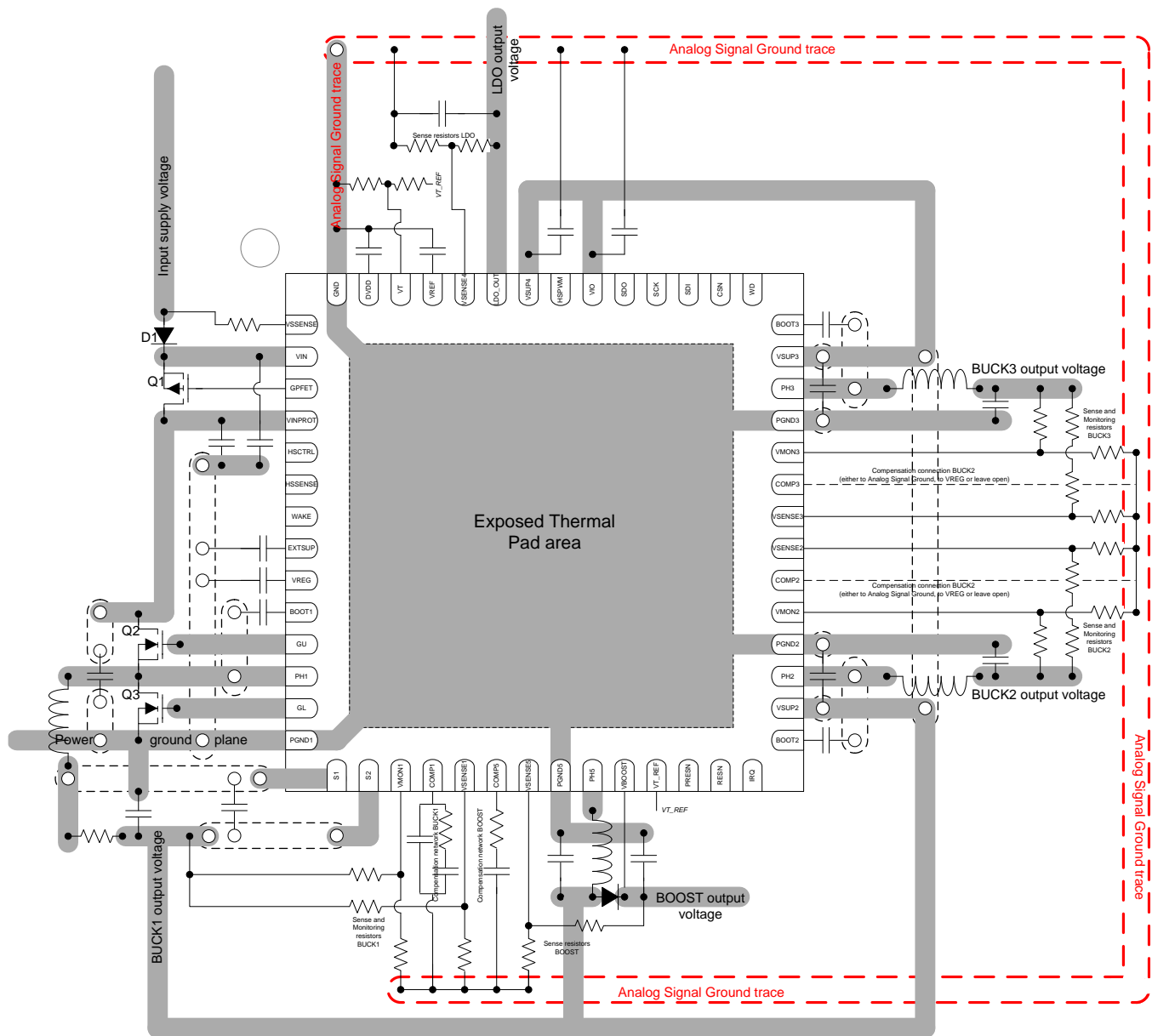


Figure 41. TPS65311-Q1 Layout Example

## 12 Device and Documentation Support

### 12.1 Documentation Support

For related documentation see the following:

- Texas Instruments, [TPS65310A-Q1 Efficiency application report](#)
- Texas Instruments, [TPS65310AEVM and TPS65311EVM Evaluation Module user's guide](#)
- Texas Instruments, [TPS65311-Q1 BUCK1 Controller DCR Current Sensing application report](#)
- Texas Instruments, [TPS65311-Q1/TPS65310A-Q1 GPFET Soft Start Using a Capacitor Between GPFET Pin and PMOS-Protection Switch Source Pin application report](#)
- Texas Instruments, [TPS65311-Q1/TPS65310A-Q1 Monitoring and Diagnostic Mechanism Definitions application report](#)

### 12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.4 Trademarks

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All other trademarks are the property of their respective owners.

### 12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 12.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS65311QRVJRQ1	ACTIVE	VQFN	RVJ	56	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	TPS65311	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

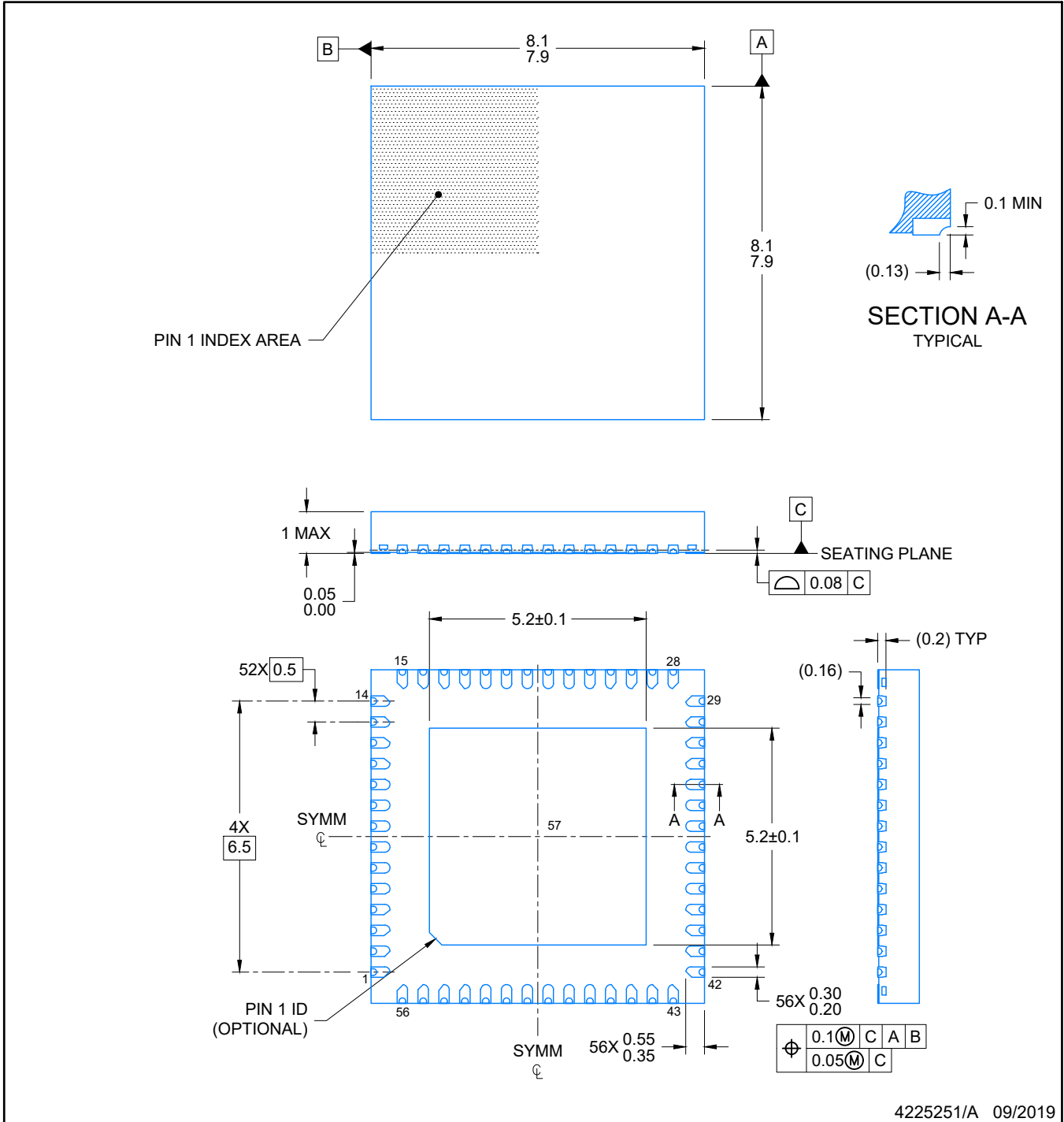

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65311QRVJRQ1	VQFN	RVJ	56	2000	330.0	16.4	8.3	8.3	2.25	12.0	16.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65311QRVJRQ1	VQFN	RVJ	56	2000	350.0	350.0	43.0



NOTES:

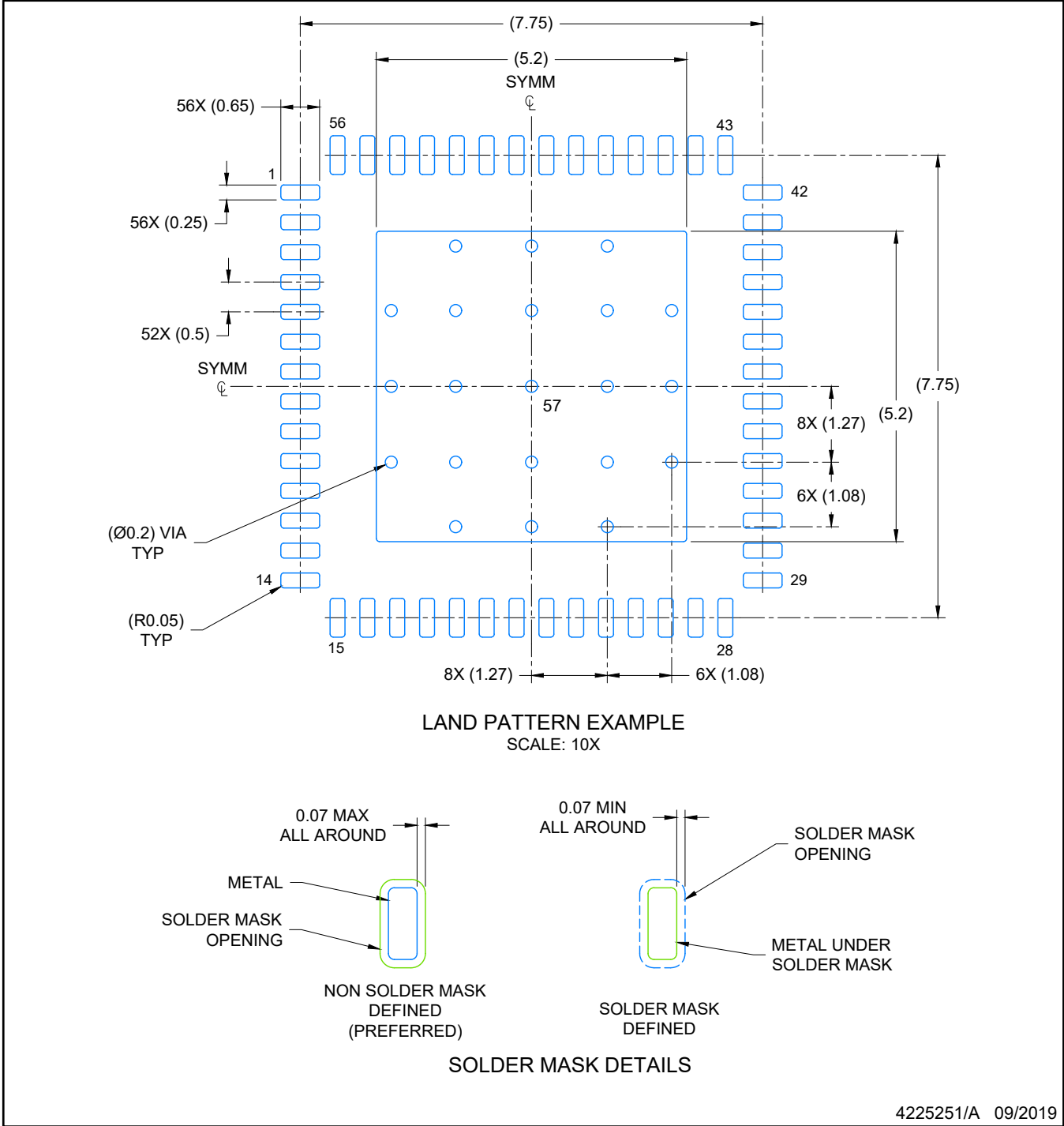
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

RVJ0056A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



NOTES: (continued)

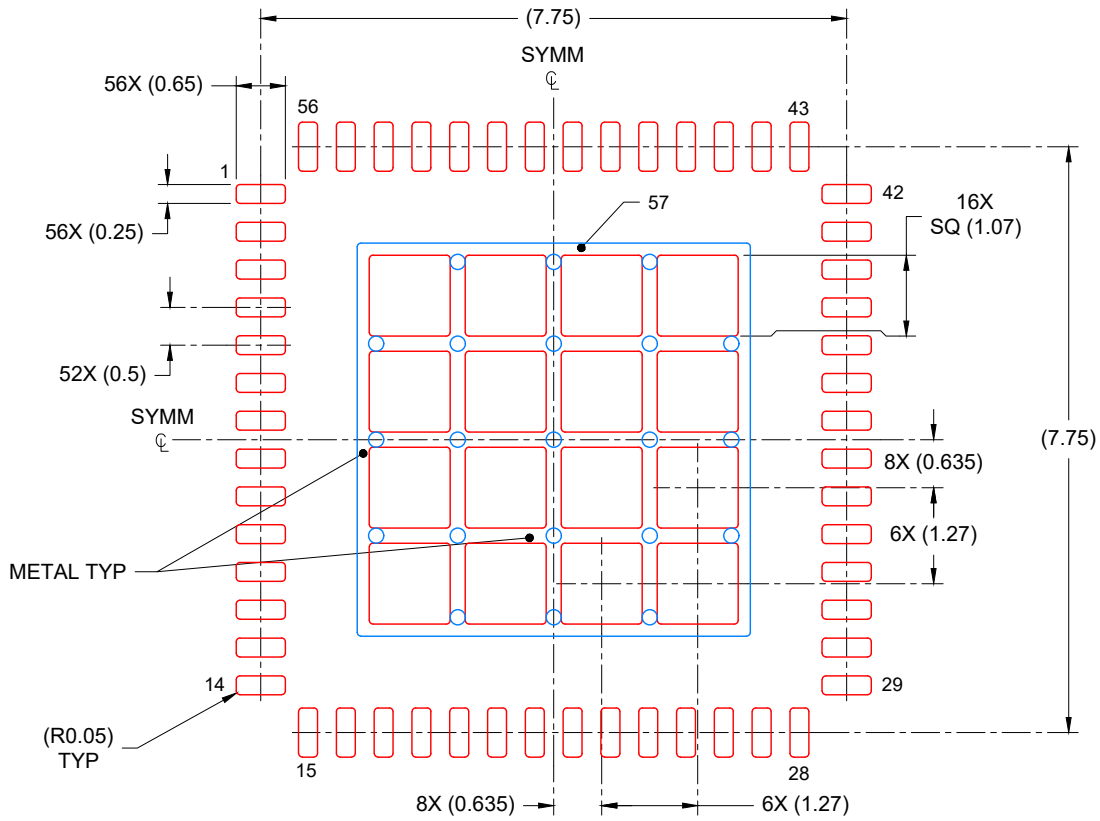
- 4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).
- 5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RVJ0056A

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD  
67% PRINTED COVERAGE BY AREA  
SCALE: 10X

4225251/A 09/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



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