CHANGE NOTIFICATION

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900

February 09, 2015

Dear Sir/Madam: PCN# 020915

Subject: Notification of Change to LTC6090, LTC6090-5 Die and Datasheet

Please be advised that Linear Technology has made improvements to the ESD protection devices of the LTC6090 and LTC6090-5. As these products now pass 4kV HBM ESD, the ESD Sensitivity Warning will be removed from page 2 of the datasheet. For informational purposes, CDM and MM ESD ratings are 1.5kV and 150V respectively. Also, internal resistor values were modified to simplify thermal shutdown functionality for single supply operation. The Thermal Shutdown application section of the data sheet will be modified to reflect this change as shown in attached mark-up pages of datasheet. This new revision silicon will ship with date codes 1514 and later. The data sheet specifications are unaffected by these changes.

Should you have any further questions, please feel free to contact me at 408-432-1900 ext. 2077, or by e-mail at JASON.HU@linear.com. If I do not hear from you by April 09, 2015, we will consider this change approved by your company.

Sincerely,

Jason Hu
Quality Assurance Engineer

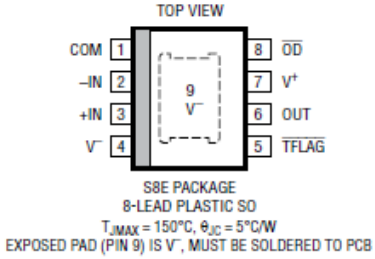
ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage (V^+ to V^-) 150V
COM ..... V^- to V^+
Input Voltage
$\overline{OD}$ ..... V^- to V^+ + 0.3V
+IN, –IN, ... V^- – 0.3V to V^+ + 0.3V
$\overline{OD}$ to COM ..... –3V to 7V
Input Current
+IN, –IN ..... ±10mA
$\overline{TFLAG}$ Output
$\overline{TFLAG}$ ..... V^- – 0.3V to V^+ + 0.3V
$\overline{TFLAG}$ to COM ..... –3V to 7V

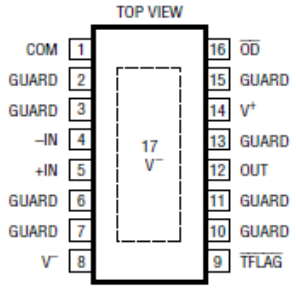
Output Current
Continuous (Note 2) ..... $50mA_{RMS}$
Operating Junction Temperature Range
(Note 3) ..... –40°C to 125°C
Specified Junction Temperature Range (Note 4)
LTC6090C ..... 0°C to 70°C
LTC6090I ..... –40°C to 85°C
LTC6090H ..... –40°C to 125°C
Junction Temperature (Note 5) ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

ESD Sensitive: The output pin (OUT) is sensitive to ESD. Any ESD greater than 500V may cause permanent damage to the device.

PIN CONFIGURATION



S8E PACKAGE
8-LEAD PLASTIC SO
T_{JMAX} = 150°C, θ_{JC} = 5°C/W
EXPOSED PAD (PIN 9) IS V^-, MUST BE SOLDERED TO PCB

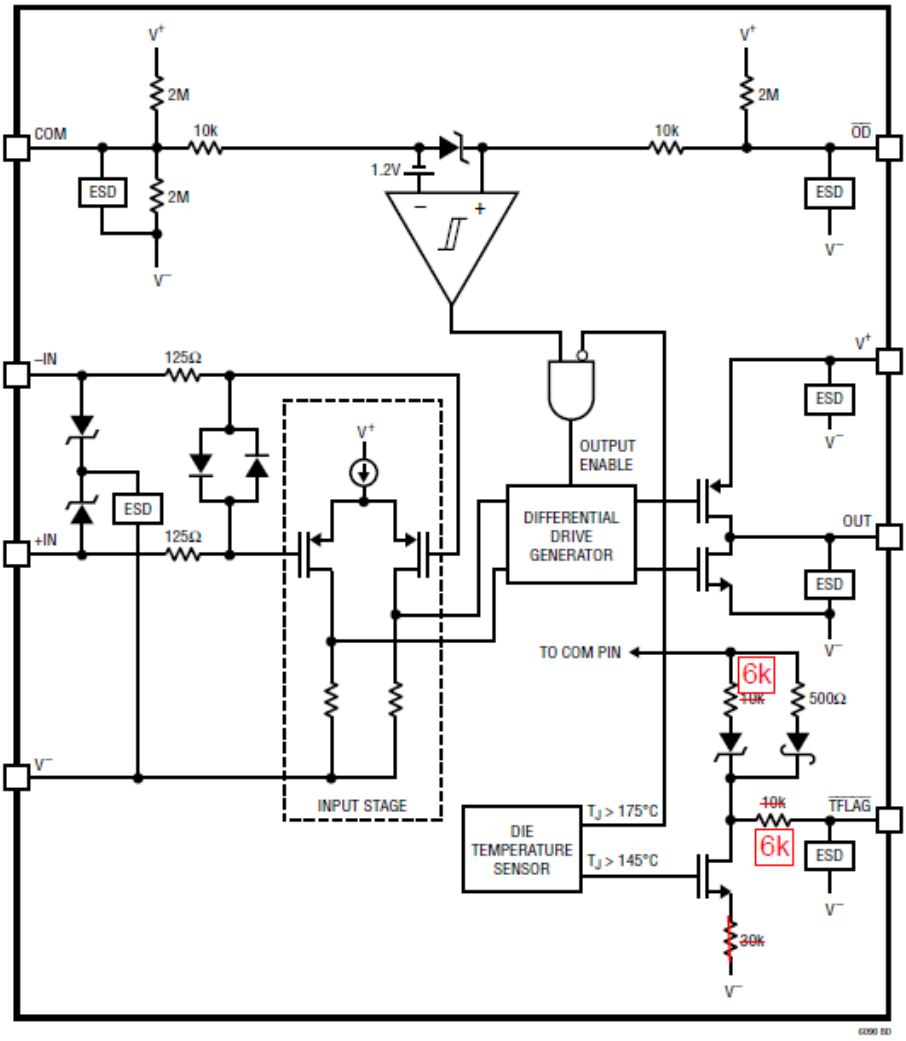


FE PACKAGE
16-LEAD PLASTIC TSSOP
T_{JMAX} = 150°C, θ_{JC} = 10°C/W
EXPOSED PAD (PIN 17) IS V^-, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	JUNCTION TEMPERATURE RANGE
LTC6090CS8E#PBF	LTC6090CS8E#TRPBF	6090	8-Lead Plastic SO	0°C to 70°C
LTC6090IS8E#PBF	LTC6090IS8E#TRPBF	6090	8-Lead Plastic SO	–40°C to 85°C
LTC6090HS8E#PBF	LTC6090HS8E#TRPBF	6090	8-Lead Plastic SO	–40°C to 125°C
LTC6090CFE#PBF	LTC6090CFE#TRPBF	6090FE	16-Lead Plastic TSSOP	0°C to 70°C
LTC6090IFE#PBF	LTC6090IFE#TRPBF	6090FE	16-Lead Plastic TSSOP	–40°C to 85°C
LTC6090HFE#PBF	LTC6090HFE#TRPBF	6090FE	16-Lead Plastic TSSOP	–40°C to 125°C

BLOCK DIAGRAM



APPLICATIONS INFORMATION

General

The LTC6090 high voltage operational amplifier is designed in a Linear Technology proprietary process enabling a rail-to-rail output stage with a 140V supply while maintaining precision, low offset, and low noise.

Power Supply

The LTC6090 works off single or split supplies. Split supplies can be balanced or unbalanced. For example, two ±70V supplies can be used, or a 100V and –40V supply can be used. For single supply applications place a high quality surface mount ceramic 0.1µF bypass capacitor between the supply pins close to the part. For dual supply applications use two high quality surface mount ceramic capacitors between V^+ to ground, and V^- to ground located close to the part. When using split supplies, supply sequencing does not cause problems.

Input Protection

As shown in the block diagram, the LTC6090 has a comprehensive protection network to prevent damage to the input devices. The current limiting resistors and back to back diodes are to keep the inputs from being driven apart. The voltage-current relationship combines exponential and resistive until the voltage difference between the pins reach 12V.

At that point the Zeners turn on. Additional current into the pins will snap back the input differential voltage to 9V. In the event of an ESD strike between an input and V^-, the voltage clamps and ESD device fire providing a current path to V^- protecting the input devices.

The input pin protection is designed to protect against momentary ESD events. A repetitive large fast input swing (>5.5V and <20ns rise time) will cause repeated stress on the MOSFET input devices. When in such an application, anti-parallel diodes (1N4148) should be connected between the inputs to limit the swing.

Feedback Resistor Selection

To get the most accuracy, the feedback resistor should be chosen carefully. Consider an amplifier with $A_V = -50$ and a 5k feedback resistor. A 1V input will cause the output to rise to 50V, causing 10mA to flow through the feedback resistor. The power dissipated in the output stage will create thermal feedback to the input stage potentially causing shifts in offset voltage. A better choice is a 50k feedback resistor reducing the current in the feedback resistor to 1mA.

Interfacing to Low Voltage Circuits

The COM pin is provided to set a common signal ground for communication to a microprocessor or other low voltage logic circuit. The COM pin should be tied to the low voltage ground as shown in Figure 1. If left floating, the internal resistive voltage divider will cause the COM pin to rise 30% above mid-supply. The COM, $\overline{OD}$, and $\overline{TFLAG}$ pins are protected from overvoltage by internal Zener diodes and current limiting resistors. Extra care should be taken to observe the absolute maximum voltage limits between ($\overline{OD}$ and COM) and between ($\overline{TFLAG}$ and COM). Voltage limits between these pins must remain between –3V and 7V.

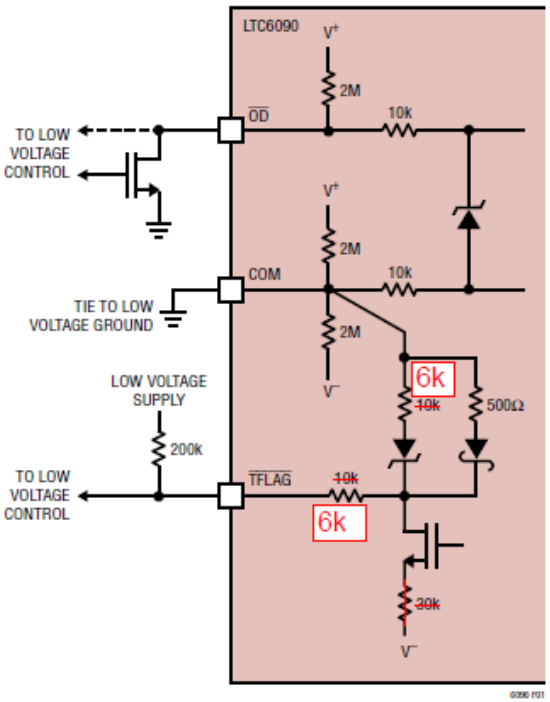


Figure 1. Low Voltage Interface

APPLICATIONS INFORMATION

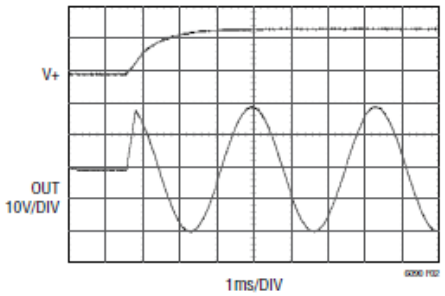


Figure 2. Starting Up

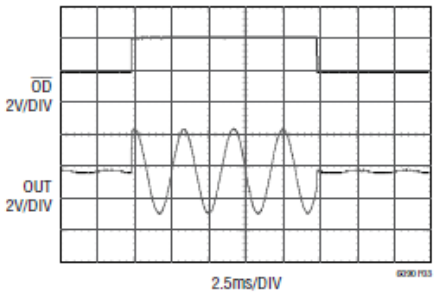


Figure 3. LTC6090 Output Disable Function

Output Disable

The $\overline{OD}$ pin is an active low disable with an internal 2MΩ resistor that will pull up the $\overline{OD}$ pin enabling the output stage if left open. The $\overline{OD}$ pin voltage is limited by an internal Zener diode. When the $\overline{OD}$ pin is brought low to within 0.65V of the COM pin, the output stage is disabled, leaving the bias and input circuits enabled. This results in 580µA (typical) standby current through the device. The $\overline{OD}$ pin can be directly connected to the low voltage logic or an open drain NMOS device as shown in Figure 1.

For simplest shutdown operation, float the COM pin, and tie the $\overline{OD}$ pin to the $\overline{TFLAG}$ pin. This will float the low voltage control pins, and the overtemperature circuit will safely shutdown the output stage if the die temperature reaches 145°C.

Extra care should be taken to observe the absolute maximum voltage limits between ($\overline{OD}$ and COM) and between ($\overline{TFLAG}$ and COM). Voltage limits between these pins must remain between –3V and 7V.

When coming out of shutdown the LTC6090 bias circuits and input stage are already powered up leaving only the output stage to turn on and drive to the proper output voltage. Figures 2 and 3 show the part starting up and coming out of shutdown, respectively.

Thermal Shutdown

The $\overline{TFLAG}$ pin is an open drain output pin that sinks 200µA (typical) when the die temperature exceeds 145°C. The temperature sensor has 5°C of hysteresis requiring the part to cool to 140°C before disabling the $\overline{TFLAG}$ pin. Extra care should be taken to observe the absolute maximum voltage limits between ($\overline{OD}$ and COM) and between ($\overline{TFLAG}$ and COM). Voltage limits between these pins must remain between –3V and 7V.

~~To guarantee proper operation of thermal shutdown, a few precautions must be followed when interfacing the output disable pin ($\overline{OD}$) to the $\overline{TFLAG}$ pin:~~

- ~~As already stated, if the COM pin is left floating, simply tying $\overline{OD}$ to $\overline{TFLAG}$ (as shown in Figure 4) will result in the proper operation of thermal shutdown regardless of the supply voltages chosen. The output stage will be safely disabled should the die temperature reach 145°C. The COM pin may also be tied to ground in this configuration so long as V^- is biased more negatively than –3V with respect to ground for proper thermal shutdown operation.~~
- ~~In the case where the COM pin is grounded, but the V^- supply is within 0V and –3V of ground, a logic buffer must be used to force $\overline{OD}$ to a logic low as shown in Figure 5. The pullup resistor (R_{PULLUP}) of Figure 5 must be chosen large enough to guarantee a logic low for the logic buffer. For most CMOS, this requires at least 402k of pullup resistance. Alternatively, the logic buffer is not needed if you float the COM pin. With COM floating, you may simply tie $\overline{OD}$ directly to $\overline{TFLAG}$ for proper thermal shutdown operation.~~

For sa... old sh... rises t... circui... devic... **Degra... the junction temperature of the device exceeds 150°C.**

Tying the TFLAG pin to the OD pin will automatically shut down the output stage as shown in Figure 4. This will ensure the junction temperature does not exceed 150C.

APPLICATIONS INFORMATION

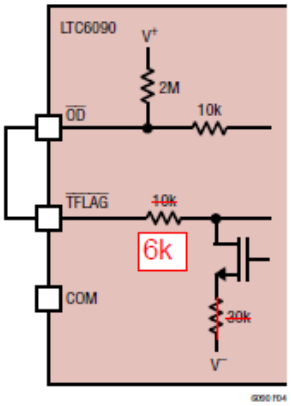


Figure 4. Automatic Thermal Output Disable Using the $\overline{\text{TFLAG}}$ Pin

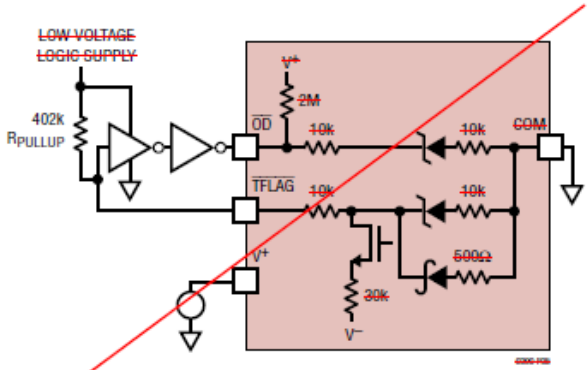


Figure 5. Automatic Thermal Output Disable Using the $\overline{\text{TFLAG}}$ Pin with Unbalanced Split Supply or Single Supply Applications

Board Layout

The LTC6090 is a precision low offset high gain amplifier that requires good analog PCB layout techniques to maintain high performance. Start with a ground plane that is star connected. Pull back the ground plane from any high voltage vias. Critical signals such as the inputs should have short and narrow PCB traces to reduce stray capacitance which also improves stability. Use high quality surface mount ceramic capacitors to bypass the supply(s).

In addition to the typical layout issues encountered with a precision operational amplifier, there are the issues of high voltage and high power. Important consideration for high voltage traces are spacing, humidity and dust. High voltage electric fields between adjacent conductors attract dust. Moisture is absorbed by the dust and can contribute to board leakage and electrical breakdown.

It is important to clean the PCB after soldering down the part. Solder flux will accumulate dust and become a leakage hazard. It is recommended to clean the PCB with a solvent, or simply use soap and water to remove residue. Baking the PCB will remove left over moisture. Depending on the application, a special low leakage board material may be considered.

The TSSOP package has guard pins for applications that require a guard ring. An example schematic diagram and PCB layout is shown in Figures 6a and 6b, respectively, of a circuit using a guard ring to protect the –IN pin. The guard ring completely encloses the high impedance node –IN. To simplify the PCB layout avoid using vias on this node. In addition, the solder mask should be pulled back along the guard ring exposing the metal. To help the spacing between nodes, one of the extra pins on the TSSOP package is used to route the guard ring behind the –IN pin. The PCB should be thoroughly cleaned after soldering to ensure there is no solder paste between the exposed pad (Pin 17) and the guard ring.

Power Dissipation

With a supply voltage of 140V it doesn't take much current to consume a lot of power. Consider that 10mA at 140V consumes 1.4W of power and needs to be dissipated in a small plastic SO package. To aid in power dissipation both LTC6090 packages have exposed pads for low thermal resistance. The amount of metal connected to the exposed pad will lower the θ_{JA} of a package. An optimal amount of PCB metal connected to the SO package will lower the junction to ambient thermal resistance down to 33°C/W. If minimal metal is used, the θ_{JA} could more than double (see Table 1). If the exposed pad has no metal beneath it, θ_{JA} could be as high 120°C/W.

It's recommended that the exposed pad have as much PCB metal connected to it as reasonably available. The more PCB metal connected to the exposed pad, the lower the thermal resistance. Use multiple vias from the exposed pad to the V^- supply plane. The exposed pad is electrically connected to the V^- pin. In addition, a heat sink may be necessary if operating near maximum junction temperature. See Table 1 for guidance on how thermal resistance changes as a function of metal area connected to the exposed pad.