Process Change Notification

PCN Number: PCN-2019-114 **PCN Notification Date:** 03/08/2019

Informational PCN

CS47L15 Data Sheet revision from F1 to F2

Dear Customer,

This notification is to advise you of the following change(s).

The Data Sheet for CS47L15 has been updated to reflect the following change(s):

- Change to DSP memory during Software Reset due to a change in the OTP (One Time Programmable), which results in the Firmware Memory of the DSP not being retained following a Software Reset.
- Clarification of System-Clock Control requirements.
- Correction to the HPD_DACVAL limit.
- Material ordering compliancy update.

The described change(s) within this PCN will not take effect (i.e. Shipped) any earlier than 30 days from this PCN notification or the successful completion of the Cirrus Logic qualification, unless a customer agreement has been reached on an earlier implementation of the identified change.

Cirrus Logic would like to take this opportunity to thank our customers for their cooperation and assistance in this respective matter. Any specific or immediate inquiries should be directed to your local Field Sales Representative.

If you have any questions, please contact your Sales Representative.

Sincerely,

Quality Systems Administrator
Cirrus Logic Corporate Quality
Phone: +1(512) 851-4000

Process Change Notification

PCN Number: PCN-2019-114 **PCN Notification Date:** 03/08/2019

Products Affected:

The devices listed on this page are the complete list of affected devices. According to our records, these are the devices that you have purchased within the past twenty-four (24) months. The corresponding customer part number is also listed, if available.

Technical details of this Process / Product Change follow on the next page(s).

Title:	CS47L15 Data Sheet revision from F1 to F2						
Customer Contact:	Local Field Sales Representative		**Phone:** (512) 851-4000		**Dept:**	Corporate Quality	
Proposed 1st Ship Date:		NA	**Estimated Sample Availability Date:**			NA	
Change Type:							
	Assembly Site		Assembly Process		Assembly Materials		
	Wafer Fab Site		Wafer Fab Process		Wafer Fab Materials		
	Wafer Bump Site		Wafer Bump Process		Wafer Bump Material		
	Test Site		Test Process		Design		
X	Electrical Specification		Mechanical Specification		Part Number		
	Packing/Shipping/Labeling	X	Other				
Comments:	Data Sheet Update						

PCN Details

Description of Change:

The Data Sheet for CS47L15 has been updated to reflect the following change(s):

- Change to DSP memory during Software Reset due to a change in the OTP (One Time Programmable), which results in the Firmware Memory of the DSP not being retained following a Software Reset.
- Clarification of System-Clock Control requirements.
- Correction to the HPD_DACVAL limit.
- Material ordering compliancy update.

Data Sheet Reference Link: https://www.cirrus.com/products/cs47l15/

Datasheet of CS47L15 has been revised from version F1 to version F2:

Change	***Section***
Software Reset Behavior Updated	Section 4.4.3.1, Table 4-30 (Section 4.4.3.6), Section 4.14.3, Section 4.19, Section 5.2
Clarification of System-Clock Control Requirements	Section 4.13.4.2, Table 4-82
Correction to HPD_DACVAL Limit	Section 4.9.4.2
Material Ordering Compliancy Update	Section 9

Software Reset Behavior Updated:

5.2 Resets Summary - Page 230

Version F1 (Before change)

Table 5-3. Memory Reset Summary

Reset Type	Always-On Registers [1]	Other Registers	Control-Write Sequencer Memory	DSP Firmware Memory
Power-on reset	Reset	Reset	Reset	Reset
Hardware reset	Reset	Reset	Reset	Reset
Software reset	Reset	Reset	Retained	Retained [2]
Sleep Mode	Retained	Reset	Reset	Reset

1. See Section 4.10 for details of Sleep Mode and the always-on registers.
2. To retain the DSP firmware memory contents during software reset, it must be ensured that DCVDD is held above its reset threshold.

Version F2 (After change)

Table 5-3. Memory Reset Summary

Reset Type	Always-On Registers [1]	Other Registers	Control-Write Sequencer Memory	DSP Firmware Memory
Power-on reset	Reset	Reset	Reset	Undefined
Hardware reset	Reset	Reset	Reset	Undefined
Software reset	Reset	Reset	Retained	Undefined
Sleep Mode	Retained	Reset	Reset	Undefined

1. See Section 4.10 for details of Sleep Mode and the always-on registers.

4.4.3.1 DSP Memory - Page 81

Version F1 (Before change)

4.4.3.1 DSP Memory

The DSP memory (program, X-data, Y-data, and coefficient) is enabled by setting DSP1_MEM_ENA. This memory must be enabled (DSP1_MEM_ENA = 1) for read/write access, code execution, and DMA functions. The DSP memory is disabled, and the contents lost, whenever the DSP1_MEM_ENA bit is cleared.

The DSP1_MEM_ENA bit is not affected by software reset; it remains in its previous state under software reset conditions. Accordingly, the DSP memory contents are maintained through software reset, provided DCVDD is held above its reset threshold.

The DSP firmware memory is always cleared under power-on reset, hardware reset, and Sleep Mode conditions. See Section 5.2 for a summary of the CS47L15 reset behavior.

Version F2 (After change)

4.4.3.1 DSP Memory

The DSP memory (program, X-data, Y-data, and coefficient) is enabled by setting DSP1_MEM_ENA. This memory must be enabled (DSP1_MEM_ENA = 1) for read/write access, code execution, and DMA functions. The DSP memory is disabled, and the contents lost, whenever the DSP1_MEM_ENA bit is cleared.

The default value of DSP1_MEM_ENA (following power-on reset, hardware reset, software reset, or wake-up from Sleep Mode) is dependent on the master-boot function (see Section 4.14):

- If the master-boot function is selected, DSP1_MEM_ENA is set by default
- If the master-boot function is not selected, the DSP1_MEM_ENA is cleared by default

See Section 5.2 for a summary of the CS47L15 reset behavior.

Software Reset Behavior Updated: (Continued)

Table 4-30. DSP Memory and Clocking Control - Page 84

Version F1 (Before change)

Table 4-30. DSP Memory and Clocking Control

Register Address	Bit	Label	Default	Description
R1048064 (0xF_FE00) DSP1_Config_1	24	DSP1_FLL_AO_ CLKENA	0	DSP1 always-on clock control Selects the DSP1 clocking if DSPCLK is disabled 0 = No clock 1 = DSP1 is clocked directly from FLL_AO
	4	DSP1_MEM_ENA	0	DSP1 memory control 0 = Disabled 1 = Enabled The DSP1 memory contents are lost when DSP1_MEM_ENA =0. Note that this bit is not affected by software reset; it remains in its previous condition.
	1	DSP1_CORE_ENA	0	DSP1 enable. Controls the DSP1 firmware execution 0 = Disabled 1 = Enabled
	0	DSP1_START	—	DSP1 start Write 1 to start DSP1 firmware execution

Version F2 (After change)

Table 4-30. DSP Memory and Clocking Control

Register Address	Bit	Label	Default	Description
R1048064 (0xF_FE00) DSP1_Config_1	24	DSP1_FLL_AO_ CLKENA	0	DSP1 always-on clock control Selects the DSP1 clocking if DSPCLK is disabled 0 = No clock 1 = DSP1 is clocked directly from FLL_AO
	4	DSP1_MEM_ENA	0	DSP1 memory control 0 = Disabled 1 = Enabled The DSP1 memory contents are lost if DSP1_MEM_ENA=0. **Note:** If the master-boot function is selected (MSTRBOOT asserted), DSP1_MEM_ENA is set following power-up, hardware reset, software reset, and wake-up from Sleep Mode.
	1	DSP1_CORE_ENA	0	DSP1 enable. Controls the DSP1 firmware execution 0 = Disabled 1 = Enabled
	0	DSP1_START	—	DSP1 start Write 1 to start DSP1 firmware execution

Software Reset Behavior Updated: (Continued)

4.14.3 SPI Master-Boot Interface - Page 203

Version F1 (Before change)

4.14.3 SPI Master-Boot Interface

The SPI master-boot interface mode uses the $\overline{SS}$, SCLK, MOSI, and MISO pin functions, as described in Table 4-90. The interface connects directly to an external non-volatile memory (e.g., EEPROM or flash memory), enabling the CS47L15 to self-boot to an application-specific configuration and to be used independently of a host processor.

The SPI master-boot interface is selected using the MSTRBOOT pin—if a Logic 1 is detected on the MSTRBOOT pin during device start-up, the CS47L15 downloads the firmware and register-configuration data over the SPI master interface. This self-boot function is scheduled as part of power-on reset or hardware reset (assuming a Logic 1 is detected on the MSTRBOOT pin).

Version F2 (After change)

4.14.3 SPI Master-Boot Interface

The SPI master-boot interface mode uses the $\overline{SS}$, SCLK, MOSI, and MISO pin functions, as described in Table 4-90. The interface connects directly to an external non-volatile memory (e.g., EEPROM or flash memory), enabling the CS47L15 to self-boot to an application-specific configuration and to be used independently of a host processor.

The SPI master-boot interface is selected using the MSTRBOOT pin—if a Logic 1 is detected on the MSTRBOOT pin during device start-up, the CS47L15 downloads the firmware and register-configuration data over the SPI master interface. This self-boot function is scheduled as part of power-on reset, hardware reset, software reset, and wake-up from Sleep Mode (assuming a Logic 1 is detected on the MSTRBOOT pin).

4.19 Power-Up, Resets, and Device ID - Page 217~219

Version F1 (Before change)

4.19.3 Software Reset

A software reset is executed by writing any value to register R0. A software reset causes most of the CS47L15 control registers to be reset to their default states. Note that the control-write sequencer memory is retained during software reset.

4.19.5 Boot Sequence

Following power-on reset, hardware reset, software reset, or wake-up from Sleep Mode, a boot sequence is executed. The BOOT_DONE_STS*x* bits (see Table 4-109) are asserted on completion of the boot sequence. Control-register writes should not be attempted until BOOT_DONE_STS*x* has been asserted. Note that the BOOT_DONE_STS1 and BOOT_DONE_STS2 bits provide the same information.

The BOOT_DONE_STS*x* status is an input to the interrupt control circuit and can be used to trigger an interrupt event on completion of the boot sequence; see Section 4.12. Under default register conditions, a falling edge on the $\overline{IRQ}$ pin indicates completion of the boot sequence.

For details of the boot sequence, see Section 4.15.

An additional sequence of initialization settings must be written after the boot sequence has completed—this is specified in Table 4-108. The host system should ensure the CS47L15 is ready (i.e., BOOT_DONE_STS*x* is set) before scheduling these register operations.

Note: If the master-boot function is selected (see Section 4.14), the initialization sequence must be incorporated within the device configuration file on the external EEPROM.

Software Reset Behavior Updated: (Continued)

Table 4-108. CS47L15 Initialization Sequence

Control Register Writes
• Write 0x5555 to address 0x008C • Write 0xAAAA to address 0x008C • Write 0x0080 to address 0x0314 • Write 0x6023 to address 0x04A8 • Write 0x6023 to address 0x04A9 • Write 0x0008 to address 0x04D4 • Write 0x0F00 to address 0x04CF • Write 0xCCCC to address 0x008C • Write 0x3333 to address 0x008C

If the master-boot function is selected, the $\overline{\text{IRQ}}$ pin is asserted (Logic 0) after the normal boot sequence has completed. The subsequent behavior depends upon what event caused the boot sequence to occur:

- If the boot sequence was scheduled due to a power-on reset or hardware reset, the CS47L15 downloads data from the external EEPROM, and is configured according to the applicable user program data. Clearing the interrupt, and the subsequent behavior of the $\overline{\text{IRQ}}$ output, is dependent on the user program data.
- If the boot sequence was scheduled due to a software reset or wake-up from Sleep Mode, the CS47L15 does not download data from the external EEPROM. Caution is advised if scheduling a software reset or wake-up transition in master-boot applications.

The BOOT_DONE_STS*x* bits are defined in Table 4-109.

Table 4-109. Device Boot-Up Status

Register Address	Bit	Label	Default	Description
R6272 (0x1880) IRQ1_Raw_ Status_1	7	BOOT_DONE_ STS1	0	Boot Status 0 = Busy (boot sequence in progress) 1 = Idle (boot sequence completed) Control register writes should not be attempted until Boot Sequence has completed.
R6528 (0x1980) IRQ2_Raw_ Status_1	7	BOOT_DONE_ STS2	0	Boot Status 0 = Busy (boot sequence in progress) 1 = Idle (boot sequence completed) Control register writes should not be attempted until Boot Sequence has completed.

4.19.7 Write Sequencer and DSP Firmware Memory Control in Reset and Wake-Up

The control-write sequencer memory reverts to its default state following power-on reset, a hardware reset, or a Sleep Mode transition. The control sequences (including any user-defined sequences) are maintained in the sequencer memory through software reset.

The DSP firmware memory contents are cleared following power-on reset, a hardware reset, or a Sleep Mode transition. The firmware memory contents are not affected by software reset, provided DCVDD is held above its reset threshold.

See Section 5.2 for a summary of the CS47L15 memory reset conditions.

Software Reset Behavior Updated: (Continued)

Version F2 (After change)

4.19.3 Software Reset

A software reset is executed by writing any value to register R0. A software reset causes the CS47L15 control registers to be reset to their default states. Note that the control-write sequencer memory is retained during software reset. The DSP firmware-memory contents are not retained during software reset.

4.19.5 Boot Sequence

Following power-on reset, hardware reset, software reset, or wake-up from Sleep Mode, a boot sequence is executed. The BOOT_DONE_STS*x* bits (see Table 4-109) are asserted on completion of the boot sequence. Control-register writes should not be attempted until BOOT_DONE_STS*x* has been asserted. Note that the BOOT_DONE_STS1 and BOOT_DONE_STS2 bits provide the same information.

The BOOT_DONE_STS*x* status is an input to the interrupt control circuit and can be used to trigger an interrupt event on completion of the boot sequence; see Section 4.12. Under default register conditions, a falling edge on the IRQ pin indicates completion of the boot sequence.

For details of the boot sequence, see Section 4.15.

An additional sequence of initialization settings must be written after the boot sequence has completed—this is specified in Table 4-108. The host system should ensure the CS47L15 is ready (i.e., BOOT_DONE_STS*x* is set) before scheduling these register operations.

Note: If the master-boot function is selected (see Section 4.14), the initialization sequence must be incorporated within the device configuration file on the external EEPROM.

Table 4-108. CS47L15 Initialization Sequence

Control Register Writes
• Write 0x5555 to address 0x008C
• Write 0xAAAA to address 0x008C
• Write 0x0080 to address 0x0314
• Write 0x6023 to address 0x04A8
• Write 0x6023 to address 0x04A9
• Write 0x0008 to address 0x04D4
• Write 0x0F00 to address 0x04CF
• Write 0xCCCC to address 0x008C
• Write 0x3333 to address 0x008C

If the master-boot function is selected, the IRQ pin is asserted (Logic 0) after the normal boot sequence has completed. At this point, the CS47L15 starts to download data from the external EEPROM, and is configured according to the applicable user program data. Clearing the interrupt, and the subsequent behavior of the IRQ output, is dependent on the user program data.

The BOOT_DONE_STS*x* bits are defined in Table 4-109.

Table 4-109. Device Boot-Up Status

Register Address	Bit	Label	Default	Description
R6272 (0x1880) IRQ1_Raw_ Status_1	7	BOOT_DONE_ STS1	0	Boot Status 0 = Busy (boot sequence in progress) 1 = Idle (boot sequence completed) Control register writes should not be attempted until Boot Sequence has completed.
R6528 (0x1980) IRQ2_Raw_ Status_1	7	BOOT_DONE_ STS2	0	Boot Status 0 = Busy (boot sequence in progress) 1 = Idle (boot sequence completed) Control register writes should not be attempted until Boot Sequence has completed.

Software Reset Behavior Updated: (Continued)

4.19.7 Write Sequencer and DSP Firmware Memory Control in Reset and Wake-Up

The control-write sequencer memory reverts to its default state following power-on reset, a hardware reset, or a Sleep Mode transition. The control sequences (including any user-defined sequences) are maintained in the sequencer memory through software reset.

The DSP firmware-memory contents are undefined following power-on reset, hardware reset, software reset, or a Sleep Mode transition—the memory contents are not retained during these events.

See Section 5.2 for a summary of the CS47L15 memory reset conditions.

Clarification of System-Clock Control Requirements:

4.13.4.2 DSPCLK Configuration - Page 176

Version F1 (Before change)

The DSPCLK signal is enabled by setting DSP_CLK_ENA. The applicable clock source (MCLK*n*, AIF*n*BCLK, or FLL) must be enabled before setting DSP_CLK_ENA. This bit should be cleared when reconfiguring the clock sources.

Version F2 (After change)

The DSPCLK signal is enabled by setting DSP_CLK_ENA. The applicable clock source (MCLK*n*, AIF*n*BCLK, or FLL) must be enabled before setting DSP_CLK_ENA. This bit should be cleared before stopping or removing the applicable clock source.

Table 4-82. Clocking Control - Page 178, 179

Version F1 (Before change)

R257 (0x0101) System_Clock_1	15	SYSCLK_FRAC	0	SYSCLK Frequency 0 = SYSCLK is a multiple of 6.144MHz 1 = SYSCLK is a multiple of 5.6448MHz
	10:8	SYSCLK_ FREQ[2:0]	100	SYSCLK Frequency 000 = 6.144 MHz (5.6448 MHz) 001 = 12.288 MHz (11.2896 MHz) 010 = 24.576 MHz (22.5792 MHz) 011 = 49.152 MHz (45.1584 MHz) 100 = 98.304 MHz (90.3168 MHz) All other codes are reserved The frequencies in brackets apply for 44.1 kHz–related sample rates only (i.e., SAMPLE_RATE_*n* = 01XXX).
	6	SYSCLK_ENA	0	SYSCLK Control 0 = Disabled 1 = Enabled SYSCLK should only be enabled after the applicable clock source has been configured and enabled. Set this bit to 0 when reconfiguring the clock sources. All digital core (audio mixer) x_SRC fields must be cleared before clearing SYSCLK_ENA = 0.

Clarification of System-Clock Control Requirements: (Continued)

R288 (0x0120) DSP_Clock_1	6	DSP_CLK_ENA	0	DSPCLK Control 0 = Disabled 1 = Enabled DSPCLK should only be enabled after the applicable clock source has been configured and enabled. Set this bit to 0 when reconfiguring the clock sources.
	3:0	DSP_CLK_ SRC[3:0]	0100	DSPCLK Source 0000 = MCLK1 0001 = MCLK2 0100 = FLL1 (x1.5) 0111 = FLL_AO (x3) 1000 = AIF1BCLK 1001 = AIF2BCLK 1010 = AIF3BCLK 1111 = FLL_AO All other codes are reserved

Version F2 (After change)

R257 (0x0101) System_Clock_1	15	SYSCLK_FRAC	0	SYSCLK Frequency 0 = SYSCLK is a multiple of 6.144MHz 1 = SYSCLK is a multiple of 5.6448MHz
	10:8	SYSCLK_ FREQ[2:0]	100	SYSCLK Frequency 000 = 6.144 MHz (5.6448 MHz) 001 = 12.288 MHz (11.2896 MHz) 010 = 24.576 MHz (22.5792 MHz) 011 = 49.152 MHz (45.1584 MHz) 100 = 98.304 MHz (90.3168 MHz) All other codes are reserved The frequencies in brackets apply for 44.1 kHz–related sample rates only (i.e., SAMPLE_RATE_*n* = 01XXX).
	6	SYSCLK_ENA	0	SYSCLK Control 0 = Disabled 1 = Enabled SYSCLK should only be enabled if the selected clock source is available at the selected frequency. Clear this bit before stopping the reference clock or changing the frequency of the selected source. Note that the SYSCLK source and SYSCLK frequency can be changed using a single register write; this can be used to change the clock source without disabling SYSCLK.

R288 (0x0120) DSP_Clock_1	6	DSP_CLK_ENA	0	DSPCLK Control 0 = Disabled 1 = Enabled DSPCLK should only be enabled if the selected clock source is available at the selected frequency. Clear this bit before stopping the reference clock or changing the frequency of the selected source. Note that the DSPCLK source and DSPCLK frequency can be changed using a single register write; this can be used to change the clock source without disabling DSPCLK.
	3:0	DSP_CLK_ SRC[3:0]	0100	DSPCLK Source 0000 = MCLK1 0001 = MCLK2 0100 = FLL1 (x1.5) 0111 = FLL_AO (x3) 1000 = AIF1BCLK 1001 = AIF2BCLK 1010 = AIF3BCLK 1111 = FLL_AO All other codes are reserved

Correction to HPD_DACVAL Limit:

4.9.4.2 Measurement Output - Page 146

Version F1 (Before change)

The impedance measurement result is valid if 169 ≤ HPD_DACVAL ≤ 1019. (In case of any contradiction with the HPD_IMPEDANCE_RANGE description, the HPD_DACVAL validity takes precedence.)

Version F2 (After change)

The impedance measurement result is valid if 169 ≤ HPD_DACVAL ≤ 1017. (In case of any contradiction with the HPD_IMPEDANCE_RANGE description, the HPD_DACVAL validity takes precedence.)

Material Ordering Compliancy Update:

9 Ordering information - Page 278

Version F1 (Before change)

Table 9-1. Ordering Information

Product	Description	Package	Halogen Free	Pb Free	Grade	Temperature Range	Container	Order #
CS47L15	Smart Codec with Low-Power Audio DSP	70-ball WLCSP	Yes	Yes	Commercial	–40 to +85°C	Tape and Reel [1]	CS47L15–CWZR

1.Reel quantity = 6,000 units.

Version F2 (After change)

Table 9-1. Ordering Information

Product	Description	Package	RoHS Compliant	Grade	Temperature Range	Container	Order #
CS47L15	Smart Codec with Low-Power Audio DSP	70-ball WLCSP	Yes	Commercial	–40 to +85°C	Tape and Reel [1]	CS47L15–CWZR

1.Reel quantity = 6,000 units.

Reason for Change:

CS47L15 factory-blown OTP (One time programmable) registers have been updated to ensure robust operation of the master boot (Self-Boot) feature.
This change also has following impact if using this device in Slave-Boot mode.

- Change to DSP memory during software reset. Due to a change in the OTP, DSP memory will not be retained following a Software reset.

Process Change Notification

PCN Number: PCN-2019-114 **PCN Notification Date:** 03/08/2019

Anticipated Impact on Form, Fit, Function, Quality or Reliability:

No impact to form, fit, quality or reliability.
Impact to function as per the details described and outlined above.

Anticipated Impact on Material Declaration:

☒ No Impact to the Material Declaration

☐ Material Declarations or Product Content reports are driven from production data and will be available following the production release.

Product Affected:

Device	Cirrus Logic Part Number
CS47L15	CS47L15-CWZR

Changes To Product Identification Resulting From This PCN:

No marking changes, this is a datasheet only change and the data sheet will be revised accordingly.