VSC8512-02 Datasheet
12-Port 10/100/1000BASE-T PHY with SGMII and QSGMII MAC

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 4.4

Revision 4.4 of this datasheet was published in February 2019. In revision 4.4, VeriPHY descriptions were updated and VeriPHY register information was deleted. For functional details of the VeriPHY suite and operating instructions, see the ENT-AN0125 PHY, Integrated PHY-Switch VeriPHY - Cable Diagnostics application note.

1.2 Revision 4.3

Revision 4.3 of this datasheet was published in September 2014. In revision 4.3 of the document, the package drawing was updated to reflect two top views, which represent one of two packages customers can expect to receive. The maximum package height was changed to 2.44 mm. For more information, see Figure 40, page 125.

1.3 Revision 4.2

Revision 4.2 of this datasheet was published in May 2014. The following is a summary of the changes made to the datasheet:

- Information about the device SerDes MAC and the device media interface was updated. Neither the integrated SerDes media access controller (MAC) or the enhanced SerDes media interface of the device include internal AC-decoupling capacitors; external capacitors must be used.
- Information about AC-coupling, which is required when using a differential reference clock (REFCLK) input, was added.
- Information about the typical input impedance for a differential REFCLK signal (R_I) was added.
- The order of the information in the Pins by Function section was changed to match the alphabetical sort in the Pins spreadsheet attached to this document.
- "LED and Multipurpose Pins," in the Pins by Function section, was changed to "LED and Multi/General Purpose Input and Output Pins" to more accurately describe the functionality of the pins.
- The names of pins V3 and W3 were changed. The name of V3 was changed to PHY0_LED0/BASIC_SLED_DATA to accurately reflect its function as a source of basic serial LED data. The name of W3 was changed to PHY8_LED1/GPIO_13 to accurately reflect that it does not provide basic serial LED data.
- The description of the following pins was changed from "Reserved" to "No Connect": AA23, AA24, AA25, AA26, AB23, AB24, AB25, AB26, AC23, AC24, AC25, AC26, AD24, AD25, AD26, AE25, C5, R23, R24, R25, R26, T23, T24, T25, T26, U23, U24, U25, U26, V23, V24, V25, V26, W23, W24, W25, W26, Y23, Y24, Y25, Y26. This change does not effect the functionality of these pins or the device.
- Information about pin C18 was corrected. C18 must not be left floating/unconnected. It should be connected to VDD_IO for correct functioning of fiber media ports.

1.4 Revision 4.1

Revision 4.1 of this datasheet was published in January 2013. In revision 4.1 of the document, the VSC8512-03 part number was added to reflect the availability of a device with an extended operating temperature range of –40 °C ambient to 125 °C junction.

1.5 Revision 4.0

Revision 4.0 of this datasheet was published in October 2012. In revision 4.0 of the document, errata items, which were previously published in the VSC8512-02 Errata revision 1.0 as open issues, are now reconciled in the datasheet. Now that the information is available in the datasheet, the previously published errata document no longer applies, and it has been removed from the Microsemi Web site.

1.6 Revision 2.0

- Revision 2.0 of this datasheet was published in September 2012. This was the first publication of the document.

2 Introduction

This document consists of descriptions and specifications for both functional and physical aspects of the VSC8512-02 12-port 10/100/1000BASE-T PHY device with four dual media ports for the Ethernet market segment.

In addition to datasheets, the Microsemi Web site offers an extensive library of documentation, support files, and application materials specific to each device. The address of the Microsemi Web site is www.microsemi.com.

2.1 Register and Bit Conventions

This document refers to registers by their address and bit number in decimal notation. A range of bits is indicated with a colon. For example, a reference to address 26, bits 15 through 14 is shown as 26.15:14.

A register with an E and a number attached (example 27E1) means it is a register contained within extended register page number 1. A register with a G attached (example 13G) means it is a GPIO page register.

Bit numbering follows the IEEE standard with bit 15 being the most significant bit and bit 0 being the least significant bit.

3 Overview

The VSC8512-02 is a low-power 12-port Gigabit Ethernet transceiver with four SerDes interfaces for quad-port dual media capability. It also includes an integrated quad port I2C multiplexer (MUX) to control SFPs or PoE modules. It has a low electromagnetic interference (EMI) line driver and integrated line side termination resistors that conserve both power and printed circuit board (PCB) space.

Microsemi's mixed signal and digital signal processing (DSP) architecture is a key operational feature of the VSC8512-02, assuring robust performance even under less-than-favorable environmental conditions. It supports both half-duplex and full duplex 10BASE-T, 100BASE-TX, and 1000BASE-T communication speeds over Category 5 (Cat5) unshielded twisted pair (UTP) cable at distances greater than 100 m, displaying excellent tolerance to NEXT, FEXT, echo, and other types of ambient environmental and system electronic noise. This device also supports four dual media ports and can support up to four 100BASE-FX, 1000BASE-X, and/or triple-speed copper SFPs on ports 8 through 11 of the VSC8512-02.

The following illustrations show a high-level, general view of typical VSC8512-02 applications.

Figure 1 • **QSGMII Application Diagram**
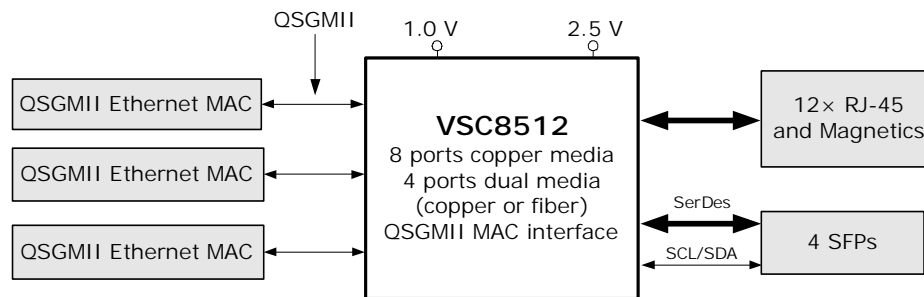
Figure 2 • **SGMII Application Diagram**
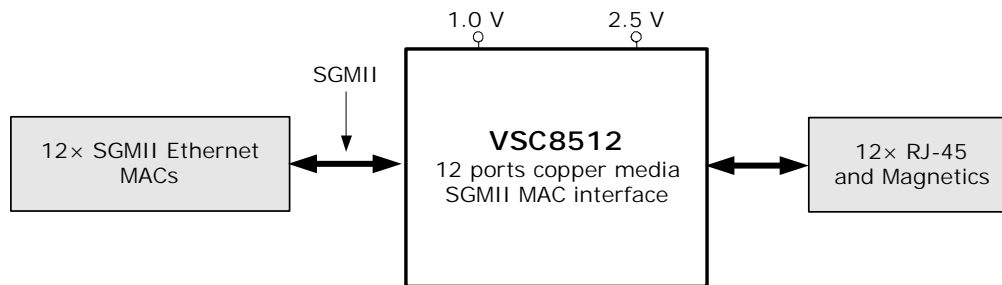
3.1   Key Features

This section lists the main features and benefits of the VSC8512-02 device.

Low Power

- Low power consumption of approximately 425 mW per port in 1000BASE-T mode, 200 mW per port in 100BASE-TX mode, 225 mW per port in 10BASE-T mode, and less than 115 mW per port in 100BASE-FX and 1000BASE-X modes
- ActiPHY™ link down power savings
- PerfectReach™ smart cable reach algorithm
- IEEE 802.3az Energy Efficient Ethernet idle power savings

Wide Range of Support

- Compliant with IEEE 802.3 (10BASE-T, 100BASE-TX, 1000BASE-T, 100BASE-FX, and 1000BASE-X) specifications
- Support for IEEE 802.3ah unidirectional transport for 100BASE-FX and 1000BASE-X fiber media
- Support for >16 kB jumbo frames in all speeds with programmable synchronization FIFOs
- Supports Cisco SGMII v1.9, Cisco QSGMII v1.3 and 1000BASE-X MACs, IEEE 1149.1 JTAG boundary scan, and IEEE 1149.6 AC-JTAG
- Support for applications that need to meet 2 kV CDE, IEC 61000-4-2 at 8 kV
- Available in a low-cost, 672-pin BGA package with a 27 mm × 27 mm body size for low-power, fanless applications

Flexibility

- VeriPHY® cable diagnostics suite provides extensive network cable operating conditions and status
- Patented, low EMI line driver with integrated line side termination resistors
- Two programmable direct-drive LEDs per port with adjustable brightness levels using register controls; bi-color LED support using both LED pins
- Serial LED interface option
- Extensive test features including near end, far end, copper media connector, SerDes MAC/media loopback, and Ethernet packet generator with CRC error counter to decrease time-to-market

3.2   Block Diagram

The following illustration shows the primary functional blocks of the VSC8512-02 device.

Figure 3 • **Block Diagram**

1. Pin shared with PHY4_LED1
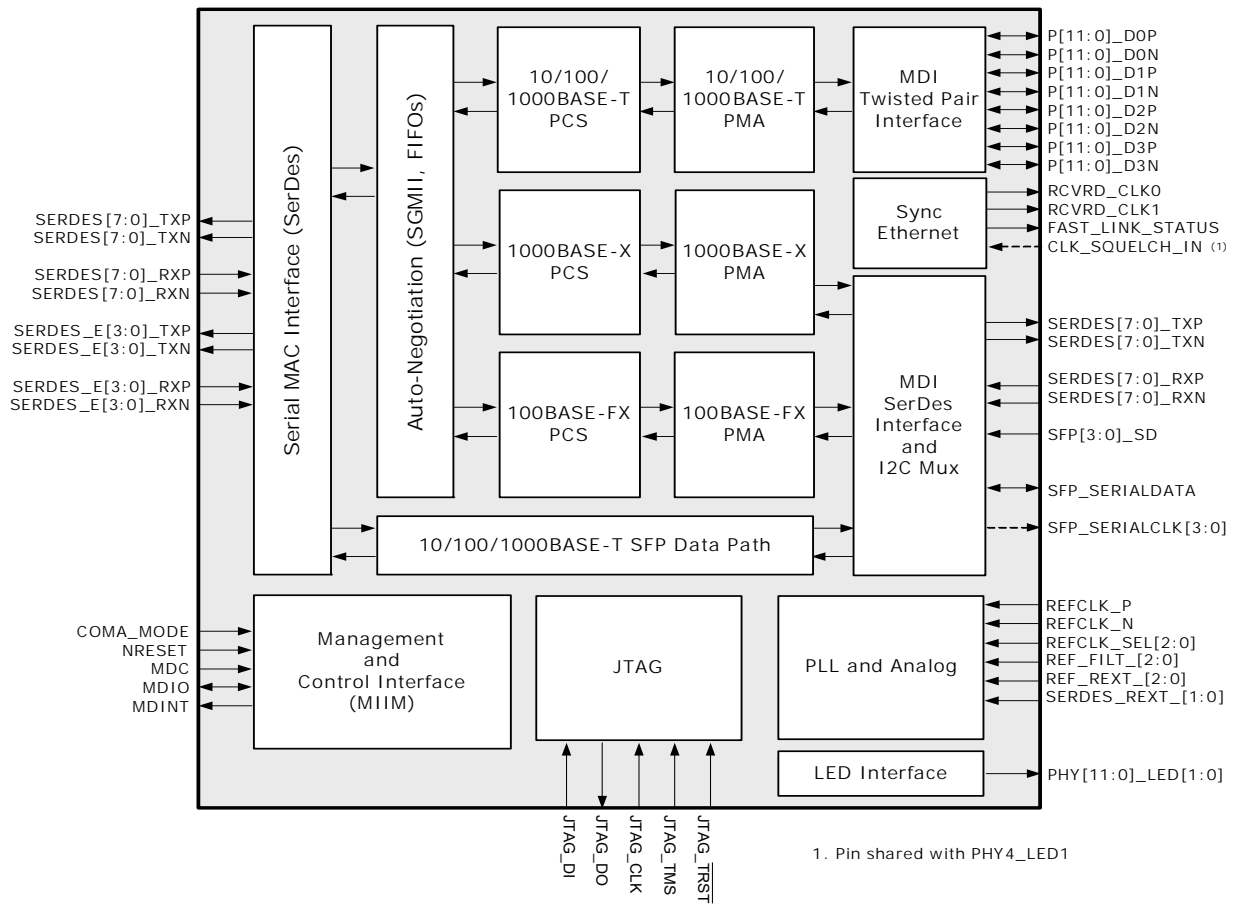
4 Functional Descriptions

This section provides detailed information about the functionality of the VSC8512-02 device, available configurations, operational features, and testing functionality. It includes descriptions of the various device interfaces and their configuration. With the information in this section, the device setup parameters can be determined for configuring the VSC8512-02 part for use in a particular application.

4.1 Operating Modes

The following table lists the operating modes of the VSC8512-02 device.

Table 1 • **Operating Modes**

Operating Mode	Supported Media	Notes
SerDes MAC-to-Cat5 Link Partner	1000BASE-T only	See Figure 2, page 4.
SGMII MAC-to-Cat5 Link Partner	10/100/1000BASE-T	See Figure 2, page 4.
QSGMII MAC-to-Cat5 Link Partner	10/100/1000BASE-T	See Figure 1, page 4.
QSGMII MAC-to-1000BASE-X Link Partner	1000BASE-X	See Figure 1, page 4. Ports 8–11 only.
QSGMII MAC-to-100BASE-FX Link Partner	100BASE-FX	See Figure 1, page 4. Ports 8–11 only.
QSGMII MAC-to-SGMII/1000BASE-X	SFP/Fiber (1000BASE-X, 10/100/1000BASE-T Cu SFP)	See Figure 1, page 4. Ports 8–11 only (SGMII/1000BASE-X protocol transfer).
QSGMII MAC-to-AMS and 1000BASE-X SerDes	1000BASE-X, 10/100/1000BASE-T	See Figure 1, page 4.
QSGMII MAC-to-AMS and 100BASE-FX SerDes	100BASE-FX, 10/100/1000BASE-T	See Figure 1, page 4.
QSGMII MAC-to-AMS and SGMII/1000BASE-X	SFP/Fiber (1000BASE-X, 10/100/1000BASE-T, 1000BASE-X, 10/100/1000BASE-T Cu SFP)	See Figure 1, page 4. SGMII/1000BASE-X protocol transfer on ports 8–11 when configured for SerDes media operation.

4.2 SerDes MAC Interface

The VSC8512-02 SerDes MAC interface performs data serialization and deserialization functions using an integrated SerDes block. The interface operates in the following modes: 1000BASE-X mode, SGMII mode, and QSGMII mode. The SerDes and Enhanced SerDes blocks include integrated termination resistors. Register 19G is a global register and only needs to be set once to configure the device. The other register bits are configured on a per-port basis and the operation either needs to be repeated for each port, or a broadcast write needs to be used by setting register 22, bit 0 to configure all the ports simultaneously.

4.2.1 SerDes MAC

When connected to a SerDes MAC compliant to 1000BASE-X, the VSC8512-02 device provides data throughput at a rate of 1000 Mbps only; 10 Mbps and 100 Mbps rates are not supported. To configure the device for SerDes MAC mode, set register 19G, bits 15:14 = 01, and register 23, bit 12 = 1. The device also supports 1000BASE-X Clause 37 MAC-side autonegotiation, and is enabled through register 16E3,

bit 7. To configure the rest of the device for 1000 Mbps only operation, select 1000BASE-T only by disabling the 10BASE-T/100BASE-TX advertisements in register 4.

Figure 4 • **SerDes MAC Interface**
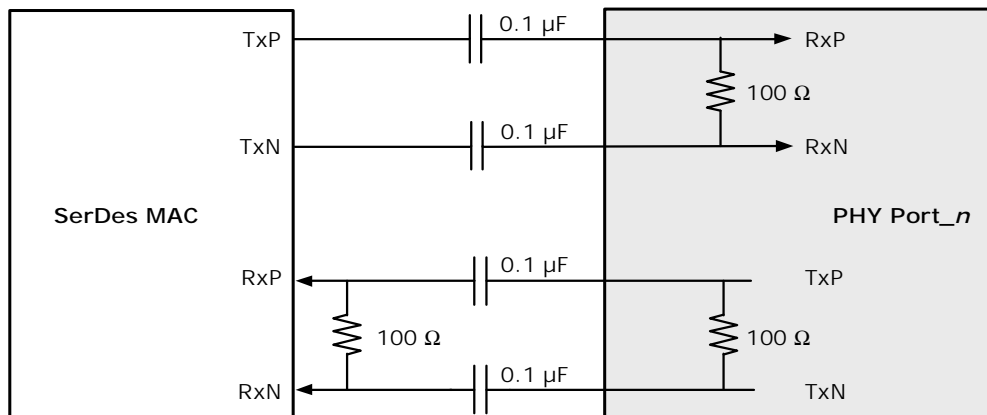
4.2.2 SGMII MAC

When configured to detect and switch between 10BASE-T, 100BASE-T, and 1000BASE-T data rates, the VSC8512-02 device can be connected to an SGMII-compatible MAC. To configure the device for SGMII MAC mode, set register 19G, bits 15:14 = 01 and register 23, bit 12 = 0. This device also supports SGMII MAC-side autonegotiation and is enabled through register 16E3, bit 7.

Figure 5 • **SGMII MAC Interface**
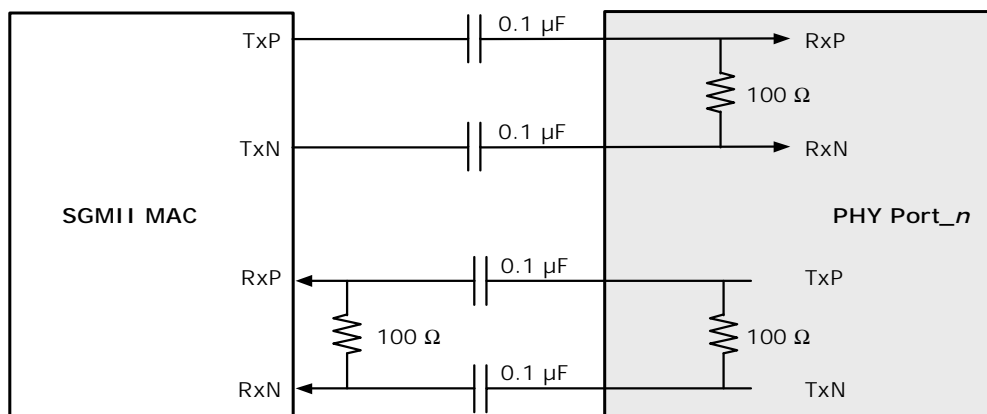
4.2.3 QSGMII MAC

The VSC8512-02 device supports a QSGMII MAC to convey four ports of network data and port speed between 10BASE-T, 100BASE-T, and 1000BASE-T data rates and operates in both half-duplex and full-duplex at all port speeds. The MAC interface protocol for each port within QSGMII can either be 1000BASE-X or SGMII, if the QSGMII MAC that the VSC8512-02 is connecting to supports this functionality. To configure the device for QSGMII MAC mode, set register 19G, bits 15:14 = 00 or 10. This device also supports SGMII MAC-side autonegotiation on each individual port and is enabled through register 16E3, bit 7, of that port.

Figure 6 • **QSGMII MAC Interface**
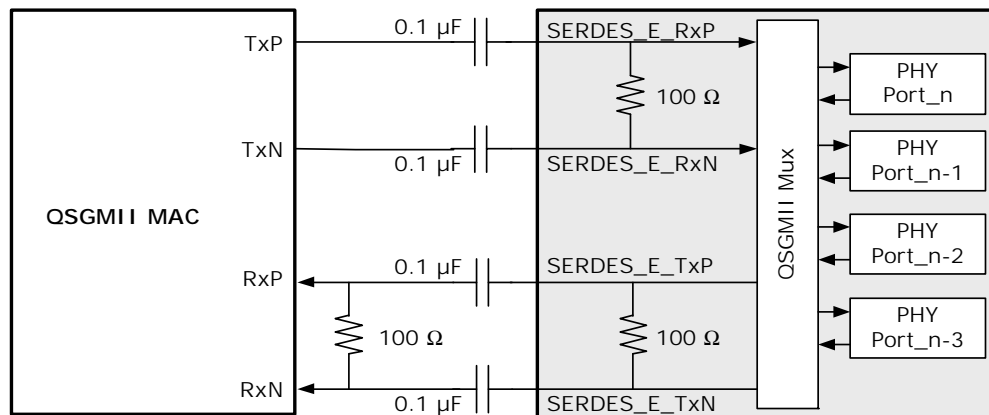
4.3 SerDes Media Interface

The VSC8512-02 device SerDes media interface performs data serialization and deserialization functions using an integrated SerDes block in the SerDes media interface. The interface operates at 1.25 Gbps speed, providing full-duplex and half-duplex for 10/100/1000 Mbps bandwidth that can connect directly to 100BASE-FX/1000BASE-X-compliant optical devices as well as to 10/100/1000BASE-T copper SFP devices. The interface also provides support for unidirectional transport as defined in IEEE 802.3-2008, Clause 66. The interface has the following SerDes operating modes:

- QSGMII to 1000BASE-X
- QSGMII to 100BASE-FX
- QSGMII to SGMII/1000BASE-X SGMII/1000BASE-X protocol transfer

The SerDes media block includes an integrated termination resistor.

A software reset through register 0, bit 15 is required when changing operating modes between 100BASE-FX and 1000BASE-X.

4.3.1 QSGMII to 1000BASE-X

The 1000BASE-X SerDes media in QSGMII mode supports IEEE 802.3 Clause 36 and Clause 37, which describe 1000BASE-X fiber autonegotiation. In this mode, control and status of the SerDes media is displayed in the VSC8512-02 device registers 0 through 15 in a manner similar to what is described in IEEE 802.3 Clause 28. In this mode, connected copper SFPs can only operate at 1000BASE-T speed. A link in this mode is established using autonegotiation (enabled or disabled) between the PHY and the link partner. To configure the PHY in this mode, set register 23, bits 10:8 = 010. To configure 1000BASE-X autonegotiation for this mode, set register 0, bit 12. Setting this mode and configurations can be performed individually on each of the four ports. Ethernet packet generator (EPG), cyclical redundancy check (CRC) counters, and loopback modes are supported in 1000BASE-X mode.

4.3.2 QSGMII to 100BASE-FX

The VSC8512-02 supports 100BASE-FX communication speed for connecting to fiber modules such as GBICs and SFPs. This capability is facilitated by using the connections on the SerDes pins when connected to a MAC through QSGMII only. Ethernet packet generator (EPG), cyclical redundancy check (CRC) counters, and loopback modes are supported in the 100BASE-FX mode. Setting this mode and configurations can be performed individually on each of the four ports. To configure the PHY in this mode, set register 23, bits 10:8 = 011.

4.3.3 QSGMII to SGMII Protocol Conversion

QSGMII to SGMII (protocol transfer) mode is a feature that links a fiber module or triple speed 10/100/1000-T copper SFP to the QSGMII MAC through the VSC8512-02 device. SGMII can be converted to QSGMII with protocol conversion using this mode.

To configure the PHY in this mode, set register 23, bits 10:8 = 001. To establish the link, assert the SFP[3:0]_SD pins.

All relevant LED modes are supported except for collision, duplex, and autonegotiation fault. The triple-speed copper SFP's link status and data type plugged into the port can be indicated by the PHY's LEDs. Setting this particular mode and configuration can be performed individually on each of the four ports within a QSGMII grouping.

4.3.4 Unidirectional Transport for Fiber Media

The VSC8512-02 device supports 802.3ah for unidirectional transport across its 1000BASE-X and 100BASE-FX fiber media. This feature enables transmission across fiber media, regardless of whether the PHY has determined that a valid link has been established (register 1, bit 2). The only valid operating modes for unidirectional fiber mode are 100BASE-FX or 1000BASE-X fiber media.

To enable this feature, set register 0, bit 5 to 1. For status of the unidirectional ability, read register 1, bit 7.

Note: Automatic media-sensing does not work with this feature. In addition, because unidirectional fiber media must have autonegotiation disabled, SGMII autonegotiation must also be disabled (register 16E3, bit 7 = 0).

4.4 PHY Addressing and Port Mapping

This section contains information about PHY addressing and port mapping.

4.4.1 PHY Addressing

The VSC8512-02 includes two external PHY address pins to allow control of multiple PHY devices on a system board that are sharing a common management bus. Based on the settings of these two address control pins, the internal PHYs in the VSC8512-02 device take on the address ranges as shown in the following table.

Table 2 •   **PHY Address Range Selection**

PHYADD4	PHYADD3	Internal PHY Addresses
0	0	0–11
0	1	12–23
1	0	4–15
1	1	20–31

4.4.2 SerDes Port Mapping

The VSC8512-02 includes eight 1.25 GHz SerDes macros and four 5 GHz enhanced SerDes macros. Depending on the configuration, some of the SerDes macros are configured as either 1000BASE-X/100BASE-FX SerDes media interfaces or SGMII MAC interfaces. Also, based on configuration, the enhanced SerDes macros are configured as either QSGMII MAC interfaces or SGMII MAC interfaces. The following table shows the different operating modes based on the settings of register 19G, bits 15:14.

Table 3 •   **Operating Modes**

Mode	19G[15:14]	Operating Mode
Mode 0	00	QSGMII to CAT5 mode
Mode 1	01	SGMII to CAT5 mode
Mode 2	10	QSGMII to CAT5 and fiber media mode

The following table shows the SerDes port mapping in the modes of operation shown in the previous table.

Table 4 • **SerDes Port Mapping**

Interface Pins	Mode 0	Mode 1	Mode 2
SERDES_E0_TXP, SERDES_E0_TXN		SGMII0	
SERDES_E0_RXP, SERDES_E0_RXN		SGMII0	
SERDES_E1_TXP, SERDES_E1_TXN	QSGMII0	SGMII3	QSGMII0
SERDES_E1_RXP, SERDES_E1_RXN	QSGMII0	SGMII3	QSGMII0
SERDES_E2_TXP, SERDES_E2_TXN	QSGMII1	SGMII6	QSGMII1
SERDES_E2_RXP, SERDES_E2_RXN	QSGMII1	SGMII6	QSGMII1
SERDES_E3_TXP, SERDES_E3_TXN	QSGMII2	SGMII9	QSGMII2
SERDES_E3_RXP, SERDES_E3_RXN	QSGMII2	SGMII9	QSGMII2
SERDES0_TXP, SERDES0_TXN		SGMII1	
SERDES0_RXP, SERDES0_RXN		SGMII1	
SERDES1_TXP, SERDES1_TXN		SGMII2	
SERDES1_RXP, SERDES1_RXN		SGMII2	
SERDES2_TXP, SERDES2_TXN		SGMII4	
SERDES2_RXP, SERDES2_RXN		SGMII4	
SERDES3_TXP, SERDES3_TXN		SGMII5	
SERDES3_RXP, SERDES3_RXN		SGMII5	
SERDES4_TXP, SERDES4_TXN		SGMII7	FIBER11
SERDES4_RXP, SERDES4_RXN		SGMII7	FIBER11
SERDES5_TXP, SERDES5_TXN		SGMII8	FIBER10
SERDES5_RXP, SERDES5_RXN		SGMII8	FIBER10
SERDES6_TXP, SERDES6_TXN		SGMII10	FIBER9
SERDES6_RXP, SERDES6_RXN		SGMII10	FIBER9
SERDES7_TXP, SERDES7_TXN		SGMII11	FIBER8
SERDES7_RXP, SERDES7_RXN		SGMII11	FIBER8

4.5　Cat5 Twisted Pair Media Interface

The VSC8512-02 twisted pair interface is compliant with IEEE 802.3-2008 and the IEEE 802.3az standard for Energy Efficient Ethernet.

4.5.1　Voltage-Mode Line Driver

Unlike many other gigabit PHYs, the VSC8512-02 uses a patented voltage-mode line driver that allows it to fully integrate the series termination resistors, which are required to connect the PHY's Cat5 interface to an external 1:1 transformer. Also, the interface does not require the user to place an external voltage on the center tap of the magnetic. The following illustration shows the connections.

Figure 7 • **Cat5 Media Interface**
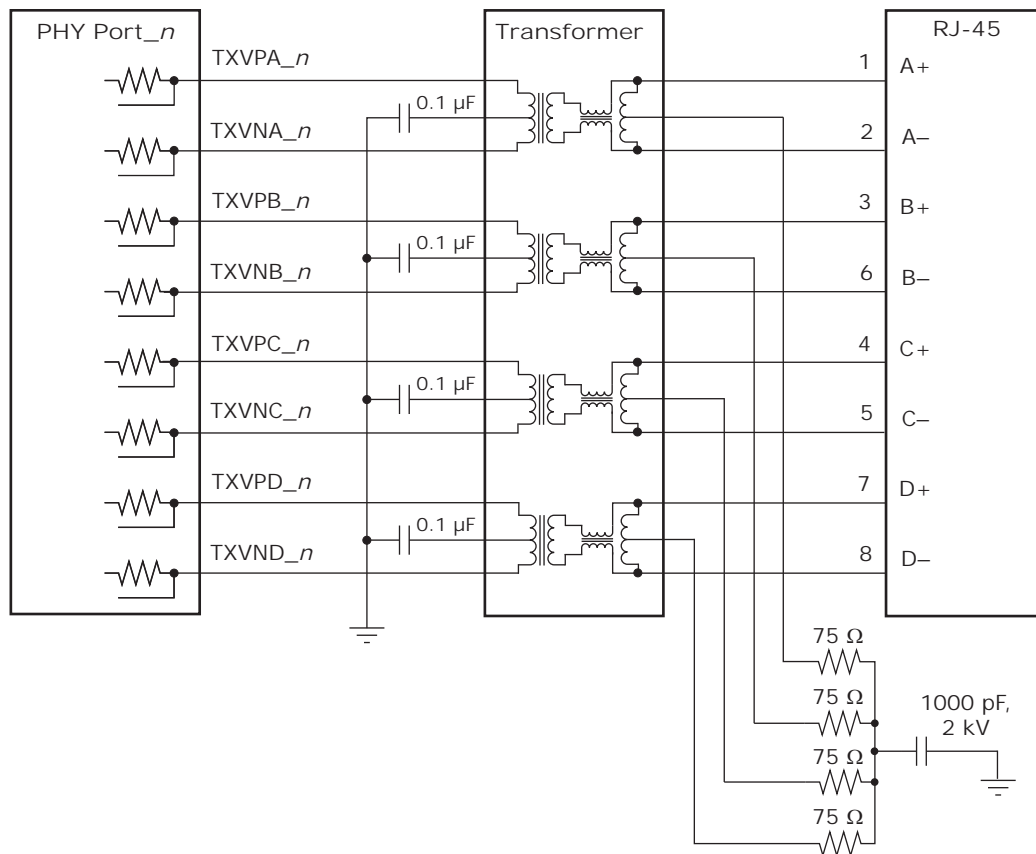
4.5.2 Cat5 Autonegotiation and Parallel Detection

The VSC8512-02 supports twisted pair autonegotiation, as defined by IEEE 802.3-2008 Clause 28 and IEEE 802.3az. The autonegotiation process evaluates the advertised capabilities of the local PHY and its link partner to determine the best possible operating mode. In particular, autonegotiation can determine speed, duplex configuration, and master or slave operating modes for 1000BASE-TX. Autonegotiation also enables a connected MAC to communicate with its link partner MAC through the VSC8512-02 using optional next pages, which set attributes that may not otherwise be defined by the IEEE standard.

If the Cat5 link partner does not support autonegotiation, the VSC8512-02 automatically uses parallel detection to select the appropriate link speed.

Autonegotiation is disabled by clearing register 0, bit 12. If autonegotiation is disabled, the state of register bits 0.6, 0.13, and 0.8 determine the device operating speed and duplex mode. Note that while 10BASE-T and 100BASE-T do not require autonegotiation, Clause 40 has defined 1000BASE-T to require autonegotiation.

4.5.3 1000BASE-T Forced Mode Support

VSC8512-02 provides support for a 1000BASE-T forced test mode. In this mode, the PHY can be forced into 1000BASE-T mode and does not require manual setting of master/slave at the two ends of the link. This mode is for test purposes only, and should not be used in normal operation. To configure a PHY in this mode, set register 17E2, bit 5 = 1 and register 0, bits 6 and 13 = 10.

4.5.4 Automatic Crossover and Polarity Detection

For trouble-free configuration and management of Ethernet links, the VSC8512-02 includes a robust automatic crossover detection feature for all three speeds on the twisted-pair interface (10BASE-T, 100BASE-T, and 1000BASE-T). Known as HP Auto-MDIX, the function is fully compliant with Clause 40 of IEEE 802.3-2008.

Additionally, the device detects and corrects polarity errors on all MDI pairs — a useful capability that exceeds the requirements of the standard.

Both HP Auto-MDIX detection and polarity correction are enabled in the device by default. Default settings can be changed using device register bits 18.5:4. Status bits for each of these functions are located in register 28.

Note: The VSC8512-02 can be configured to perform HP Auto-MDIX, even when autonegotiation is disabled and the link is forced into 10/100 speeds. To enable this feature, set register 18.7 to 0. To disable the feature, set register 0.12 to 0.

The HP Auto-MDIX algorithm successfully detects, corrects, and operates with any of the MDI wiring pair combinations listed in the following table.

Table 5 •   **Supported MDI Pair Combinations**

1, 2	3, 6	4, 5	7, 8	Mode
A	B	C	D	Normal MDI
B	A	D	C	Normal MDI-X
A	B	D	C	Normal MDI with pair swap on C and D pair
B	A	C	D	Normal MDI-X with pair swap on C and D pair

4.5.5   Manual HP Auto-MDIX Setting

As an alternative to HP Auto-MDIX detection, the PHY can be forced to be MDI or MDI-X using register 19E1, bits 3:2. Setting these bits to 10 forces MDI and setting 11 forces MDI-X. Leaving the bits 00 enables the HP Auto-MDIX setting to be based on register 18, bits 7 and 5.

4.5.6   Link Speed Downshift

For operation in cabling environments that are incompatible with 1000BASE-T, the VSC8512-02 provides an automatic link speed downshift option. When enabled, the device automatically changes its 1000BASE-T autonegotiation advertisement to the next slower speed after a set number of failed attempts at 1000BASE-T. No reset is required to get out of this state if a subsequent link partner with 1000BASE-T support is connected. This feature is useful in setting up in networks using older cable installations that include only pairs A and B, and not pairs C and D.

To configure and monitor link speed downshifting, set register 20E1, bits 4:1. For more information, see

4.5.7   Energy Efficient Ethernet

The VSC8512-02 supports the IEEE 802.3az Energy Efficient Ethernet standard that is currently in development. This new standard provides a method for reducing power consumption on an Ethernet link during times of low utilization. It uses low power idles (LPI) to achieve this objective.

Figure 8 •   **Low Power Idle Operation**
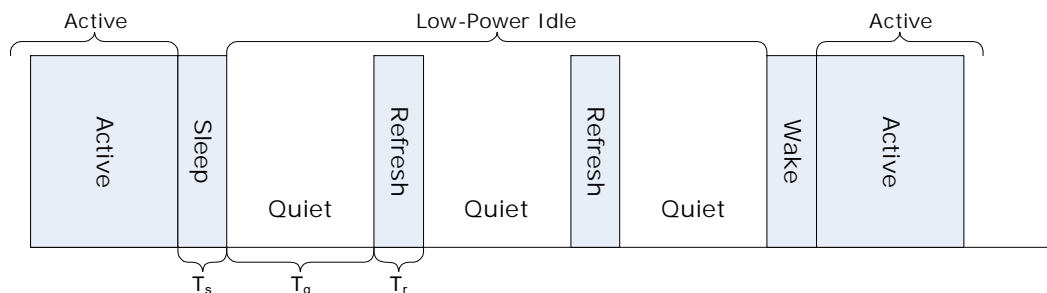
Using LPI, the usage model for the link is to transmit data as fast as possible and then return to a low power idle state. Energy is saved on the link by cycling between active and low power idle states. During

LPI, power is reduced by turning off unused circuits and using this method, energy use scales with bandwidth utilization.

The VSC8512-02 uses LPI to optimize power dissipation in 100BASE-TX and 1000BASE-T modes of operation. In addition, the IEEE 802.3az standard defines a 10BASE-Te mode that reduces transmit signal amplitude from 5 V_{p-p} to ~3.3 V_{p-p}. This mode reduces power consumption in 10 Mbps link speed and fully interoperates with legacy 10BASE-T compliant PHYs over 100 m Cat5 cable or better.

To configure the VSC8512-02 in 10BASE-Te mode, set register 17E2.15 to 1 for each port. Additional Energy Efficient Ethernet features are controlled through Clause 45 registers. For more information, see Clause 45 Registers to Support Energy Efficient Ethernet, page 77.

4.6   Automatic Media-Sense Interface Mode

Automatic media-sense (AMS) mode automatically sets the media interface to Cat5 mode or SerDes mode. The active media mode chosen is based on the automatic media-sense preferences set in the device register 23, bit 11. The following illustration shows a block diagram of AMS functionality on ports 8 through 11 of the VSC8512-02 device.

Figure 9 •   **Automatic Media-Sense Block Diagram**
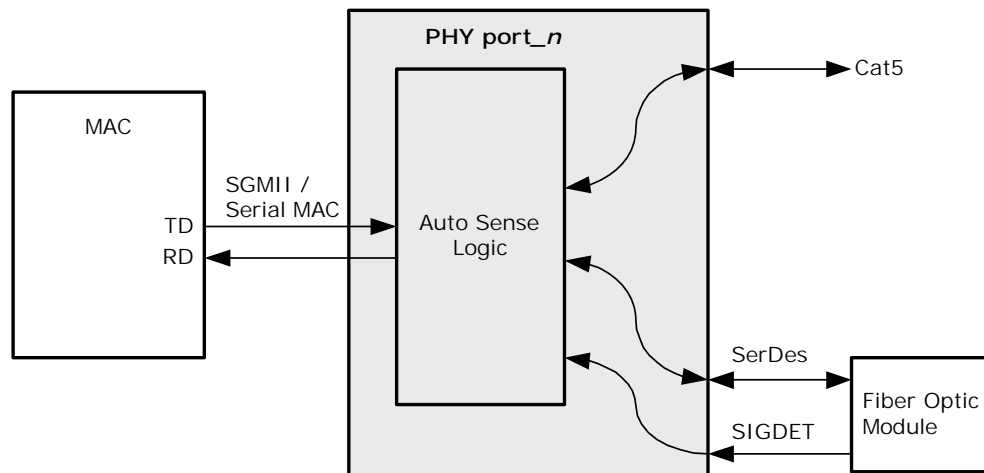
When both SerDes and Cat5 media interfaces attempt to establish a link, the preferred media interface overrides a link-up of the non-preferred media interface. For example, if the preference is set for SerDes mode and Cat5 media establishes a link, then Cat5 becomes the active media interface. However, after the SerDes media interface establishes a link, the Cat5 interface drops its link because the preference was set for SerDes mode. In this scenario, the SerDes preference determines the active media source until the SerDes link is lost. Also, Cat5 media cannot link up unless there is no SerDes media link established. The following table shows the possible link conditions based on preference settings.

Table 6 •   **AMS Media Preferences**

Preference Setting	Cat5 Linked, Fiber Not Linked	SerDes Linked, Cat5 Not Linked	Cat5 Linked, SerDes Attempts to Link	SerDes Linked, Cat5 Attempts to Link	Both Cat5 and SerDes Attempt to Link
SerDes	Cat5	SerDes	SerDes	SerDes	SerDes
Cat5	Cat5	SerDes	Cat5	Cat5	Cat5

The status of the media mode selected by the AMS can be read from device register 20E1, bits 7:6. It indicates whether copper media, SerDes media, or no media is selected. Each PHY has four automatic media-sense modes. The difference between the modes is based on the SerDes media modes:

*   QSGMII MAC to AMS and 1000BASE-X SerDes
*   QSGMII MAC to AMS and 100BASE-FX SerDes
*   QSGMII MAC to AMS and SGMII (protocol transfer)

For more information about SerDes media mode functionality with AMS enabled, see SerDes Media Interface, page 9.

4.7 Reference Clock

The device reference clock can be a 25 MHz, 125 MHz, or 156.25 MHz clock signal. It can be either a differential reference clock or a single-ended clock. However, 25 MHz single-ended operation is not recommended when using QSGMII due to the jitter specification requirements of this interface. For more information, see Reference Clock, page 80.

4.7.1 Configuring the REFCLK

There are three REFCLK_SEL pins to configure the REFCLK speed. The following table shows the functionality and associated REFCLK frequency.

Table 7 • **REFCLK Frequency Selection**

REFCLK_SEL2	REFCLK_SEL1	REFCLK_SEL0	REFCLK Frequency
0	0	0	125 MHz
0	0	1	156.25 MHz
1	0	0	25 MHz

4.7.2 Single-Ended REFCLK Input

To use a single-ended REFCLK, an external resistor network is required. The purpose of the network is to limit the amplitude and to adjust the center of the swing. The configurations for a single-ended REFCLK are shown in the following illustrations.

Figure 10 • **2.5 V CMOS Single-Ended REFCLK Input Resistor Network**
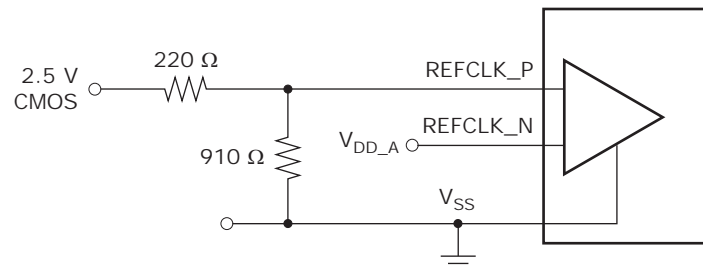
Figure 11 • **3.3 V CMOS Single-Ended REFCLK Input Resistor Network**
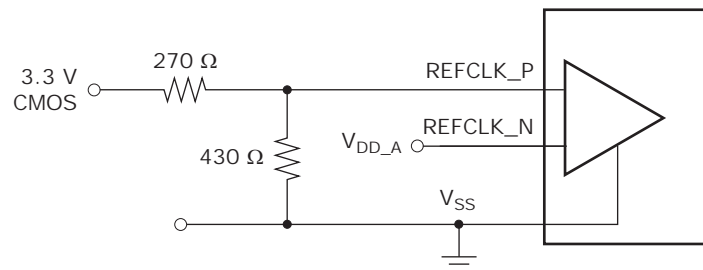
4.7.3 Differential REFCLK Input

AC-coupling is required when using a differential REFCLK. Differential clocks must be capacitively coupled and LVDS-compliant. The following illustration shows the configuration.

Figure 12 • **AC-Coupling Required for REFCLK Input**
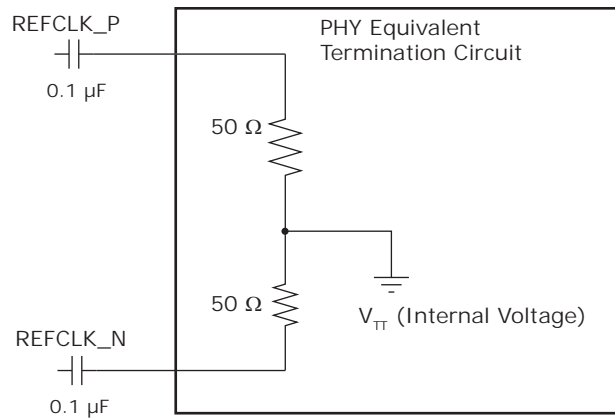
4.8 Ethernet Inline Powered Devices

The VSC8512-02 can detect legacy inline powered devices in Ethernet network applications. Inline powered detection capability is useful in systems that enable IP phones and other devices (such as wireless access points) to receive power directly from their Ethernet cable, similar to office digital phones receiving power from a private branch exchange (PBX) office switch over telephone cabling. This type of setup eliminates the need for an external power supply and enables the inline powered device to remain active during a power outage, assuming that the Ethernet switch is connected to an uninterrupted power supply, battery, back-up power generator, or other uninterruptable power source.

For more information about legacy inline powered device detection, visit the Cisco Web site at www.cisco.com. The following illustration shows an example of an inline powered Ethernet switch application.

Figure 13 • **Inline Powered Ethernet Switch Diagram**
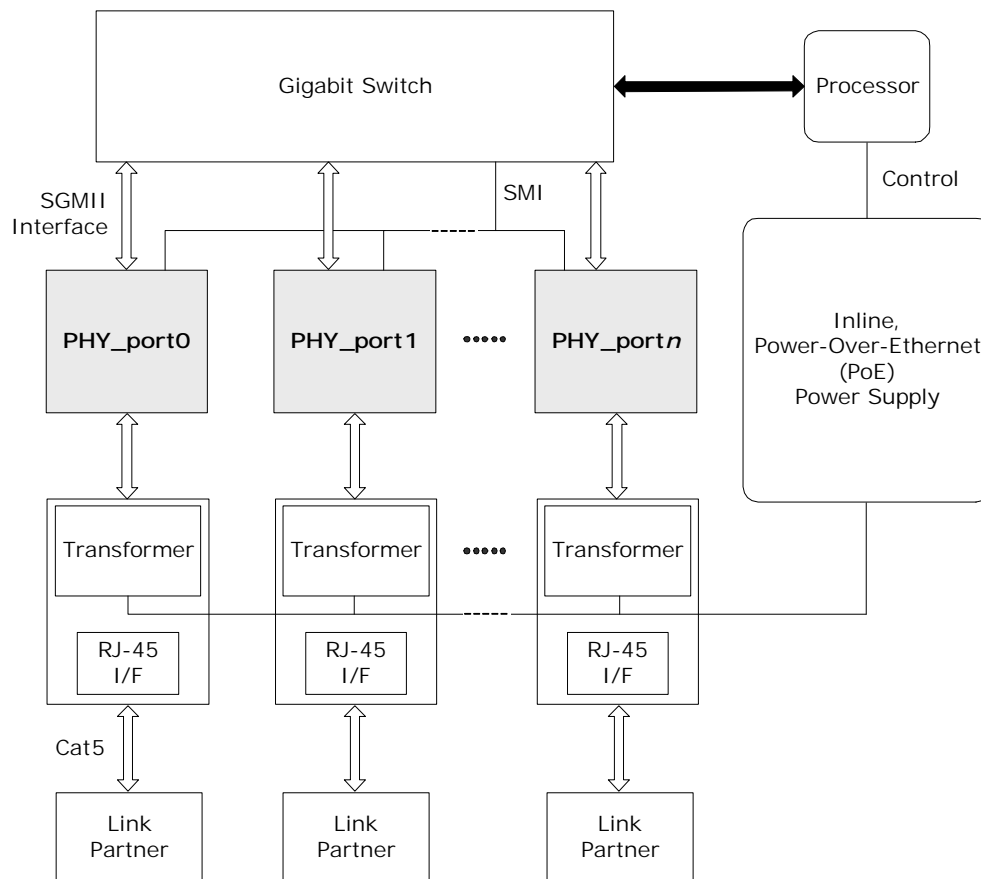
The following procedure describes the process that an Ethernet switch must perform to process inline power requests made by a link partner (LP) that is, in turn, capable of receiving inline power:

1. Enable the inline powered device detection mode on each VSC8512-02 PHY using its serial management interface. Set register bit 23E1.10 to 1.
2. Ensure that the VSC8512-02 autonegotiation enable bit (register 0.12) is also set to 1. In the application, the device sends a special fast link pulse (FLP) signal to the LP. Reading register bit 23E1.9:8 returns 00 during the search for devices that require power over Ethernet (PoE).
3. The VSC8512-02 PHY monitors its inputs for the FLP signal looped back by the LP. An LP capable of receiving PoE loops back the FLP pulses when the LP is in a powered down state. This is reported when VSC8512-02 register bit 23E1.9:8 reads back 01. It can also be verified as an inline power detection interrupt by reading VSC8512-02 register bit 26.9, which should be a 1, and which is subsequently cleared and the interrupt de-asserted after the read. If an LP device does not loop back the FLP after a specific time, VSC8512-02 register bit 23E1.9:8 automatically resets to 10.
4. If the VSC8512-02 PHY reports that the LP requires PoE, the Ethernet switch must enable inline power on this port, externally of the PHY.
5. The PHY automatically disables inline powered device detection if the VSC8512-02 register bits 23E1.9:8 automatically resets to 10, and then automatically changes to its normal autonegotiation process. A link is then auto-negotiated and established when the link status bit is set (register bit 1.2 is set to 1).
6. In the event of a link failure (indicated when VSC8512-02 register bit 1.2 reads 0), the inline power should be disabled to the inline powered device external to the PHY. The VSC8512-02 PHY disables its normal autonegotiation process and re-enables its inline powered device detection mode.

4.9 IEEE 802.3af PoE Support

The VSC8512-02 is compatible with switch designs that are intended for use in systems that supply power to data terminal equipment (DTE) by means of the MDI or twisted pair cable, as described in IEEE 802.3af Clause 33.

4.10 ActiPHY Power Management

In addition to the IEEE-specified power-down control bit (device register bit 0.11), the device also includes an ActiPHY power management mode for each PHY. This mode enables support for power-sensitive applications. It utilizes a signal-detect function that monitors the media interface for the presence of a link to determine when to automatically power-down the PHY. The PHY wakes up at a programmable interval and attempts to wake up the link partner PHY by sending a burst of FLP over copper media.

The ActiPHY power management mode in the VSC8512-02 is enabled on a per-port basis during normal operation at any time by setting register bit 28.6 to 1.

The following operating states are possible when ActiPHY mode is enabled:

- Low power state
- LP wake-up state
- Normal operating state (link-up state)

The VSC8512-02 switches between the low power state and LP wake-up state at a programmable rate (the default is two seconds) until signal energy has been detected on the media interface pins. When signal energy is detected, the PHY enters the normal operating state. If the PHY is in its normal operating state and the link fails, the PHY returns to the low power state after the expiration of the link status time-out timer. After reset, the PHY enters the low power state.

When autonegotiation is enabled in the PHY, the ActiPHY state machine operates as described. If autonegotiation is disabled and the link is forced to use 10BASE-T or 100BASE-TX modes while the PHY is in its low power state, the PHY continues to transition between the low power and LP wake-up states until signal energy is detected on the media pins. At that time, the PHY transitions to the normal operating state and stays in that state even when the link is dropped. If autonegotiation is disabled while the PHY is in the normal operation state, the PHY stays in that state when the link is dropped and does not transition back to the low power state.

The following illustration shows the relationship between ActiPHY states and timers.

Figure 14 • **ActiPHY State Diagram**
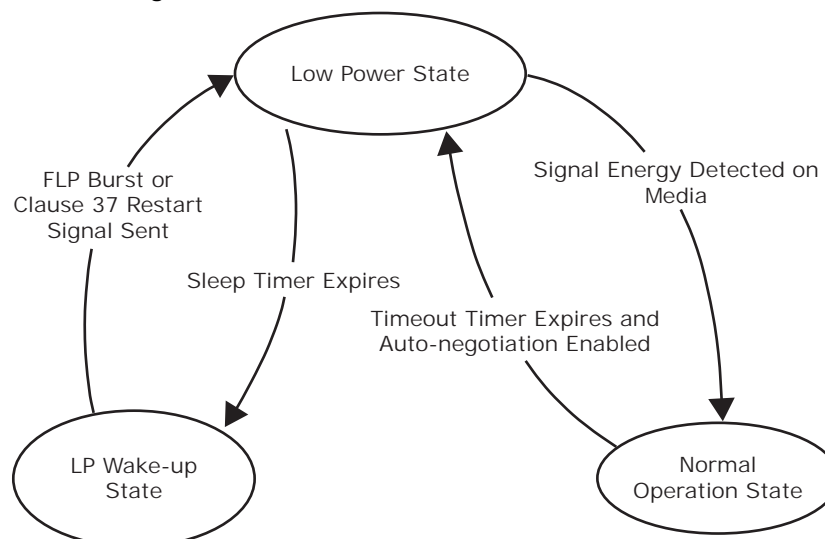
4.10.1 Low Power State

In the low power state, all major digital blocks are powered down. However, the following functionality is provided:

- SMI interface (MDC, MDIO, and MDINT pins)
- CLKOUT

In this state, the PHY monitors the media interface pins for signal energy. The PHY comes out of low power state and transitions to the normal operating state when signal energy is detected on the media. This happens when the PHY is connected to one of the following:

- Autonegotiation-capable link partner
- Another PHY in enhanced ActiPHY LP wake-up state

In the absence of signal energy on the media pins, the PHY periodically transitions from low-power state to LP wake-up state, based on the programmable sleep timer (register bits 20E1.14:13). The actual sleep time duration is randomized from –80 ms to 60 ms to avoid two linked PHYs in ActiPHY mode entering a lock-up state during operation.

4.10.2 Link Partner Wake-Up State

In the link partner wake-up state, the PHY attempts to wake up the link partner. Up to three complete FLP bursts are sent on alternating pairs A and B of the Cat5 media for a duration based on the wake-up timer, which is set using register bits 20E1.12:11.

In this state, the following functionality is provided:

- SMI interface (MDC, MDIO, and MDINT pins)
- CLKOUT

After sending signal energy on the relevant media, the PHY returns to the low power state.

4.10.3 Normal Operating State

In the normal operating state, the PHY establishes a link with a link partner. When the media is unplugged or the link partner is powered down, the PHY waits for the duration of the programmable link status time-out timer, which is set using register bit 28.7 and bit 28.2. It then enters the low power state.

4.11 Media Recovered Clock Outputs

For Synchronous Ethernet applications, the VSC8512-02 includes two recovered clock output pins, RCVRD_CLK0 and RCVRD_CLK1, that are controlled by registers 23G and 24G, respectively. These pins are synchronized to the clock of the active media link.

To enable recovered clock output, set register 23G or 24G, bit 15, to 1. By default, the recovered clock output pins are disabled and held low, including when NRESET is asserted. Registers 23G and 24G also control the PHY port for clock output, the clock source, the clock frequency (either 25 MHz or 125 MHz), and squelch conditions.

4.11.1 Clock Selection Settings

On each pin, the recovered clock supports the following sources, as set by registers 23G or 24G, bits 2:0:

- Fiber SerDes media
- Copper media
- Copper transmitter TCLK output (RCVRD_CLK0 only)

Note: When using the automatic media-sense feature, the recovered clock output cannot automatically change between each active media. Changing the media source must be managed through the recovered clock register settings.

Note: The 10BASE-T mode and 1000BASE-T master mode are not effective for Synchronous Ethernet clock recovery. For 10BASE-T mode, the receiver does not produce a reliable continuous clock source. For 1000BASE-T master mode, the clock is based on the VSC8512-02 REFCLK input, which is a local clock.

4.11.2 Clock Output Squelch

Under certain conditions, the PHY outputs a clock based on the REFCLK pin, such as when there is no link present or during autonegotiation. To prevent an undesirable clock from appearing on the recovered clock pins, the VSC8512-02 squelches, or inhibits, the clock output based on any of the following criteria:

- No link is detected (the link status register 1, bit 2 = 0).
- The link is found to be unstable using the fast link failure detection feature (FAST_LINK_STATUS pin is asserted high when enabled).
- The active link is in 10BASE-T or in 1000BASE-T master mode. These modes produce unreliable recovered clock sources.
- CLK_SQUELCH_IN is enabled to squelch the clock.

Use registers 23G or 24G, bits 5:4 to configure the clock squelch criteria. These registers can also disable the squelch feature. The CLK_SQUELCH_IN pin functionality is controlled by register bit 14G.14. When this bit is set to 1, the CLK_SQUELCH_IN pin also controls the squelching of the clock. When enabled, both RCVRD_CLK0 and RCVRD_CLK1 are squelched when the CLK_SQUELCH_IN pin is high.

4.12 Serial Management Interface

The VSC8512-02 device includes an IEEE 802.3-compliant serial management interface (SMI) that is affected by use of its MDC and MDIO pins. The SMI provides access to device control and status registers. The register set that controls the SMI consists of 32 16-bit registers, including all required IEEE-specified registers. Also, there are additional pages of registers accessible using device register 31.

Energy Efficient Ethernet control registers are available through the SMI using Clause 45 registers and Clause 22 register access in registers 13 through 14. For more information, see Table 27, page 46 and Table 86, page 77.

The SMI is a synchronous serial interface with input data to the VSC8512-02 on the MDIO pin that is clocked on the rising edge of the MDC pin. The output data is sent on the MDIO pin on the rising edge of the MDC signal. The interface can be clocked at a rate from 0 MHz to 12.5 MHz, depending on the total load on MDIO. An external 2-kΩ pull-up resistor is required on the MDIO pin.

4.12.1 SMI Frames

Data is transferred over the SMI using 32-bit frames with an optional, arbitrary-length preamble. Before the first frame can be sent, at least two clock pulses on MDC must be provided with the MDIO signal at logic one to initialize the SMI state machine. The following illustrations show the SMI frame format for read and write operations.

Figure 15 • **SMI Read Frame**
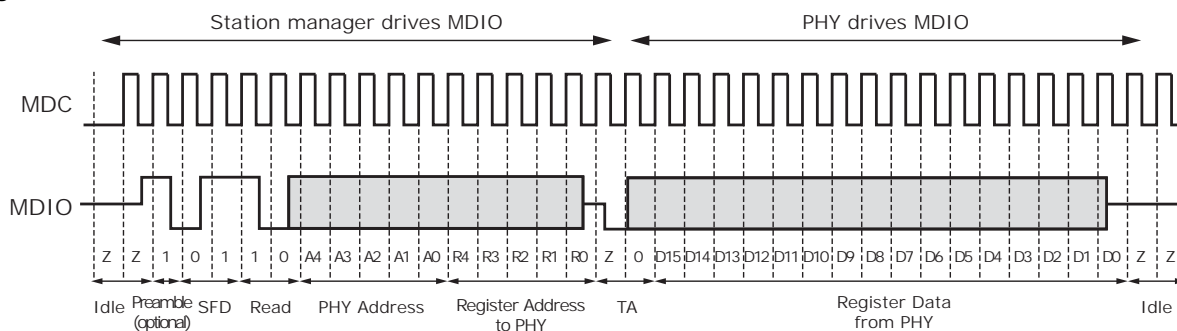
Figure 16 • **SMI Write Frame**
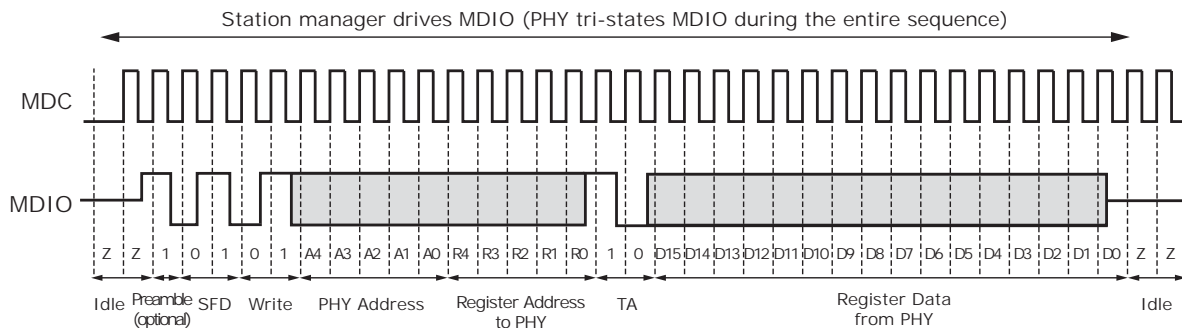
The following list provides additional information about the terms used in the SMI read and write timing diagrams.

4.12.1.1 Idle

During idle, the MDIO node goes to a high-impedance state. This allows an external pull-up resistor to pull the MDIO node up to a logical 1 state. Because the idle mode should not contain any transitions on MDIO, the number of bits is undefined during idle.

4.12.1.2 Preamble

By default, preambles are not expected or required. The preamble is a string of ones. If it exists, the preamble must be at least one bit; otherwise, it can be of an arbitrary length.

4.12.1.3 Start of Frame (SFD)

A pattern of 01 indicates the start of frame. If the pattern is not 01, all following bits are ignored until the next preamble pattern is detected.

4.12.1.4 Read or Write Opcode

A pattern of 10 indicates a read. A 01 pattern indicates a write. If the bits are not either 01 or 10, all following bits are ignored until the next preamble pattern is detected.

4.12.1.5 PHY Address

The particular VSC8512-02 responds to a message frame only when the received PHY address matches its physical address. The physical address is 5 bits long (4:0).

4.12.1.6 Register Address

The next five bits are the register address.

4.12.1.7 Turnaround

The two bits used to avoid signal contention when a read operation is performed on the MDIO are called the turnaround (TA) bits. During read operations, the VSC8512-02 drives the second TA bit, a logical 0.

4.12.1.8 Data

The 16-bits read from or written to the device are considered the data or data stream. When data is read from a PHY, it is valid at the output from one rising edge of MDC to the next rising edge of MDC. When data is written to the PHY, it must be valid around the rising edge of MDC.

4.12.1.9 Idle

The sequence is repeated.

4.12.2 SMI Interrupt

The SMI includes an output interrupt signal, MDINT, for signaling the station manager when certain events occur in the VSC8512-02.

The MDINT pin can be configured for open-drain (active-low) by tying the pin to a pull-up resistor and to VDDIO. The following illustration shows this configuration.

Figure 17 • **MDINT Configured as an Open-Drain (Active-Low) Pin**
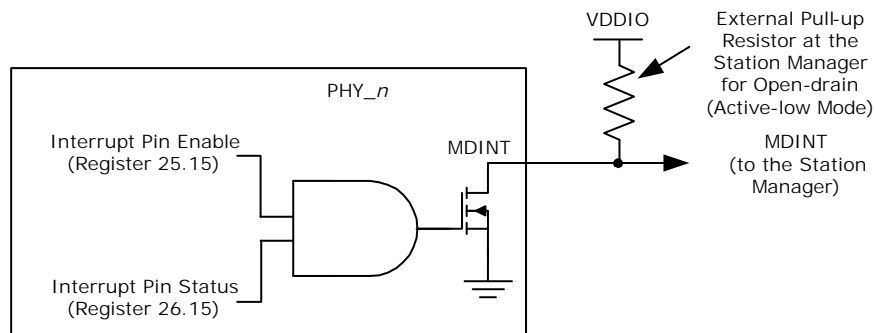
Alternatively, the MDINT pin can be configured for open-source (active-high) by tying the pin to a pull-down resistor and to VSS. The following illustration shows this configuration.

Figure 18 • **MDINT Configured as an Open-Source (Active-High) Pin**
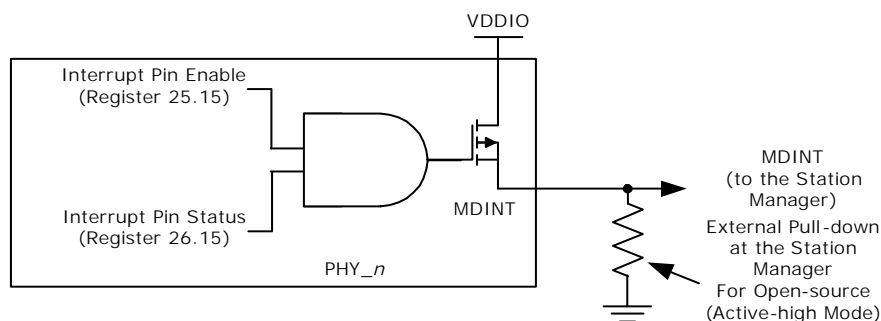
When a PHY generates an interrupt, the MDINT pin is asserted (driven high or low, depending on resistor connection) if the interrupt pin enable bit (MII register 25.15) is set.

4.13   LED Interface

The VSC8512-02 outputs two LED signals per port, LED0 and LED1, through direct-drive signal outputs, or four LED signals per port (LED0, LED1, LED2, and LED3) through an enhanced serial LED mode. For more information, see Enhanced Serial LED Mode, page 26. The polarity of the LED outputs is programmable and can be changed through register 17E2.13:10. The default polarity is active low.

Basic serial LED mode is also supported, in which all possible signals that can be displayed on LEDs are sent out on the serial LED stream for further processing by an external programmable device. For more information, see "Basic Serial LED Mode," .

The PHY[11:8]_LED1 pins are multipurpose pins and can be configured to serve as LED input pins. For more information, see Table 72, page 69.

4.13.1   LED Modes

Each LED pin can be configured to display different status information that can be selected by setting the LED mode in register 29. The modes listed in the following table are equivalent to the setting used in register 29 to configure each LED pin. The default LED state is active low and can be changed by

modifying the value in register 17E2, bits 13:10. The blink/pulse-stretch is dependent on the LED behavior setting in register 30.

Table 8 • **LED Mode and Function Summary**

Mode	Function Name	LED State and Description
0	Link/Activity	1 = No link in any speed on any media interface. 0 = Valid link at any speed on any media interface. Blink or pulse-stretch = Valid link at any speed on any media interface with activity present.
1	Link1000/Activity	1 = No link in 1000BASE-T or 1000BASE-X. 0 = Valid 1000BASE-T or 1000BASE-X. Blink or pulse-stretch = Valid 1000BASE-T or 1000BASE-X link with activity present.
2	Link100/Activity	1 = No link in 100BASE-TX or 100BASE-FX. 0 = Valid 100BASE-TX or 100BASE-FX. Blink or pulse-stretch = Valid 100BASE-TX or 100BASE-FX link with activity present.
3	Link10/Activity	1 = No link in 10BASE-T. 0 = Valid 10BASE-T link. Blink or pulse-stretch = Valid 10BASE-T link with activity present.
4	Link100/1000/Activity	1 = No link in 100BASE-TX, 100BASE-FX, 1000BASE-X, or 1000BASE-T. 0 = Valid 100BASE-TX, 100BASE-FX, 1000BASE-X, or 1000BASE-T link. Blink or pulse-stretch = Valid 100BASE-TX, 100BASE-FX, 1000BASE-X, or 1000BASE-T link with activity present.
5	Link10/1000/Activity	1 = No link in 10BASE-T, 1000BASE-X, or 1000BASE-T. 0 = Valid 10BASE-T, 1000BASE-X, or 1000BASE-T link. Blink or pulse-stretch = Valid 10BASE-T, 1000BASE-X, or 1000BASE-T link with activity present.
6	Link10/100/Activity	1 = No link in 10BASE-T, 100BASE-FX, or 100BASE-TX. 0 = Valid 10BASE-T 100BASE-FX, or 100BASE-TX, link. Blink or pulse-stretch = Valid 10BASE-T, 100BASE-FX, or 100BASE-TX link with activity present.
7	Link100BASE-FX/1000 BASE-X/Activity	1 = No link in 100BASE-FX or 1000BASE-X. 0 = Valid 100BASE-FX or 1000BASE-X link. Blink or pulse-stretch = Valid 100BASE-FX or 1000BASE-X link with activity present.
8	Duplex/Collision	1 = Link established in half-duplex mode, or no link established. 0 = Link established in full-duplex mode. Blink or pulse-stretch = Link established in half-duplex mode but collisions are present.
9	Collision	1 = No collision detected. Blink or pulse-stretch = Collision detected.
10	Activity	1 = No activity present. Blink or pulse-stretch = Activity present (becomes TX activity present if register bit 30.14 is set to 1).
11	100BASE-FX/1000BASE-X Fiber Activity	1 = No 100BASE-FX or 1000BASE-X activity present. Blink or pulse-stretch = 100BASE-FX or 1000BASE-X activity present (becomes RX activity present if register bit 30.14 is set to 1).

Table 8 •   **LED Mode and Function Summary** *(continued)*

Mode	Function Name	LED State and Description
12	Autonegotiation Fault	1 = No autonegotiation fault present. 0 = Autonegotiation fault occurred.
13	Serial Mode	Serial stream = See Basic Serial LED Mode, page 25. Only relevant on PHY port 0 and reserved in others.
14	Force LED Off	1 = De-asserts the LED[1].
15	Force LED On	0 = Asserts the LED[1].

1.   Setting this mode suppresses LED blinking after reset.

4.13.2   Extended LED Modes

In addition to the LED modes in register 29, there are also additional LED modes that are enabled on PHY[11:8]_LED1 whenever the corresponding register 19E1, bits 15 to 12 are set to 1. Each of these bits enables extended modes on a specific LED pin and these extended modes are shown in the following table. For example, LED0 = mode 17 means that register 19E1 bit 12 = 1 and register 29 bits 3 to 0 = 0001.

Table 9 •   **Extended LED Mode and Function Summary**

Mode	Function Name	LED State and Description
16	Link1000BASE-X Activity	1 = No link in 1000BASE-X. 0 = Valid 1000BASE-X link.
17	Link100BASE-FX Activity	1 = No link in 100BASE-FX. 0 = Valid 100BASE-FX link.
18	1000BASE-X Activity	1 = No 1000BASE-X activity present. Blink or pulse-stretch = 1000BASE-X activity present.
19	100BASE-FX Activity	1 = No 100BASE-FX activity present. Blink or pulse-stretch = 100BASE-FX activity present.
20	Force LED Off	1 = De-asserts the LED.
21	Force LED On	0 = Asserts the LED. LED pulsing is disabled in this mode.
22	Fast Link Fail	1 = Enable Fast Link Fail on LED0 pin 0 = Disable

4.13.3   LED Behavior

Several LED behaviors can be programmed into the VSC8512-02. Use the settings in register 30 and 19E1 to program LED behavior, which includes the following:

4.13.3.1   LED Combine

Enables an LED to display the status for a combination of primary and secondary modes. This can be enabled or disabled for each LED pin. For example, a copper link running in 1000BASE-T mode and activity present can be displayed with one LED by configuring an LED pin to Link1000/Activity mode. The LED asserts when linked to a 1000BASE-T partner and also blinks or performs pulse-stretch when activity is either transmitted by the PHY or received by the Link Partner. When disabled, the combine feature only provides status of the selected primary function. In this example, only Link1000 asserts the LED, and the secondary mode, activity, does not display if the combine feature is disabled.

4.13.3.2   LED Blink or Pulse-Stretch

This behavior is used for activity and collision indication. This can be uniquely configured for each LED pin. Activity and collision events can occur randomly and intermittently throughout the link-up period. Blink is a 50% duty cycle oscillation of asserting and de-asserting an LED pin. Pulse-stretch guarantees

that an LED is asserted and de-asserted for a specific period of time when activity is either present or not present. These rates can also be configured using a register setting.

4.13.3.3 Rate of LED Blink or Pulse-Stretch

This behavior controls the LED blink rate or pulse-stretch length when blink/pulse-stretch is enabled on an LED pin. The blink rate, which alternates between a high and low voltage level at a 50% duty cycle, can be set to 2.5 Hz, 5 Hz, 10 Hz, or 20 Hz. For pulse-stretch, the rate can be set to 50 ms, 100 ms, 200 ms, or 400 ms. The blink rate selection for PHY0 globally sets the rate used for all LED pins on all PHY ports.

4.13.3.4 LED Pulsing Enable

To provide additional power savings, the LEDs (when asserted) can be pulsed at 5 kHz, 20% duty cycle.

4.13.3.5 LED Blink After Reset

The LEDs will blink for one second after power-up and after any time all resets have been de-asserted. This can be disabled through register 19E1, bit 11 = 0.

4.13.3.6 Fiber LED Disable

This bit controls whether the LEDs indicate the fiber and copper status (default) or the copper status only.

4.13.3.7 Pulse Programmable Control

These bits add the ability to width and frequency of LED pulses. This feature facilities power reduction options.

4.13.3.8 Fast Link Failure

For more information about this feature, see Fast Link Failure Indication, page 26.

4.13.4 Basic Serial LED Mode

Optionally, the VSC8512-02 can be configured so that access to all its LED signals is available through two pins. This option is enabled by setting LED0 on PHY0 to serial LED mode. When serial LED mode is enabled on PHY0, the PHY0_LED0 pin becomes the basic serial data pin, and the PHY0_LED1 pin becomes the serial clock pin. All other LED pins can still be configured normally. The serial LED mode clocks the 144 LED status bits on the rising edge of the serial clock.

The LED behavior settings can also be used in serial LED mode. The controls are used on a per-PHY basis, where the LED combine and LED blink or pulse-stretch setting of LED0_n for each PHY is used to control the behavior of each bit of the serial LED stream for each corresponding PHY. To configure LED behavior, set device register 30.

The serial bitstream outputs, 1 through 144, of each LED signal are shown in the following table beginning with PHY port 0 and ending with PHY port 11. The individual signals can be clocked in the order shown.

Table 10 • **LED Serial Stream Order**

PHY0	PHY1	PHYx	PHY11
Bit 1. Link/Activity	Bit 13. Link/Activity	Bit [X]. Link/Activity	Bit 133. Link/Activity
Bit 2. Link1000/Activity	Bit 14. Link1000/Activity	Bit [X]. Link1000/Activity	Bit 134. Link1000/Activity
Bit 3. Link100/Activity	Bit 15. Link100/Activity	Bit [X]. Link100/Activity	Bit 135. Link100/Activity
Bit 4. Link10/Activity	Bit 16. Link10/Activity	Bit [X]. Link10/Activity	Bit 136. Link10/Activity
Bit 5. Fiber Link/Activity	Bit 17. Fiber Link/Activity	Bit [X]. Fiber Link/Activity	Bit 137. Fiber Link/Activity
Bit 6. Duplex/Collision	Bit 18. Duplex/Collision	Bit [X]. Duplex/Collision	Bit 138. Duplex/Collision
Bit 7. Collision	Bit 19. Collision	Bit [X]. Collision	Bit 139. Collision
Bit 8. Activity	Bit 20. Activity	Bit [X]. Activity	Bit 140. Activity

Table 10 • **LED Serial Stream Order** *(continued)*

PHY0	PHY1	PHYx	PHY11
Bit 9. Fiber Activity	Bit 21. Fiber Activity	Bit [X]. Fiber Activity	Bit 141. Fiber Activity
Bit 10. TX Activity	Bit 22. TX Activity	Bit [X]. TX Activity	Bit 142. TX Activity
Bit 11. RX Activity	Bit 23. RX Activity	Bit [X]. RX Activity	Bit 143. RX Activity
Bit 12. Autonegotiation Fault	Bit 24. Autonegotiation Fault	Bit [X]. Autonegotiation Fault	Bit 144. Autonegotiation Fault

4.13.5 Enhanced Serial LED Mode

VSC8512-02 can be configured to output up to four LED signals per port on a serial stream that can be de-serialized externally to drive LEDs on the system board. This functionality is controlled by setting register 25G, bits 7:1. In this mode, the serial LED_DATA is shifted out on the falling edge of LED_CLK and is latched in the external serial to parallel converter on the rising edge of LED_CLK. The falling edge of LED_LD signal can be used to shift the data from the shift register in the converter to the parallel output drive register. If a separate parallel output drive register is not used in the external serial to parallel converter, then the LEDs will blink at a high frequency as the data bits are being shifted through which may be undesirable. The LED_PULSE signal provides a 5 kHz pulse stream whose duty cycle can be modulated to turn on/off LEDs at a high rate. This signal can be tied to the output enable signal of the serial to parallel converter to provide the LED dimming functionality to save energy.

4.13.6 LED Port Swapping

For additional hardware configurations, the VSC8512-02 can have its LED port order swapped. This is a useful feature to help simplify PCB layout design. Register 25G bit 0 controls the LED port swapping mode.

4.14 Fast Link Failure Indication

To aid Synchronous Ethernet applications, the VSC8512-02 can indicate the onset of a link failure in less than 1 ms. By comparison, the IEEE 802.3 standard establishes a delay of up to 750 ms before indicating that a 1000BASE-T link is no longer present. A fast link failure indication is critical to support ports used in a synchronization timing link application. The fast link failure indication works for all copper and fiber media speeds. The FAST_LINK_STATUS pin provides the external hardware notification of this event.

Note: For all links except 1000BASE-T, the fast link failure indication matches the link status register (address 1, bit 2). For 1000BASE-T links, the link failure is based on a circuit that analyzes the integrity of the link, and at the indication of failure, will assert.

4.15 Integrated I2C Multiplexer

The VSC8512-02 includes an integrated quad I2C multiplexer (MUX), eliminating the need for an external two-wire serial device for the control and status of SFP or PoE modules. There are five I2C controller pins: four clocks and one shared data pin. Each SFP or PoE connects to the corresponding SFP_SERIALCLK0 or PHY[5:7]_LED1 pins (configured as SFP_SERIALCLK[3:0], respectively), and shares the SFP_SERIALDATA device pin (configured as I2C_SDA), as shown in the following illustration. For SFP modules, VSC8512-02 can also provide control for the MODULE_DETECT and TX_DIS module pins using the multipurpose LED/GPIO pins.

Figure 19 • **I2C MUX with SFP Control and Status**
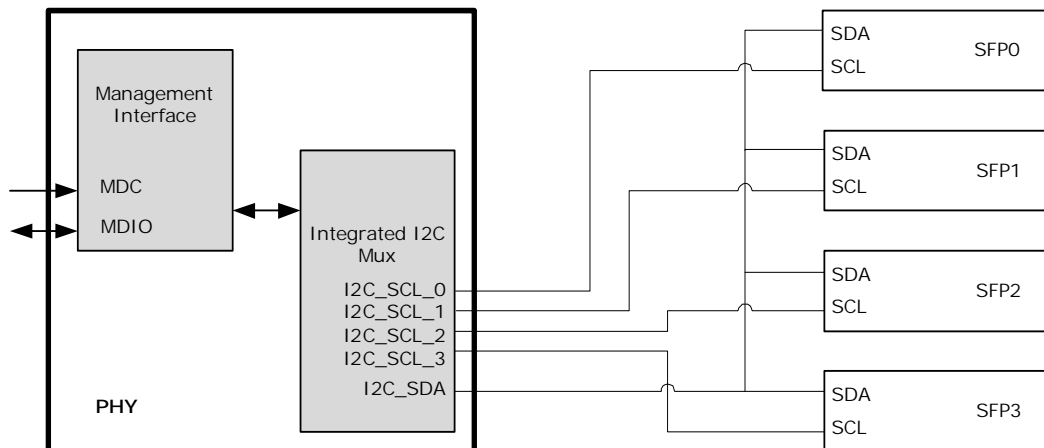
4.15.1 Read/Write Access Using the I2C MUX

Using the integrated I2C MUX, the VSC8512-02 device can read and write to an SFP or PoE module through the SCL and SDA pins. If the ability is required to write to the slave I2C device, refer to the device's specific datasheet for more information.

Note: The VSC8512-02 device does not automatically increment the I2C address. Each desired address must be intentionally set.

Main control of the integrated I2C MUX is available through register 20G. The I2C MUX pins are enabled or disabled using register 20G bits 3:0. Register 20G bits 15:9 set the I2C device address (the default is 0xA0). Using register 20G bits 5:4, the two-wire serial frequency can be changed from 100 kHz to other speeds, such as 50 kHz, 100 kHz (the default), 400 kHz, and 2 MHz. Registers 21G and 22G provide status and control of the read/write process. The following illustration shows the read and write register flow.

Figure 20 • **I2C MUX Read and Write Register Flow**
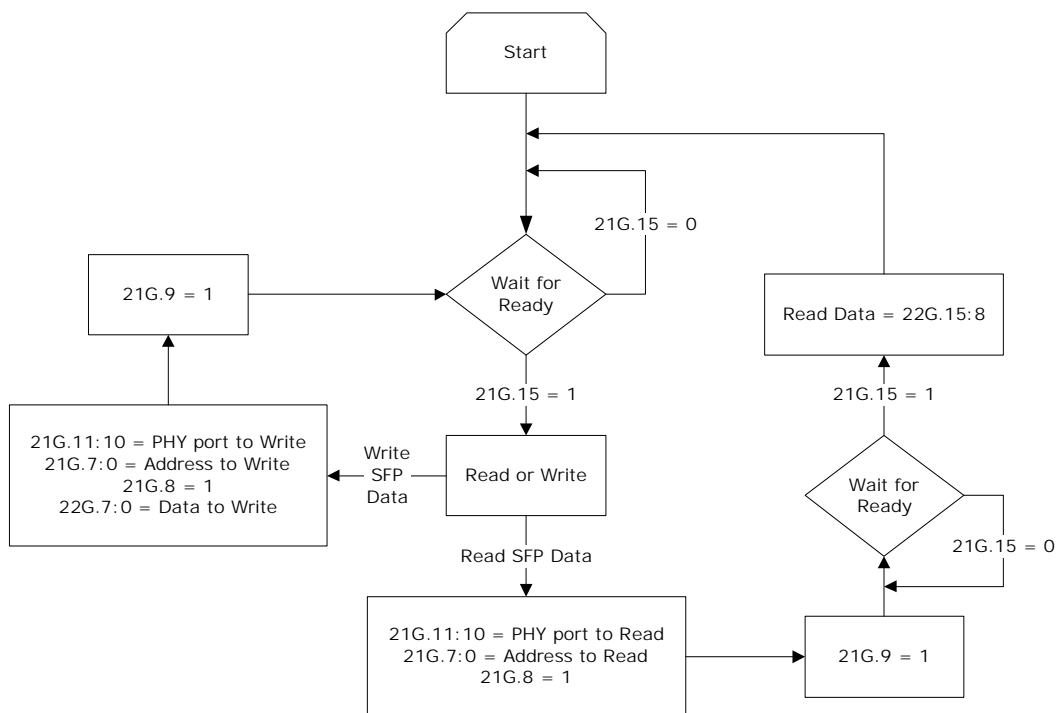
To read a value from a specific address of the I2C slave device:

1. Read the VSC8512-02 device register 21G bit 15, and ensure that it is set.
2. Write the PHY port address to be read to register 21G bits 11:10.
3. Write the I2C address to be read to register 21G bits 7:0.
4. Set both register 21G bits 8 and 9 to 1.
5. When register 21G bit 15 changes to 1, read the 8-bit data value found at register 22G bits 15:8. This is the contents of the address just read by the PHY.

To write a value to a specific address of the I2C slave device:

1. Read the VSC8512-02 device register 21G bit 15 and ensure that it is set.
2. Write the PHY port address to be written to register 21G bits 11:10.
3. Write the address to be written to register 21G bits 7:0.
4. Set register 21 bit 8 to 0.
5. Set register 22G bits 7:0 with the 8-bit value to be written to the slave device.
6. Set register 21G bit 9 to 1.

To avoid collisions during read and write transactions on the I2C serial bus, always wait until register 21G bit 15 changes to 1 before performing another I2C read or write operation.

4.16 GPIO Pins

The VSC8512-02 provides 30 multiplexed multipurpose pins. For more information about the available GPIO pins, see LED and Multi/General Purpose Input and Output Pins, page 99, and for information about configuring them, see General Purpose Registers, page 68.

4.17 Testing Features

The VSC8512-02 device includes several testing features designed to facilitate performing system-level debugging and in-system production testing. This section describes the available features.

4.17.1 Ethernet Packet Generator

The Ethernet packet generator (EPG) can be used at each of the 10/100/1000BASE-T speed settings for copper Cat5 media and fiber media to isolate problems between the MAC and the VSC8512-02, or between a locally connected PHY and its remote link partner. Enabling the EPG feature effectively disables all MAC interface transmit pins and selects the EPG as the source for all data transmitted onto the twisted pair interface. This feature is not used when the SerDes media is set to pass-through mode.

Important The EPG is intended for use with laboratory or in-system testing equipment only. Do not use the EPG testing feature when the VSC8512-02 is connected to a live network.

To enable the VSC8512-02 EPG feature, set the device register bit 29E1.15 to 1.

When the EPG is enabled, packet loss occurs during transmission of packets from the MAC to the PHY. However, the PHY receive output pins to the MAC are still active when the EPG is enabled. If it is necessary to disable the MAC receive pins as well, set the register bit 0.10 to 1.

When the device register bit 29E1.14 is set to 1, the PHY begins transmitting Ethernet packets based on the settings in registers 29E1 and 30E1. These registers set:

- Source and destination addresses for each packet
- Packet size
- Inter-packet gap
- FCS state
- Transmit duration
- Payload pattern

If register bit 29E1.13 is set to 0, register bit 29E1.14 is cleared automatically after 30,000,000 packets are transmitted.

4.17.2 CRC Counters

Two sets of cyclical redundancy check (CRC) counters are available in all PHYs in VSC8512-02 to monitor traffic on the copper and SerDes interfaces.

The device CRC counters operate in 100BASE-FX/1000BASE-X over SerDes mode and 10/100/1000BASE-T mode as follows:

- After receiving a packet on the media interface, register bit 15 in register 18E1 or register 28E3 is set and cleared after being read.
- The packet then is counted by either the good CRC counter or the bad CRC counter.
- Both CRC counters are also automatically cleared when read.

The good CRC counter's highest value is 9,999 packets. After this value is reached, the counter clears on the 10,000th packet and continues to count additional packets beyond that value. The bad CRC counter stops counting when it reaches its maximum counter limit of 255 packets.

4.17.2.1 Copper Interface CRC Counters

Two separate CRC counters are available and reside between the copper interface PCSs and SerDes MAC interface. There is a 14-bit good CRC counter available through register bits 18E1.13:0 and a separate 8-bit bad CRC counter available in register bits 23E1.7:0.

4.17.2.2 SerDes Interface CRC Counters

Two separate CRC counters are available and reside between the SerDes media interface PCSs and SerDes MAC interface. There is a 14-bit good CRC counter available through register bits 28E3.13:0 and a separate 8-bit bad CRC counter available in register bits 29E3.7:0.

4.17.3 Far-End Loopback

The far-end loopback testing feature is enabled by setting register bit 23.3 to 1. When enabled, it forces incoming data from a link partner on the current media interface, into the MAC interface of the PHY, to be retransmitted back to the link partner on the media interface as shown in the following illustration. In addition, the incoming data also appears on the receive data pins of the MAC interface. Data present on the transmit data pins of the MAC interface is ignored when using this testing feature.

Figure 21 • **Far-End Loopback Diagram**
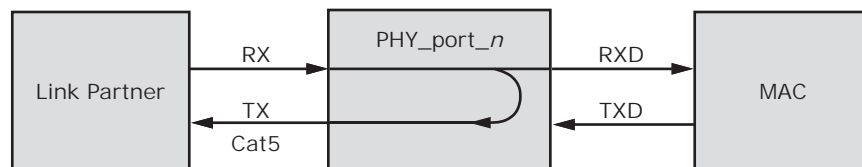
4.17.4 Near-End Loopback

When the near-end loopback testing feature is enabled, transmitted data (TXD) is looped back in the PCS block onto the receive data signals (RXD), as shown in the following illustration. When using this testing feature, no data is transmitted over the network. To enable near-end loopback, set the device register bit 0.14 to 1.

Figure 22 • **Near-End Loopback Diagram**
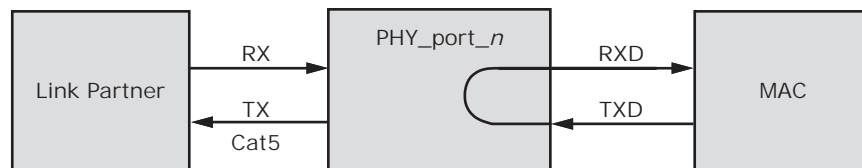
4.17.5 Connector Loopback

The connector loopback testing feature allows the twisted pair interface to be looped back externally. When using this feature, the PHY must be connected to a loopback connector or a loopback cable. Pair A should be connected to pair B, and pair C to pair D, as shown in the following illustration. The connector loopback feature functions at all available interface speeds.

Figure 23 • **Connector Loopback Diagram**
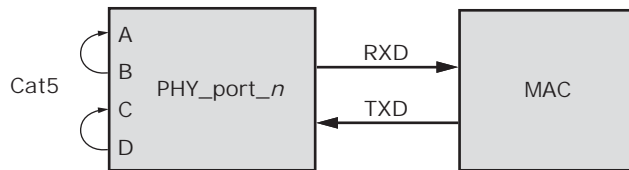
When using the connector loopback testing feature, the device autonegotiation, speed, and duplex configuration is set using device registers 0, 4, and 9. For 1000BASE-T connector loopback, the following additional writes are required. Execute the additional writes in the following order:

1. Enable the 1000BASE-T connector loopback. Set register bit 24.0 to 1.
2. Disable pair swap correction. Set register bit 18.5 to 1.

4.17.6   SerDes Loopbacks

For test purposes, the SerDes and enhanced SerDes macro interfaces provide several data loops. The following illustration shows the SerDes loopbacks.

Figure 24 • **Data Loops of the SerDes Macro**
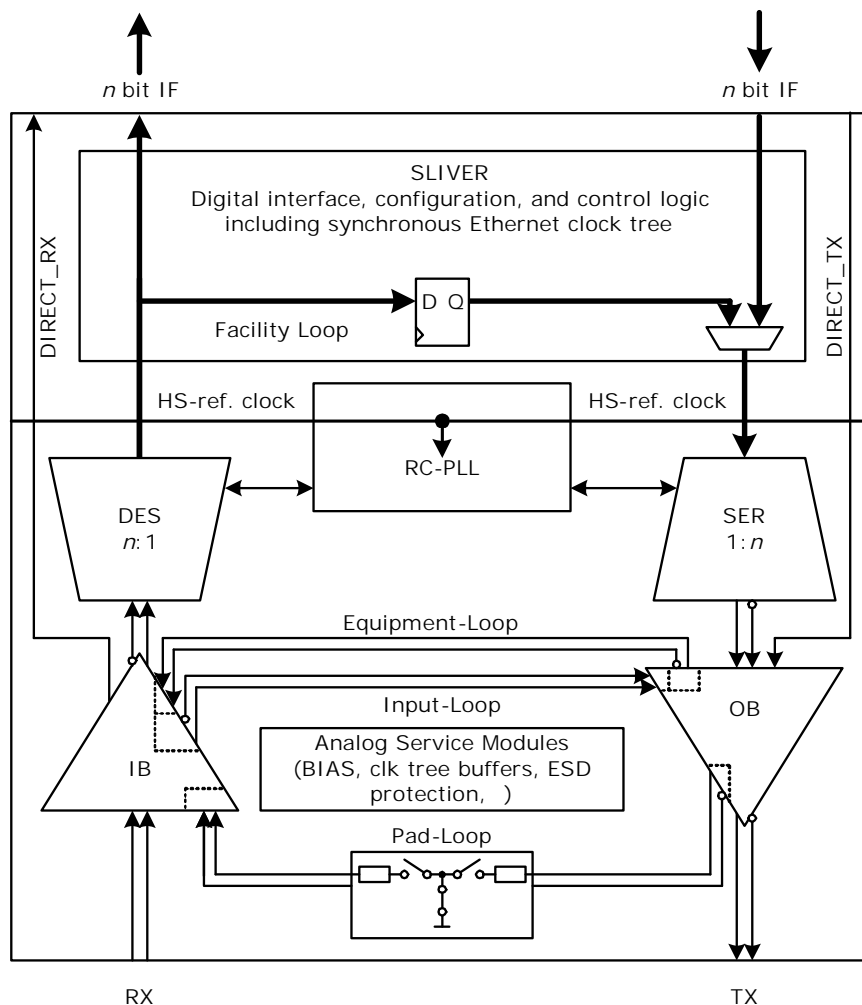
4.17.6.1   SGMII Mode

When the MAC interface is configured in SGMII mode, write the following 16-bit value to register 18G:

Bits 15:12 0x9

Bits 11:8: Port address (0x0 to 0xb)

Bits 7:4: Loopback type

Bits 3:0: 0x2

where loopback type is:

0x0: No loopback

0x1: Pad loopback

0x2: Input loopback

0x4: Facility loopback

0x8: Equipment loopback

4.17.6.2 QSGMII Mode

When the MAC interface is configured in QSGMII mode, the configuration command is the same as SGMII mode, except that the port addresses (bits 11:8) are:

0xC: Enhanced SerDes macro for ports 0–3

0xD: Enhanced SerDes macro for ports 4–7

0xE: Enhanced SerDes macro for ports 8-11

Note: Loopback configuration affects all four ports associated with a QSGMII. Individual port loopback within a QSGMII is not possible.

4.17.6.3 Fiber Media Port Mode

When the SerDes is configured as a fiber media port, write the following 16-bit value to register 18G:

Bits 15:12: 0x8

Bits 11:8: Port address

Bits 7:4: Loopback type

Bits 3:0: 0x2

where port address is:

0x1: Fiber8 port

0x2: Fiber9 port

0x4: Fiber10 port

0x8: Fiber11 port

Port addresses for fiber media SerDes can be OR'ed together to address multiple ports using a single command. Bit 18G.15 will be cleared when the internal configuration is complete.

4.17.6.4 Facility Loop

The recovered and de-multiplexer deserializer data output is looped back to the serializer data input and replaces the data delivered by the digital core. This test loop provides the possibility to test the complete analog macro data path from outside including input buffer, clock and data recovery, serialization and output buffer. The data received by the input buffer must be transmitted by the output buffer after some delay.

Additional configuration of the SerDes and Enhanced SerDes macros is required for facility loopback mode. When entering facility loopback mode, the set = 1 option should be run; when exiting facility loopback mode, the set = 0 option should be run.

For SerDes macro configurations, the following software script must be executed after running the command to enable/disable facility loopback mode.

```
PhyWrite(PhyBaseAddr, 31, 0x0010);
PhyWrite(PhyBaseAddr, 18, 0x8s03);
// where "s" is the physical address of the SerDes macro
PhyWrite(PhyBaseAddr, 18, 0xd7d3);
PhyWrite(PhyBaseAddr, 18, 0x8007);
tmp1 = PhyRead(PhyBaseAddr, 18);
tmp2 = tmp1 & 0x0ff0;
if (set)
    tmp3 = tmp2 | 0x0010;
else
    tmp3 = tmp2 & 0x0fe0;
tmp4 = tmp3 | 0x8006;
PhyWrite(PhyBaseAddr, 18, tmp4);
if (SGMII)
PhyWrite(PhyBaseAddr, 18, 0x9p40);
// where "p" is the logical address of the SGMII interface
else
    PhyWrite(PhyBaseAddr, 18, 0x8p40);
// where "p" is the logical address of the Fiber media interface
```

PhyBaseAddr is the base address of the internal PHYs and is equal to 0, 12, 4, or 20 based on the value of the PHYADDR4 and PHYADDR3 pins. For more information, see Table 2, page 10.

The value of *s* is 0–7 and corresponds to the physical address of the SerDes macro. For SerDes SGMII MAC interface configuration, the value of *p* is 1, 2, 4, 5, 7, 8, 10, or 11 and is the logical address of the SGMII lane that corresponds to the SerDes macro with physical address *s*. For SerDes Fiber Media interface configuration, the value of *p* is 8–11 and is the logical address of the Fiber Media lane that corresponds to the SerDes macro with physical address *s*. For more information about address mapping, see Table 4, page 11.

For Enhanced SerDes macro configurations, the following software script must be executed after running the command to enable/disable facility loopback mode.

```
PhyWrite(PhyBaseAddr, 31, 0x0010);
PhyWrite(PhyBaseAddr, 18, 0x8s13);
// where "s" is the physical address of the SerDes macro
PhyWrite(PhyBaseAddr, 18, 0xd7d3);
PhyWrite(PhyBaseAddr, 18, 0x8007);
tmp1 = PhyRead(PhyBaseAddr, 18);
tmp2 = tmp1 & 0x0ff0;
if (set)
    tmp3 = tmp2 | 0x0100;
else
    tmp3 = tmp2 & 0x0ef0;
tmp4 = tmp3 | 0x8006;
PhyWrite(PhyBaseAddr, 18, tmp4);
PhyWrite(PhyBaseAddr, 18, 0x9p40);
// where "p" is the logical address of the SGMII or QSGMII interface
```

PhyBaseAddr is the base address of the internal PHYs and is equal to 0, 12, 4, or 20 based on the value of the PHYADD4 and PHYADD3 pins. For more information, see Table 2, page 10.

The value of *s* is 0–3 and corresponds to the physical address of the enhanced SerDes macro. For enhanced SerDes SGMII MAC interface configuration, the value of *p* is 0, 3, 6, or 9 and is the logical address of the SGMII lane that corresponds to the enhanced SerDes macro with physical address *s*. For enhanced SerDes QSGMII MAC interface configuration, the value of *p* is 0–2 and is the logical address of the QSGMII lane that corresponds to the enhanced SerDes macro with physical address *s*. For more information about address mapping, see Table 4, page 11.

4.17.6.4.1 Equipment Loop

The 1-bit data stream at the serializer output is looped back to the deserializer and replaces the received data stream from the input buffer. This test loop provides the possibility to verify the digital data path

internally. The transmit data goes through the serialization, the clock and data recovery and deserialization before the data is fed back to the digital core.

4.17.6.4.2 Input Loop

The received 1-bit data stream of the input buffer is looped back asynchronously to the output buffer. This test loop provides the possibility to the test only the analog parts of the SGMII interface because only the input and output buffer are part of this loop.

4.17.6.4.3 Pad Loop

The 1-bit data stream at the output buffer output is looped back to the input buffer input and added to the differential pad signal. Therefore, the input pad should not be driven when the output loop is activated. The test loop provides a means to test the complete SGMII macro data path, including the input and output buffers.

4.17.7 VeriPHY Cable Diagnostics

The VSC8512-02 includes a comprehensive suite of cable diagnostic functions that are available using SMI reads and writes. These functions enable a variety of cable operating conditions and status to be accessed and checked. The VeriPHY suite has the ability to identify the cable length and operating conditions and to isolate a variety of common faults that can occur on Cat5 twisted pair cabling.

For functional details of the VeriPHY suite and the operating instructions, see the ENT-AN0125 PHY, Integrated PHY-Switch VeriPHY - Cable Diagnostics application note.

4.17.8 JTAG Boundary Scan

The VSC8512-02 supports the test access port (TAP) and boundary scan architecture described in IEEE 1149.1. The device includes an IEEE 1149.1-compliant test interface, referred to as a JTAG TAP interface.

The JTAG boundary scan logic on the VSC8512-02, accessed using its TAP interface, consists of a boundary scan register and other logic control blocks. The TAP controller includes all IEEE-required signals (TMS, TCK, TDI, and TDO), in addition to the optional asynchronous reset signal NTRST. The following illustration shows the TAP and boundary scan architecture.

Figure 25 • **Test Access Port and Boundary Scan Architecture**
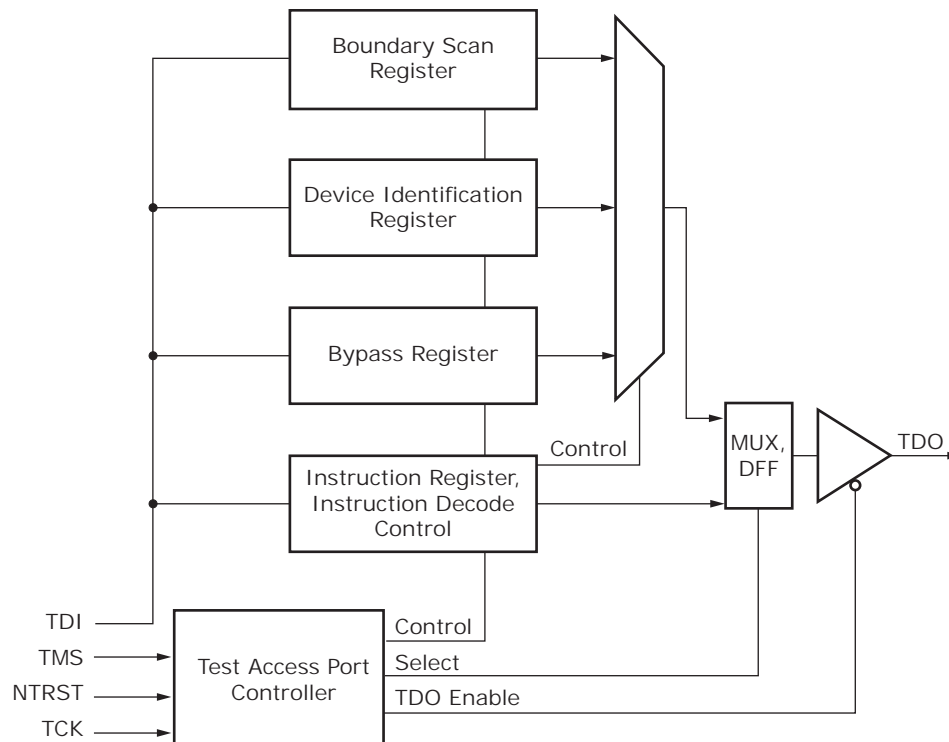
After a TAP reset, the device identification register is serially connected between TDI and TDO by default. The TAP instruction register is loaded either from a shift register when a new instruction is shifted in, or, if there is no new instruction in the shift register, a default value of 6'b100100 (IDCODE) is loaded. Using this method, there is always a valid code in the instruction register, and the problem of toggling instruction bits during a shift is avoided. Unused codes are mapped to the BYPASS instruction.

4.17.9 JTAG Instruction Codes

The VSC8512-02 supports the following instruction codes:

4.17.9.1 EXTEST

Allows tests of the off-chip circuitry and board-level interconnections by sampling input pins and loading data onto output pins. Outputs are driven by the contents of the boundary-scan cells, which have to be updated with valid values, with the PRELOAD instruction, prior to the EXTEST instruction.

4.17.9.2 SAMPLE/PRELOAD

Allows a snapshot of inputs and outputs during normal system operation to be taken and examined. It also allows data values to be loaded into the boundary-scan cells prior to the selection of other boundary-scan test instructions.

4.17.9.3 IDCODE

Provides the version number (bits 31:28), device family ID (bits 27:12), and the manufacturer identity (bits 11:1) to be serially read from the device.

The following table provides information about the meaning of IDCODE binary values stored in the device JTAG registers.

Table 11 • **IDCODE JTAG Device Identification Register Descriptions**

Description	Device Version	Family ID	Manufacturing Identity	LSB
Bit field	31–28	27–12	11–1	0

Description	Device Version	Family ID	Manufacturing Identity	LSB
Binary value	0000	1011 0000 0000 0001	000 0111 0100	1

4.17.9.4 USERCODE

Provides the version number (bits 31:28), part number (bits 27:12), and the manufacturer identity (bits 11:1) to be serially read from the device. The following table provides information about the meaning of USERCODE binary values stored in the device JTAG registers.

Table 12 • **USERCODE JTAG Device Identification Register Descriptions**

Description	Device Version	Model Number	Manufacturing Identity	LSB
Bit field	31–28	27–12	11–1	0
Binary value	0010	1000 0101 0001 0010	000 0111 0100	1

4.17.9.5 CLAMP

Allows the state of the signals driven from the component pins to be determined from the boundary scan register while the bypass register is selected as the serial path between TDI and TDO. While the CLAMP instruction is selected, the signals driven from the component pins do not change.

4.17.9.6 HIGHZ

Places the component in a state in which all of its system logic outputs are placed in a high-impedance state. In this state, an in-circuit test system can drive signals onto the connections normally driven by a component output without incurring a risk of damage to the component. This makes it possible to use a board where not all of the components are compatible with the IEEE 1149.1 standard.

4.17.9.7 BYPASS

The bypass register contains a single shift-register stage and is used to provide a minimum-length serial path (one TCK clock period) between TDI and TDO to bypass the device when no test operation is required.

The following table provides information about the location and IEEE compliance of the JTAG instruction codes used in the VSC8512-02. Instructions not explicitly listed in the table are reserved. For more information about these IEEE specifications, visit the IEEE Web site at www.IEEE.org.

Table 13 • **JTAG Interface Instruction Codes**

Instruction	Code	Selected Register	Register Width	IEEE 1149.1	IEEE 1149.6
EXTEST	6'b000000	Boundary-Scan	161	Mandatory	
SAMPLE/PRELOAD	6'b000001	Boundary-Scan	161	Mandatory	
IDCODE	6'b100100	Device Identification	32	Optional	
USERCODE	6'b100101	Device Identification	32	Optional	
CLAMP	6'b000010	Bypass Register	1	Optional	
HIGHZ	6'b000101	Bypass Register	1	Optional	
BYPASS	6'b111111	Bypass Register	1	Mandatory	
EXTEST_PULSE	6'b000011	Boundary-Scan Register	161		Mandatory
EXTEST_TRAIN	6'b000100	Boundary-Scan Register	161		Mandatory

4.17.10 Boundary Scan Register Cell Order

All inputs and outputs are observed in the boundary scan register cells. All outputs are additionally driven by the contents of boundary scan register cells. Bidirectional pins have all three related boundary scan register cells: input, output, and control.

The complete boundary scan cell order is available as a BSDL file format on the Microsemi Web site at www.microsemi.com.

4.17.11 JTAG Boundary Scan Interface

The IEEE 1149.6 AC-JTAG solution integrated on all SerDes ports of the VSC8512-02 extends the capability of IEEE 1149.1 boundary scan for robust board-level testing. This interface is backward-compatible to the IEEE 1149.1 standard.

4.18 100FX Halt Code Transmission and Reception

The VSC8512-02 device supports transmission and reception of halt code words in 100BASE-FX mode. There are three separate scripts provided to initiate transmission of halt code words, stop transmission of halt code words and detect reception of halt code words. Use the following scripts to implement each of these functions:

Sending the HALT codeword:

```
PhyWrite( <phy>, 31, 0x52b5 );
PhyWrite( <phy>, 16, 0xac82 );
reg18 = PhyRead( <phy>, 18 );
reg18 = (reg18 & 0xf0) | 0x0c;
PhyWrite( <phy>, 18, reg18 );
PhyWrite( <phy>, 17, 0xe739 );
PhyWrite( <phy>, 16, 0x8c82 );

PhyWrite< <phy>, 16, 0xbe80 );
reg17 = PhyRead( <phy>, 17 );
reg18 = PhyRead( <phy>, 18 );
reg17 = reg17 | 0x0040;
PhyWrite( <phy>, 18, reg18 );
PhyWrite( <phy>, 17, reg17 );
PhyWrite( <phy>, 16, 0x9e80 );
PhyWrite( <phy>, 31, 0 );
```

Stop sending the HALT codeword:

```
PhyWrite( <phy>, 31, 0x52b5 );
PhyWrite< <phy>, 16, 0xbe80 );
reg17 = PhyRead( <phy>, 17 );
reg18 = PhyRead( <phy>, 18 );
reg17 = reg17 & ~0x0040;
PhyWrite( <phy>, 18, reg18 );
PhyWrite( <phy>, 17, reg17 );
PhyWrite( <phy>, 16, 0x9e80 );
PhyWrite( <phy>, 31, 0 );
```

Detecting if the HALT codeword is being sent by the link partner:

```
long patternset[5] = {
    0xce739,
    0xe739c,
    0x739ce,
    0x39ce7,
    0x9ce73
};
```

Turning on the pattern checker:

```
PhyWrite( <phy>, 31, 0x52b5 );
PhyWrite( <phy>, 16, 0xbe80 );
reg18 = PhyRead( <phy>, 18 );
reg17 = PhyRead( <phy>, 17 );
reg17 = reg17 | 4;
PhyWrite( <phy>, 18, reg18 );
PhyWrite( <phy>, 17, reg17 );
PhyWrite( <phy>, 16, 0x9e80 );
```

Sweeping through all 5 pattern shifts looking for a match:

```
for (i = 0, matchfailed = 1; i < 5 && matchfailed; ++i) {
PhyWrite( <phy>, 16, 0xac84 );
reg18 = PhyRead( <phy>, 18 );
reg18 = (reg18 & 0xf0) | (patternset[i] >> 16)
PhyWrite( <phy>, 18, reg18 );
PhyWrite( <phy>, 17, patternset[i] & 0xffff );
PhyWrite( <phy>, 16, 0x8c84 );

PhyWrite( <phy>, 16, 0xbe84 ); // Dummy read to clear latched mismatch
PhyWrite( <phy>, 16, 0xbe84 ); // Read pattern check failure status
matchfailed = PhyRead( <phy>, 17 ) & 1; // Extract pattern check failure status
}
```

Turning off the pattern checker:

```
PhyWrite( <phy>, 16, 0xbe80 );
reg18 = PhyRead( <phy>, 18 );
reg17 = PhyRead( <phy>, 17 );
reg17 = reg17 & ~4;
PhyWrite( <phy>, 18, reg18 );
PhyWrite( <phy>, 17, reg17 );
PhyWrite( <phy>, 16, 0x9e80 );

PhyWrite( <phy>, 31, 0 );

HALT_codeword_detected = !matchfailed;
```

4.19 Configuration

The VSC8512-02 can be configured by setting internal memory registers using the management interface.

5 Registers

This section provides information about how to configure the VSC8512-02 using its internal memory registers and the management interface.

The VSC8512-02 uses several different types of registers:

- IEEE Clause 22 device registers with addresses from 0 to 31
- Three pages of extended registers with addresses from 16E1–30E1, 16E2–30E2, and 16E3–30E3
- General-purpose registers with addresses from 0G to 30G
- IEEE Clause 45 devices registers accessible through the Clause 22 registers 13 and 14 to support IEEE 802.3az Energy Efficient Ethernet registers

The following illustration shows the relationship between the device registers and their address spaces.

Figure 26 • **Register Space Diagram**
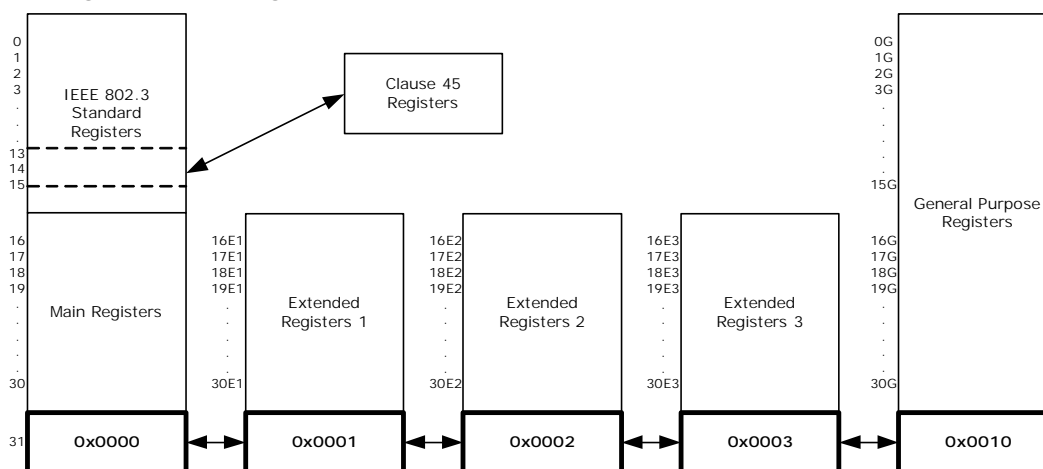
- Reserved Registers—For main registers 16–31, extended registers 16E1–30E1, 16E2–30E2, 16E3–30E3, and general purpose registers 0G–30G, any bits marked as Reserved should be processed as read-only and their states as undefined.
- Reserved Bits—In writing to registers with reserved bits, use a read-modify-then-write technique, where the entire register is read but only the intended bits to be changed are modified. Reserved bits cannot be changed and their read state cannot be considered static or unchanging.

5.1 IEEE Standard and Main Registers

In the VSC8512-02, the page space of the standard registers consists of the IEEE standard registers and the Microsemi standard registers. The following table lists the names of the registers associated with the addresses as dictated by the IEEE standard.

Table 14 • **IEEE 802.3 Standard Registers**

Address	Name
0	Mode Control
1	Mode Status
2	PHY Identifier 1
3	PHY Identifier 2
4	Autonegotiation Advertisement
5	Autonegotiation Link Partner Ability
6	Autonegotiation Expansion

Table 14 • **IEEE 802.3 Standard Registers** *(continued)*

Address	Name
7	Autonegotiation Next-Page Transmit
8	Autonegotiation Link Partner Next-Page Receive
9	1000BASE-T Control
10	1000BASE-T Status
11–12	Reserved
13	Clause 45 access registers from IEEE 802.3 Table 22-6 and 22.24.3.11-12 and Annex 22D
14	Clause 45 access registers from IEEE 802.3 Table 22-6 and 22.24.3.11-12 and Annex 22D
15	1000BASE-T Status Extension 1

The following table lists the names of the registers in the main page space of the device. These registers are accessible only when register address 31 is set to 0x0000.

Table 15 • **Main Registers**

Address	Name
16	100BASE-TX Status Extension 1
17	1000BASE-T Status Extension 2
18	Bypass Control
19	Error Counter 1
20	Error Counter 2
21	Error Counter 3
22	Extended Control and Status
23	Extended PHY Control 1
24	Extended PHY Control 2
25	Interrupt Mask
26	Interrupt Status
27	Reserved
28	Auxiliary Control and Status
29	LED Mode Select
30	LED Behavior
31	Extended Register Page Access

5.1.1 Mode Control

The device register at memory address 0 controls several aspects of VSC8512-02 functionality. The following table shows the available bit settings in this register and what they control.

Table 16 • **Mode Control, Address 0 (0x00)**

Bit	Name	Access	Description	Default
15	Software reset	R/W	Self-clearing. Restores all serial management interface (SMI) registers to default state, except for sticky and super-sticky bits. 1: Reset asserted. 0: Reset de-asserted. Wait [X] after setting this bit to initiate another SMI register access.	0
14	Loopback	R/W	1: Loopback enabled. 0: Loopback disabled. When loop back is enabled, the device functions at the current speed setting and with the current duplex mode setting (bits 6, 8, and 13 of this register).	0
13	Forced speed selection LSB	R/W	Least significant bit. MSB is bit 6. 00: 10 Mbps. 01: 100 Mbps. 10: 1000 Mbps. 11: Reserved.	0
12	Autonegotiation enable	R/W	1: Autonegotiation enabled. 0: Autonegotiation disabled.	1
11	Power-down	R/W	1: Power-down enabled.	0
10	Isolate	R/W	1: Disable MAC interface outputs and ignore MAC interface inputs.	0
9	Restart autonegotiation	R/W	Self-clearing bit. 1: Restart autonegotiation on media interface.	0
8	Duplex	R/W	1: Full-duplex. 0: Half-duplex.	0
7	Collision test enable	R/W	1: Collision test enabled.	0
6	Forced speed selection MSB	R/W	Most significant bit. LSB is bit 13. 00: 10 Mbps. 01: 100 Mbps. 10: 1000 Mbps. 11: Reserved.	10

Table 16 • **Mode Control, Address 0 (0x00)** *(continued)*

Bit	Name	Access	Description	Default
5	Unidirectional enable	R/W	When bit 0.12 = 1 or bit 0.8 = 0, this bit is ignored. When bit 0.12 = 0 and bit 0.8 = 1, the behavior is as follows: 1: Enable transmit from media independent interface regardless of whether the PHY has determined that a valid link has been established. 0: Enable transmit from media independent interface only when the PHY has determined that a valid link has been established **Note:** This bit is only applicable in 100BASE-FX and 1000BASE-X fiber media modes for ports 8-11.	0
4:0	Reserved	RO	Reserved.	00000

5.1.2 Mode Status

The register at address 1 in the device main registers space allows you to read the currently enabled mode setting. The following table shows possible readouts of this register.

Table 17 • **Mode Status, Address 1 (0x01)**

Bit	Name	Access	Description	Default
15	100BASE-T4 capability	RO	1: 100BASE-T4 capable.	0
14	100BASE-TX FDX capability	RO	1: 100BASE-TX FDX capable.	1
13	100BASE-TX HDX capability	RO	1: 100BASE-TX HDX capable.	1
12	10BASE-T FDX capability	RO	1: 10BASE-T FDX capable.	1
11	10BASE-T HDX capability	RO	1: 10BASE-T HDX capable.	1
10	100BASE-T2 FDX capability	RO	1: 100BASE-T2 FDX capable.	0
9	100BASE-T2 HDX capability	RO	1: 100BASE-T2 HDX capable.	0
8	Extended status enable	RO	1: Extended status information present in register 15.	1
7	Unidirectional ability	RO	1: PHY able to transmit from media independent interface regardless of whether the PHY has determined that a valid link has been established. 0: PHY able to transmit from media independent interface only when the PHY has determined that a valid link has been established. **Note:** This bit is only applicable to 100BASE-FX and 1000BASE-X fiber media modes.	1
6	Preamble suppression capability	RO	1: MF preamble can be suppressed. 0: MF required.	1
5	Autonegotiation complete	RO	1: Autonegotiation complete.	0

Table 17 • **Mode Status, Address 1 (0x01)** *(continued)*

Bit	Name	Access	Description	Default
4	Remote fault	RO	Latches high. 1: Far-end fault detected.	0
3	Autonegotiation capability	RO	1: Autonegotiation capable.	1
2	Link status	RO	Latches low. 1: Link is up.	0
1	Jabber detect	RO	Latches high. 1: Jabber condition detected.	0
0	Extended capability	RO	1: Extended register capable.	1

5.1.3   Device Identification

All 16 bits in both register 2 and register 3 in the VSC8512-02 are used to provide information associated with aspects of the device identification. The following tables list the expected readouts.

Table 18 • **Identifier 1, Address 2 (0x02)**

Bit	Name	Access	Description	Default
15:0	Organizationally unique identifier (OUI)	RO	OUI most significant bits (3:18)	0×0007

Table 19 • **Identifier 2, Address 3 (0x03)**

Bit	Name	Access	Description	Default
15:10	OUI	RO	OUI least significant bits (19:24)	000001
9:4	Microsemi model number	RO	VSC8512-02 (0x2e)	101110
3:0	Device revision number	RO		0011

5.1.4   Autonegotiation Advertisement

The bits in address 4 in the main registers space control the VSC8512-02 ability to notify other devices of the status of its autonegotiation feature. The following table shows the available settings and readouts.

Table 20 • **Device Autonegotiation Advertisement, Address 4 (0x04)**

Bit	Name	Access	Description	Default
15	Next page transmission request	R/W	1: Request enabled	0
14	Reserved	RO	Reserved	0
13	Transmit remote fault	R/W	1: Enabled	0
12	Reserved	R/W	Reserved	0
11	Advertise asymmetric pause	R/W	1: Advertises asymmetric pause	0
10	Advertise symmetric pause	R/W	1: Advertises symmetric pause	0
9	Advertise100BASE-T4	R/W	1: Advertises 100BASE-T4	0
8	Advertise100BASE-TX FDX	R/W	1: Advertise 100BASE-TX FDX	1
7	Advertise100BASE-TX HDX	R/W	1: Advertises 100BASE-TX HDX	1
6	Advertise10BASE-T FDX	R/W	1: Advertises 10BASE-T FDX	1
5	Advertise10BASE-T HDX	R/W	1: Advertises 10BASE-T HDX	1

Table 20 • **Device Autonegotiation Advertisement, Address 4 (0x04)** *(continued)*

Bit	Name	Access	Description	Default
4:0	Advertise selector	R/W		00001

5.1.5 Link Partner Autonegotiation Capability

The bits in main register 5 can be used to determine if the Cat5 link partner (LP) used with the VSC8512-02 is compatible with the autonegotiation functionality.

Table 21 • **Autonegotiation Link Partner Ability, Address 5 (0x05)**

Bit	Name	Access	Description	Default
15	LP next page transmission request	RO	1: Requested	0
14	LP acknowledge	RO	1: Acknowledge	0
13	LP remote fault	RO	1: Remote fault	0
12	Reserved	RO	Reserved	0
11	LP advertise asymmetric pause	RO	1: Capable of asymmetric pause	0
10	LP advertise symmetric pause	RO	1: Capable of symmetric pause	0
9	LP advertise 100BASE-T4	RO	1: Capable of 100BASE-T4	0
8	LP advertise 100BASE-TX FDX	RO	1: Capable of 100BASE-TX FDX	0
7	LP advertise 100BASE-TX HDX	RO	1: Capable of 100BASE-TX HDX	0
6	LP advertise 10BASE-T FDX	RO	1: Capable of 10BASE-T FDX	0
5	LP advertise 10BASE-T HDX	RO	1: Capable of 10BASE-T HDX	0
4:0	LP advertise selector	RO		00000

5.1.6 Autonegotiation Expansion

The bits in main register 6 work together with those in register 5 to indicate the status of the LP autonegotiation functioning. The following table shows the available settings and readouts.

Table 22 • **Autonegotiation Expansion, Address 6 (0x06)**

Bit	Name	Access	Description	Default
15:5	Reserved	RO	Reserved.	All zeros
4	Parallel detection fault	RO	This bit latches high. 1: Parallel detection fault.	0
3	LP next page capable	RO	1: LP is next page capable.	0
2	Local PHY next page capable	RO	1: Local PHY is next page capable.	1
1	Page received	RO	This bit latches low. 1: New page is received.	0
0	LP is autonegotiation capable	RO	1: LP is capable of autonegotiation.	0

5.1.7 Transmit Autonegotiation Next Page

The settings in register 7 in the main registers space provide information about the number of pages in an autonegotiation sequence. The following table shows the settings available.

Table 23 • **Autonegotiation Next Page Transmit, Address 7 (0x07)**

Bit	Name	Access	Description	Default
15	Next page	R/W	1: More pages follow	0
14	Reserved	RO	Reserved	0
13	Message page	R/W	1: Message page 0: Unformatted page	1
12	Acknowledge 2	R/W	1: Complies with request 0: Cannot comply with request	0
11	Toggle	RO	1: Previous transmitted LCW = 0 0: Previous transmitted LCW = 1	0
10:0	Message/unformatted code	R/W		00000000001

5.1.8 Autonegotiation Link Partner Next Page Receive

The bits in register 8 of the main register space work together with register 7 to determine certain aspects of the LP autonegotiation. The following table shows the possible readouts.

Table 24 • **Autonegotiation LP Next Page Receive, Address 8 (0x08)**

Bit	Name	Access	Description	Default
15	LP next page	RO	1: More pages follow	0
14	Acknowledge	RO	1: LP acknowledge	0
13	LP message page	RO	1: Message page 0: Unformatted page	0
12	LP acknowledge 2	RO	1: LP complies with request	0
11	LP toggle	RO	1: Previous transmitted LCW = 0 0: Previous transmitted LCW = 1	0
10:0	LP message/unformatted code	RO		All zeros

5.1.9 1000BASE-T Control

The VSC8512-02's 1000BASE-T functionality is controlled by the bits in register 9 of the main register space. The following table shows the settings and readouts available.

Table 25 • **1000BASE-T Control, Address 9 (0x09)**

Bit	Name	Access	Description	Default
15:13	Transmitter test mode	R/W	000: Normal. 001: Mode 1: Transmit waveform test. 010: Mode 2: Transmit jitter test as master. 011: Mode 3: Transmit jitter test as slave. 100: Mode 4: Transmitter distortion test. 101–111: Reserved	000
12	Master/slave manual configuration	R/W	1: Master/slave manual configuration enabled.	0

Table 25 • **1000BASE-T Control, Address 9 (0x09)** *(continued)*

Bit	Name	Access	Description	Default
11	Master/slave value	R/W	This register is only valid when bit 9.12 is set to 1. 1: Configure PHY as master during negotiation. 0: Configure PHY as slave during negotiation.	0
10	Port type	R/W	1: Multi-port device. 0: Single-port device.	1
9	1000BASE-T FDX capability	R/W	1: PHY is 1000BASE-T FDX capable.	1
8	1000BASE-T HDX capability	R/W	1: PHY is 1000BASE-T HDX capable.	1
7:0	Reserved	R/W	Reserved.	0x00

Note: Transmitter test mode (bits 15:13) operates in the manner described in IEEE 802.3 section 40.6.1.1.2. When using any of the transmitter test modes, the automatic media-sense feature must be disabled. For more information, see Extended PHY Control 2, page 51.

5.1.10 1000BASE-T Status

The bits in register 10 of the main register space can be read to obtain the status of the 1000BASE-T communications enabled in the device. The following table shows the readouts.

Table 26 • **1000BASE-T Status, Address 10 (0x0A)**

Bit	Name	Access	Description	Default
15	Master/slave configuration fault	RO	This bit latches high. 1: Master/slave configuration fault detected. 0: No master/slave configuration fault detected.	0
14	Master/slave configuration resolution	RO	1: Local PHY configuration resolved to master. 0: Local PHY configuration resolved to slave.	1
13	Local receiver status	RO	1: Local receiver is operating normally.	0
12	Remote receiver status	RO	1: Remote receiver OK.	0
11	LP 1000BASE-T FDX capability	RO	1: LP 1000BASE-T FDX capable.	0
10	LP 1000BASE-T HDX capability	RO	1: LP 1000BASE-T HDX capable.	0
9:8	Reserved	RO	Reserved.	00
7:0	Idle error count	RO	Self-clearing register.	0x00

5.1.11 MMD Access Control Register

The bits in register 13 of the main register space are a window to the EEE registers as defined in IEEE 802.3az Clause 45.

Table 27 • **MMD EEE Access, Address 13 (0x0D)**

Bit	Name	Access	Description
15:14	Function	R/W	00: Address 01: Data, no post increment 10: Data, post increment for read and write 11: Data, post increment for write only
13:5	Reserved	R/W	Reserved
4:0	DVAD	R/W	Device address as defined in IEEE 802.3az table 45-1

5.1.12 MMD Address or Data Register

The bits in register 14 of the main register space are a window to the EEE registers as defined in IEEE 802.3az Clause 45.

Table 28 • **MMD Address or Data Register, Address 14 (0x0E)**

Bit	Name	Access	Description
15:0	Register Address/Data	R/W	If register 13.15:14 = 2'b00, address of register of the device that is specified by 13.4:0. Otherwise, the data to be written to or read from the register.

5.1.13 1000BASE-T Status Extension 1

Register 15 provides additional information about the operation of the device 1000BASE-T communications. The following table shows the readouts available.

Table 29 • **1000BASE-T Status Extension 1, Address 15 (0x0F)**

Bit	Name	Access	Description	Default
15	1000BASE-X FDX capability	RO	1: PHY is 1000BASE-X FDX capable	0
14	1000BASE-X HDX capability	RO	1: PHY is 1000BASE-X HDX capable	0
13	1000BASE-T FDX capability	RO	1: PHY is 1000BASE-T FDX capable	1
12	1000BASE-T HDX capability	RO	1: PHY is 1000BASE-T HDX capable	1
11:0	Reserved	RO	Reserved	0x000

5.1.14 100BASE-TX Status Extension

Register 16 in the main registers page space of the VSC8512-02 provides additional information about the status of the device's 100BASE-TX operation.

Table 30 • **100BASE-TX Status Extension, Address 16 (0x10)**

Bit	Name	Access	Description	Default
15	100BASE-TX Descrambler	RO	1: Descrambler locked.	0
14	100BASE-TX lock error	RO	Self-clearing bit. 1: Lock error detected.	0

Table 30 • **100BASE-TX Status Extension, Address 16 (0x10)** *(continued)*

Bit	Name	Access	Description	Default
13	100BASE-TX disconnect state	RO	Self-clearing bit. 1: PHY 100BASE-TX link disconnect detected.	0
12	100BASE-TX current link status	RO	1: PHY 100BASE-TX link active.	0
11	100BASE-TX receive error	RO	Self-clearing bit. 1: Receive error detected.	0
10	100BASE-TX transmit error	RO	Self-clearing bit. 1: Transmit error detected.	0
9	100BASE-TX SSD error	RO	Self-clearing bit. 1: Start-of-stream delimiter error detected.	0
8	100BASE-TX ESD error	RO	Self-clearing bit. 1: End-of-stream delimiter error detected.	0
7:0	Reserved	RO	Reserved	

5.1.15 1000BASE-T Status Extension 2

The second status extension register is at address 17 in the device main registers space. It provides information about another set of parameters associated with 1000BASE-T communications. For information about the first status extension register, see Table 29, page 46.

Table 31 • **1000BASE-T Status Extension 2, Address 17 (0x11)**

Bit	Name	Access	Description	Default
15	1000BASE-T descrambler	RO	1: Descrambler locked.	0
14	1000BASE-T lock error	RO	Self-clearing bit. 1: Lock error detected.	0
13	1000BASE-T disconnect state	RO	Self-clearing bit. 1: PHY 1000BASE-T link disconnect detected.	0
12	1000BASE-T current link status	RO	1: PHY 1000BASE-T link active.	0
11	1000BASE-T receive error	RO	Self-clearing bit. 1: Receive error detected.	0
10	1000BASE-T transmit error	RO	Self-clearing bit. 1: Transmit error detected.	0
9	1000BASE-T SSD error	RO	Self-clearing bit. 1: Start-of-stream delimiter error detected.	0
8	1000BASE-T ESD error	RO	Self-clearing bit. 1: End-of-stream delimiter error detected.	0
7	1000BASE-T carrier extension error	RO	Self-clearing bit. 1: Carrier extension error detected.	0
6	Non-compliant BCM5400 detected	RO	1: Non-compliant BCM5400 link partner detected.	0
5	MDI crossover error	RO	1: MDI crossover error was detected.	0

Table 31 •   **1000BASE-T Status Extension 2, Address 17 (0x11)** *(continued)*

Bit	Name	Access	Description	Default
4:0	Reserved	RO	Reserved	

5.1.16   Bypass Control

The bits in this register control aspects of functionality in effect when the device is disabled for the purpose of traffic bypass. The following table shows the settings available.

Table 32 •   **Bypass Control, Address 18 (0x12)**

Bit	Name	Access	Description	Default
15	Transmit disable	R/W	1: PHY transmitter disabled.	0
14	4B5B encoder/decoder	R/W	1: Bypass 4B/5B encoder/decoder.	0
13	Scrambler	R/W	1: Bypass scrambler.	0
12	De-scrambler	R/W	1: Bypass de-scrambler.	0
11	PCS receive	R/W	1: Bypass PCS receiver.	0
10	PCS transmit	R/W	1: Bypass PSC transmit.	0
9	LFI timer	R/W	1: Bypass Link Fail Inhibit (LFI) timer.	0
8	Reserved	RO	Reserved.	
7	HP Auto-MDIX at forced 10/100	R/W	Sticky bit. 1: Disable HP Auto-MDIX at forced 10/100 speeds.	1
6	Non-compliant BCM5400 detect disable	R/W	Sticky bit. 1: Disable non-compliant BCM5400 detection.	0
5	Disable pair swap correction (HP Auto-MDIX when autonegotiation enabled)	R/W	Sticky bit. 1: Disable the automatic pair swap correction.	0
4	Disable polarity correction	R/W	Sticky bit. 1: Disable polarity inversion correction on each subchannel.	0
3	Parallel detect control	R/W	Sticky bit. 1: Do not ignore advertised ability. 0: Ignore advertised ability.	1
2	Pulse shaping filter	R/W	1: Disable pulse shaping filter	0
1	Disable automatic 1000BASE-T next page exchange	R/W	Sticky bit. 1: Disable automatic 1000BASE-T next page exchanges.	0
0	Reserved	RO	Reserved.	

Note: If bit 18.1 is set to 1 in this register, automatic exchange of next pages is disabled, and control is returned to the user through the SMI after the base page is exchanged. The user then must send the correct sequence of next pages to the link partner, determine the common capabilities, and force the device into the correct configuration following the successful exchange of pages.

5.1.17 Error Counter 1

The bits in register 19 provide an error counter. The following table shows the settings available.

Table 33 • **Extended Control and Status, Address 19 (0x13)**

Bit	Name	Access	Description	Default
15:8	Reserved	RO	Reserved.	
7:0	100/1000BASE-TX receive error counter	RO	8-bit counter that saturates when it reaches 255. These bits are self-clearing when read.	0x00

5.1.18 Error Counter 2

The bits in register 20 provide an error counter. The following table shows the settings available.

Table 34 • **Extended Control and Status, Address 20 (0x14)**

Bit	Name	Access	Description	Default
15:8	Reserved	RO	Reserved.	
7:0	100/1000BASE-TX false carrier counter	RO	8-bit counter that saturates when it reaches 255. These bits are self-clearing when read.	0x00

5.1.19 Error Counter 3

The bits in register 21 provide an error counter. The following table shows the settings available.

Table 35 • **Extended Control and Status, Address 21 (0x15)**

Bit	Name	Access	Description	Default
15:8	Reserved	RO	Reserved.	
7:0	Copper media link disconnect counter	RO	8-bit counter that saturates when it reaches 255. These bits are self-clearing when read.	0x00

5.1.20 Extended Control and Status

The bits in register 22 provide additional device control and readouts. The following table shows the settings available.

Table 36 • **Extended Control and Status, Address 22 (0x16)**

Bit	Name	Access	Description	Default
15	Force 10BASE-T link high	R/W	Sticky bit. 1: Bypass link integrity test. 0: Enable link integrity test.	0
14	Jabber detect disable	R/W	Sticky bit. 1: Disable jabber detect.	0
13	Disable 10BASE-T echo	R/W	Sticky bit. 1: Disable 10BASE-T echo.	1
12	Disable SQE mode	R/W	Sticky bit. 1: Disable SQE mode.	1

Table 36 • **Extended Control and Status, Address 22 (0x16)** *(continued)*

Bit	Name	Access	Description	Default
11:10	10BASE-T squelch control	R/W	Sticky bit. 00: Normal squelch. 01: Low squelch. 10: High squelch. 11: Reserved.	00
9	Sticky reset enable	R/W	Super-sticky bit. 1: Enabled.	1
8	EOF Error	RO	This bit is self-clearing. 1: EOF error detected.	0
7	10BASE-T disconnect state	RO	This bit is self-clearing. 1: 10BASE-T link disconnect detected.	0
6	10BASE-T link status	RO	1: 10BASE-T link active.	0
5:1	Reserved	RO	Reserved.	
0	SMI broadcast write	R/W	Sticky bit. 1: Enabled.	0

The following information applies to the extended control and status bits:

- When bit 22.15 is set, the link integrity state machine is bypassed and the PHY is forced into a link pass status.
- When bits 22.11:10 are set to 00, the squelch threshold levels are based on the IEEE standard for 10BASE-T. When set to 01, the squelch level is decreased, which can improve the bit error rate performance on long loops. When set to 10, the squelch level is increased and can improve the bit error rate in high-noise environments.
- When bit 22.9 is set, all sticky register bits retain their values during a software reset. Clearing this bit causes all sticky register bits to change to their default values upon software reset. Super-sticky bits retain their values upon software reset regardless of the setting of bit 22.9.
- When bit 22.0 is set, if a write to any PHY register (registers 0–31, including extended registers), the same write is broadcast to all PHYs. For example, if bit 22.0 is set to 1 and a write to PHY0 is executed (register 0 is set to 0x1040), all PHYs' register 0s are set to 0x1040. Disabling this bit restores normal PHY write operation. Reads are still possible when this bit is set, but the value that is read corresponds only to the particular PHY being addressed.

5.2 Extended PHY Control 1

The following table shows the settings available.

Table 37 • **Extended PHY Control 1, Address 23 (0x17)**

Bit	Name	Access	Description	Default
15:13	Reserved	RO	Reserved.	110

12	MAC interface mode	R/W	Super-sticky bit.
			0: SGMII
			1: 1000BASE-X
			    Note: Register 19G.15:14 = 01 for this
			        selection to be valid.
				0

11	AMS preference	R/W	Super-sticky bit.
			1: Cat5 copper preferred
			0: SerDes fiber/SFP preferred
			    Note: Register 19G.15:14 = 10 for this
			        selection to be valid.
				0

Table 37 • **Extended PHY Control 1, Address 23 (0x17)** *(continued)*

Bit	Name	Access	Description	Default
10:8	Media operating mode	R/W	Super-sticky bits. 000: Cat5 copper only. 001: SerDes fiber/SFP protocol transfer mode only. 010: 1000BASE-X fiber/SFP media only with autonegotiation performed by the PHY. 011: 100BASE-FX fiber/SFP on the fiber media pins only. 101: Automatic media-sense (AMS) with Cat5 media or SerDes fiber/SFP protocol transfer mode. 110: AMS with Cat5 media or 1000BASE-X fiber/SFP media with autonegotiation performed by PHY. 111: AMS with Cat5 media or 100BASE-FX fiber/SFP media. 100: AMS. **Note:** Register 19G.15:14 = 10 for the any of the fiber media selections to be valid.	000
7:6	Force AMS override	R/W	00: Normal AMS selection 01: Force AMS to select SerDes media only 10: Force AMS to select copper media only 11: Reserved **Note:** Register 19G.15:14 = 10 for this selection to be valid.	00
5:4	Reserved	RO	Reserved.	
3	Far-end loopback mode	R/W	1: Enabled.	0
2:0	Reserved	RO	Reserved.	

Note: After configuring bits 13:8 of the extended PHY control register set 1, a software reset (register 0, bit 15) must be written to change the device operating mode. On read, these bits only indicate the actual operating mode and not the pending operating mode setting before a software reset has taken place.

5.2.1 Extended PHY Control 2

The second set of extended controls is located in register 24 in the main register space for the device. The following table shows the settings and readouts available.

Table 38 • **Extended PHY Control 2, Address 24 (0x18)**

Bit	Name	Access	Description	Default
15:13	100BASE-TX edge rate control	R/W	Sticky bit. 011: +5 Edge rate (slowest). 010: +4 Edge rate. 001: +3 Edge rate. 000: +2 Edge rate. 111: +1 Edge rate. 110: Default edge rate. 101: –1 Edge rate. 100: –2 Edge rate (fastest).	000
12	PICMG 2.16 reduced power mode	R/W	Sticky bit. 1: Enabled.	0
11:6	Reserved	RO	Reserved.	

Table 38 • **Extended PHY Control 2, Address 24 (0x18)** *(continued)*

Bit	Name	Access	Description	Default
5:4	Jumbo packet mode	R/W	Sticky bit. 00: Normal IEEE 1.5 kB packet length. 01: 9 kB jumbo packet length (12 kB with 60 ppm or better reference clock). 10: 12 kB jumbo packet length (16 kB with 70 ppm or better reference clock). 11: Reserved.	00
3:1	Reserved	RO	Reserved.	
0	1000BASE-T connector loopback	R/W	1: Enabled.	0

Note: When bits 5:4 are set to jumbo packet mode, the default maximum packet values are based on 100 ppm driven reference clock to the device. Controlling the ppm offset between the MAC and the PHY as specified in the bit description results in a higher jumbo packet length.

5.2.2 Interrupt Mask

These bits control the device interrupt mask. The following table shows the settings available.

Table 39 • **Interrupt Mask, Address 25 (0x19)**

Bit	Name	Access	Description	Default
15	MDINT interrupt status enable	R/W	Sticky bit. 1: Enabled.	0
14	Speed state change mask	R/W	Sticky bit. 1: Enabled.	0
13	Link state change mask	R/W	Sticky bit. 1: Enabled.	0
12	FDX state change mask	R/W	Sticky bit. 1: Enabled.	0
11	Autonegotiation error mask	R/W	Sticky bit. 1: Enabled.	0
10	Autonegotiation complete mask	R/W	Sticky bit. 1: Enabled.	0
9	Inline powered device (PoE) detect mask	R/W	Sticky bit. 1: Enabled.	0
8	Symbol error interrupt mask	R/W	Sticky bit. 1: Enabled.	0
7	Fast link failure interrupt mask	R/W	Sticky bit. 1: Enabled.	0
6	TX FIFO over/underflow interrupt mask	R/W	Sticky bit. 1: Enabled.	0
5	RX FIFO over/underflow interrupt mask	R/W	Sticky bit. 1: Enabled.	0
4	AMS media changed mask	R/W	Sticky bit. 1: Enabled.	0
3	False-carrier interrupt mask	R/W	Sticky bit. 1: Enabled.	0

Table 39 • **Interrupt Mask, Address 25 (0x19)** *(continued)*

Bit	Name	Access	Description	Default
2	Link speed downshift detect mask	R/W	Sticky bit. 1: Enabled.	0
1	Master/Slave resolution error mask	R/W	Sticky bit. 1: Enabled.	0
0	RX_ER interrupt mask	R/W	Sticky bit. 1: Enabled.	0

Note: When bit 25.15 is set, the MDINT pin is enabled. When enabled, the state of this pin reflects the state of bit 26.15. Clearing this bit only inhibits the MDINT pin from being asserted. Also, before enabling this bit, read register 26 to clear any previously inactive interrupts pending that will cause bit 25.15 to be set.

5.2.3   Interrupt Status

The status of interrupts already written to the device are available for reading from register 26 in the main registers space. The following table shows the expected readouts.

Table 40 • **Interrupt Status, Address 26 (0x1A)**

Bit	Name	Access	Description	Default
15	Interrupt status	RO	Self-clearing bit. 1: Interrupt pending.	0
14	Speed state change status	RO	Self-clearing bit. 1: Interrupt pending.	0
13	Link state change status	RO	Self-clearing bit. 1: Interrupt pending.	0
12	FDX state change status	RO	Self-clearing bit. 1: Interrupt pending.	0
11	Autonegotiation error status	RO	Self-clearing bit. 1: Interrupt pending.	0
10	Autonegotiation complete status	RO	Self-clearing bit. 1: Interrupt pending.	0
9	Inline powered device detect status	RO	Self-clearing bit. 1: Interrupt pending.	0
8	Symbol error status	RO	Self-clearing bit. 1: Interrupt pending.	0
7	Fast link failure detect status	RO	Self-clearing bit. 1: Interrupt pending.	0
6	TX FIFO over/underflow detect status	RO	Self-clearing bit. 1: Interrupt pending.	0
5	RX FIFO over/underflow detect status	RO	Self-clearing bit. 1: Interrupt pending.	0
4	AMS media changed mask	RO	Self-clearing bit. 1: Interrupt pending.	0
3	False-carrier interrupt status	RO	Self-clearing bit. 1: Interrupt pending.	0
2	Link speed downshift detect status	RO	Self-clearing bit. 1: Interrupt pending.	0

Table 40 • **Interrupt Status, Address 26 (0x1A)** *(continued)*

Bit	Name	Access	Description	Default
1	Master/Slave resolution error status	RO	Self-clearing bit. 1: Interrupt pending.	0
0	RX_ER interrupt status	RO	Self-clearing bit. 1: Interrupt pending.	0

The following information applies to the interrupt status bits:

- All set bits in this register are cleared after being read (self-clearing). If bit 26.15 is set, the cause of the interrupt can be read by reading bits 26.14:0.
- For bits 26.14 and 26.12, bit 0.12 must be set for this interrupt to assert.
- For bit 26.2, bits 4.8:5 must be set for this interrupt to assert.
- For bit 26.0, this interrupt will not occur when RX_ER is used for carrier-extension decoding of a link partner's data transmission.

5.2.4 Device Auxiliary Control and Status

Register 28 provides control and status information for several device functions not controlled or monitored by other device registers. The following table shows the settings available and the expected readouts.

Table 41 • **Auxiliary Control and Status, Address 28 (0x1C)**

Bit	Name	Access	Description	Default
15	Autonegotiation complete	RO	Duplicate of bit 1.5.	0
14	Autonegotiation disabled	RO	Inverted duplicate of bit 0.12.	0
13	HP Auto-MDIX crossover indication	RO	1: HP Auto-MDIX crossover performed internally.	0
12	CD pair swap	RO	1: CD pairs are swapped.	0
11	A polarity inversion	RO	1: Polarity swap on pair A.	0
10	B polarity inversion	RO	1: Polarity swap on pair B.	0
9	C polarity inversion	RO	1: Polarity swap on pair C.	0
8	D polarity inversion	RO	1: Polarity swap on pair D.	0
7	ActiPHY link status time-out control [1]	R/W	Sticky bit. Bits 7 and 2 are part of the ActiPHY Link Status time-out control. Bit 7 is the MSB. 00: 1 second. 01: 2 seconds. 10: 3 seconds. 11: 4 seconds.	0
6	ActiPHY mode enable	R/W	Sticky bit. 1: Enabled.	0
5	FDX status	RO	1: Full-duplex. 0: Half-duplex.	00
4:3	Speed status	RO	00: Speed is 10BASE-T. 01: Speed is 100BASE-TX or 100BASE-FX. 10: Speed is 1000BASE-T or 1000BASE-X. 11: Reserved.	0

Table 41 • **Auxiliary Control and Status, Address 28 (0x1C)** *(continued)*

Bit	Name	Access	Description	Default
2	ActiPHY link status time-out control [0]	R/W	Sticky bit. Bits 7 and 2 are part of the ActiPHY Link Status time-out control. Bit 7 is the MSB. 00: 1 second. 01: 2 seconds. 10: 3 seconds. 11: 4 seconds.	1
1:0	Media mode status	RO	00: No media selected. 01: Copper media selected. 10: SerDes media selected. 11: Reserved.	00

5.2.5 LED Mode Select

The device LED outputs are controlled using the bits in register 29 of the main register space. The following table shows the information needed to access the functionality of each of the outputs. For more information about LED modes, see Table 8, page 23. For information about enabling the extended LED mode bits in Register 19E1 bits 13 to 12, see Table 9, page 24.

Table 42 • **LED Mode Select, Address 29 (0x1D)**

Bit	Name	Access	Description	Default
15:12	LED3 mode select	R/W	Sticky bit. Select from LED modes 0–15.	1000
11:8	LED2 mode select	R/W	Sticky bit. Select from LED modes 0–15.	0000
7:4	LED1 mode select	R/W	Sticky bit. Select from LED modes 0–15.	0010
3:0	LED0 mode select	R/W	Sticky bit. Select from LED modes 0–15.	0001

5.2.6 LED Behavior

The bits in register 30 control and enable you to read the status of the pulse or blink rate of the device LEDs. The following table shows the settings you can write to the register or read from the register.

Table 43 • **LED Behavior, Address 30 (0x1E)**

Bit	Name	Access	Description	Default
15:13	Reserved	RO	Reserved.	
12	LED pulsing enable	R/W	Sticky bit. 0: Normal operation. 1: LEDs pulse with a 5 kHz, programmable duty cycle when active.	0
11:10	LED blink/pulse-stretch rate	R/W	Sticky bit. 00: 2.5 Hz blink rate/400 ms pulse-stretch. 01: 5 Hz blink rate/200 ms pulse-stretch. 10: 10 Hz blink rate/100 ms pulse-stretch. 11: 20 Hz blink rate/50 ms pulse-stretch. The blink rate selection for PHY0 globally sets the rate used for all LED pins on all PHY ports.	01
9:7	Reserved	RO	Reserved.	
6	LED1 pulse-stretch/blink select	R/W	Sticky bit. 1: Pulse-stretch. 0: Blink.	0

Table 43 • **LED Behavior, Address 30 (0x1E)** *(continued)*

Bit	Name	Access	Description	Default
5	LED0 pulse-stretch/blink select	R/W	Sticky bit. 1: Pulse-stretch. 0: Blink.	0
4:2	Reserved	RO	Reserved.	
1	LED1 combine feature disable	R/W	Sticky bit. 0: Combine enabled (link/activity, duplex/collision). 1: Disable combination (link only, duplex only).	0
0	LED0 combine feature disable	R/W	Sticky bit. 0: Combine enabled (link/activity, duplex/collision). 1: Disable combination (link only, duplex only).	0

Note: Bits 30.11:10 are active only in port 0 and affect the behavior of LEDs for all the ports.

5.2.7 Extended Page Access

To provide functionality beyond the IEEE 802.3-specified registers and main device registers, the VSC8512-02 includes an extended set of registers that provide an additional 15 register spaces.

The register at address 31 controls the access to the extended registers for the VSC8512-02. Accessing the GPIO page register space is similar to accessing the extended page registers. The following table shows the settings available.

Table 44 • **Extended/GPIO Page Access, Address 31 (0x1F)**

Bit	Name	Access	Description	Default
15:0	Extended/GPIO page register access	R/W	0x0000: Register 16–30 accesses main register space. Writing 0x0000 to register 31 restores the main register access. 0x0001: Register 16–30 accesses extended register space 1 0x0002: Register 16–30 accesses extended register space 2 0x0003: Register 16–30 accesses extended register space 3 0x0010: Register 0–30 accesses GPIO register space	0x0000

5.3 Extended Page 1 Registers

To access the extended page 1 registers (16E1–30E1), enable extended register access by writing 0x0001 to register 31. Writing 0x0000 to register 31 restores the main register access.

When extended page 1 register access is enabled, reads and writes to registers 16–30 affect the extended registers 16E1–30E1 instead of those same registers in the IEEE-specified register space. Registers 0–15 are not affected by the state of the extended page register access.

Table 45 • **Extended Registers Page 1 Space**

Address	Name
16E1	SerDes Media Control
17E1	Reserved

Table 45 • **Extended Registers Page 1 Space** *(continued)*

Address	Name
18E1	Cu Media CRC Good Counter
19E1	Extended Mode Control (SerDes loopback and SIGDET control)
20E1	Extended PHY Control 3 (ActiPHY)
21E1–22E1	Reserved
23E1	Extended PHY Control 4 (PoE and CRC error counter)
27E1–28E1	Reserved
29E1	Ethernet Packet Generator (EPG) Control 1
30E1	EPG Control 2

5.3.1   SerDes Media Control

Register 16E1 controls some functions of the SerDes media interface on ports 8-11. These settings are only valid for those ports. The following table shows the setting available in this register.

Table 46 • **SerDes Media Control, Address 16E1 (0x10)**

Bit	Name	Access	Description	Default
15:14	Transmit remote fault	R/W	Remote fault indication sent to link partner (LP)	00
13:12	Link partner (LP) remote fault	RO	Remote fault bits sent by LP during autonegotiation	00
11:10	Reserved	RO	Reserved	
9	Allow 1000BASE-X link-up	R/W	Sticky bit. 1: Allow 1000BASE-X fiber media link-up capability 0: Suppress 1000BASE-X fiber media link-up capability	1
8	Allow 100BASE-FX link-up	R/W	Sticky bit. 1: Allow 100BASE-FX fiber media link-up capability 0: Suppress 100BASE-FX fiber media link-up capability	1
7	Reserved	RO	Reserved	
6	Far end fault detected in 100BASE-FX	RO	Self-clearing bit. 1: Far end fault in 100BASE-FX detected	0
5:0	Reserved	RO	Reserved	

5.3.2 Cu Media CRC Good Counter

Register 18E1 makes it possible to read the contents of the CRC good counter for packets that are received on the Cu media interface; the number of CRC routines that have executed successfully. The following table shows the expected readouts.

Table 47 • **Cu Media CRC Good Counter, Address 18E1 (0x12)**

Bit	Name	Access	Description	Default
15	Packet since last read	RO	Self-clearing bit. 1: Packet received since last read.	0
14	Reserved	RO	Reserved.	
13:0	Cu Media CRC good counter contents	RO	Self-clearing counter containing the number of packets with valid CRCs modulo 10,000. This counter does not saturate and will roll over to 0 on the next good packet received after 9,999.	0x0000

5.3.3 Extended Mode Control

Register 19E1 controls the extended LED and other chip modes. The following table shows the settings available.

Table 48 • **Extended Mode Control, Address 19E1 (0x13)**

Bit	Name	Access	Description	Default
15	LED3 Extended Mode	R/W	1: See Extended LED Modes, page 24.	0
14	LED2 Extended Mode	R/W	1: See Extended LED Modes, page 24.	0
13	LED1 Extended Mode	R/W	1: See Extended LED Modes, page 24.	0
12	LED0 Extended Mode	R/W	1: See Extended LED Modes, page 24.	0
11	LED Reset Blink Suppress	R/W	1: Blink LEDs after COMA_MODE is deasserted. 0: Suppress LED blink after COMA_MODE is deasserted.	0
10:4	Reserved	RO	Reserved	0
3:2	Force MDI crossover	R/W	00: Normal HP Auto-MDIX operation. 01: Reserved. 10: Copper media forced to MDI. 11: Copper media forced MDI-X.	00
1	Reserved	RO	Reserved	
0	SFP[3:0]_SD pin polarity	R/W	1: Active low. 0: Active high.	0

5.3.4   ActiPHY Control

Register 20E1 controls the device ActiPHY sleep timer, its wake-up timer, the frequency of the CLKOUT signal, and its link speed downshifting feature. The following table shows the settings available.

Table 49 •   **Extended PHY Control 3, Address 20E1 (0x14)**

Bit	Name	Access	Description	Default
15	Disable carrier extension	R/W	1: Disable carrier extension in SGMII-1000BASE-T copper links.	1
14:13	ActiPHY sleep timer	R/W	Sticky bit. 00: 1 second. 01: 2 seconds. 10: 3 seconds. 11: 4 seconds.	01
12:11	ActiPHY wake-up timer	R/W	Sticky bit. 00: 160 ms. 01: 400 ms. 10: 800 ms. 11: 2 seconds.	00
10	Reserved	RO	Reserved	
9	PHY address reversal	R/W	1: Enabled	Address
8	Reserved	RO	Valid only on PHY0.	
7:6	Media mode status	RO	00: No media selected. 01: Copper media selected. 10: SerDes media selected. 11: Reserved.	00
5	Enable 10BASE-T no preamble mode	R/W	Sticky bit. 1: 10BASE-T will assert RX_DV indication when data is presented to the receiver even without a preamble preceding it.	0
4	Enable link speed auto-downshift feature	R/W	Sticky bit. 1: Enable auto link speed downshift from 1000BASE-T.	0
3:2	Link speed auto downshift control	R/W	Sticky bit. 00: Downshift after 2 failed 1000BASE-T autonegotiation attempts. 01: Downshift after 3 failed 1000BASE-T autonegotiation attempts. 10: Downshift after 4 failed 1000BASE-T autonegotiation attempts. 11: Downshift after 5 failed 1000BASE-T autonegotiation attempts.	01
1	Link speed auto downshift status	RO	0: No downshift. 1: Downshift is required or has occurred.	0
0	Reserved	RO	Reserved	

5.3.5 PoE and Miscellaneous Functionality

The register at address 23E1 controls various aspects of inline powering and the CRC error counter in the VSC8512-02.

Table 50 • **Extended PHY Control 4, Address 23E1 (0x17)**

Bit	Name	Access	Description	Default
15:11	PHY address	RO	PHY address; latched on reset.	
10	Inline powered device detection	R/W	Sticky bit. 1: Enabled.	0
9:8	Inline powered device detection status	RO	Only valid when bit 10 is set. 00: Searching for devices. 01: Device found; requires inline power. 10: Device found; does not require inline power. 11: Reserved.	00
7:0	Cu Media CRC error counter	RO	Self-clearing bit. RC error counter for packets received on the Cu media interface. The value saturates at 0xFF and subsequently clears when read and restarts count.	0x00

5.3.6 Ethernet Packet Generator Control 1

The EPG control register provides access to and control of various aspects of the EPG testing feature. There are two separate EPG control registers. The following table shows the settings available in the first register.

Table 51 • **EPG Control 1, Address 29E1 (0x1D)**

Bit	Name	Access	Description	Default
15	EPG enable	R/W	1: Enable EPG	0
14	EPG run or stop	R/W	1: Run EPG	0
13	Transmission duration	R/W	1: Continuous (sends in 10,000-packet increments) 0: Send 30,000,000 packets and stop	0
12:11	Packet length	R/W	00: 125 bytes 01: 64 bytes 10: 1518 bytes 11: 10,000 bytes (jumbo packet)	0
10	Inter-packet gap	R/W	1: 8,192 ns 0: 96 ns	0
9:6	Destination address	R/W	Lowest nibble of the 6-byte destination address	0001
5:2	Source address	R/W	Lowest nibble of the 6-byte destination address	0000
1	Payload type	R/W	1: Randomly generated payload pattern 0: Fixed based on payload pattern	0
0	Bad frame check sequence (FCS) generation	R/W	1: Generate packets with bad FCS 0: Generate packets with good FCS	0

The following information applies to the EPG control number 1:

- Do not run the EPG when the VSC8512-02 is connected to a live network.
- Bit 29E1.13 (continuous EPG mode control): When enabled, this mode causes the device to send continuous packets. When disabled, the device continues to send packets only until it reaches the next 10,000-packet increment mark. It then ceases to send packets.
- The 6-byte destination address in bits 9:6 is assigned one of 16 addresses in the range of 0xFF FF FF FF FF F0 through 0xFF FF FF FF FF FF.
- The 6-byte source address in bits 5:2 is assigned one of 16 addresses in the range of 0xFF FF FF FF FF F0 through 0xFF FF FF FF FF FF.
- If any of bits 13:0 are changed while the EPG is running (bit 14 is set to 1), bit 14 must be cleared and then set back to 1 for the change to take effect and to restart the EPG.

5.3.7   Ethernet Packet Generator Control 2

Register 30E1 consists of the second set of bits that provide access to and control over the various aspects of the EPG testing feature. The following table shows the settings available.

Table 52 •   **EPG Control 2, Address 30E1 (0x1E)**

Bit	Name	Access	Description	Default
15:0	EPG packet payload	R/W	Data pattern repeated in the payload of packets generated by the EPG	0x00

Note: If any of bits 15:0 in this register are changed while the EPG is running (bit 14 of register 29E1 is set to 1), that bit (29E1.14) must first be cleared and then set back to 1 for the change to take effect and to restart the EPG.

5.4   Extended Page 2 Registers

To access the extended page 2 registers (16E2–30E2), enable extended register access by writing 0x0002 to register 31. For more information, see Table 44, page 56.

When extended page 2 register access is enabled, reads and writes to registers 16–30 affect the extended registers 16E2–30E2 instead of those same registers in the IEEE-specified register space. Registers 0–15 are not affected by the state of the extended page register access.

Writing 0x0000 to register 31 restores the main register access.

The following table lists the addresses and register names in the extended register page 2 space. These registers are accessible only when the device register 31 is set to 0x0002.

Table 53 •   **Extended Registers Page 2 Space**

Address	Name
16E2	Cu PMD Transmit Control
17E2	EEE Control
18E2–30E2	Reserved

5.4.1   Cu PMD Transmit Control

The register at address 16E2 consists of the bits that provide control over the amplitude settings for the transmit side Cu PMD interface. These bits provide the ability to make small adjustments in the signal amplitude to compensate for minor variations in the magnetics from different vendors. Extreme caution must be exercised when changing these settings from the default values as they have a direct impact on

the signal quality. Changing these settings also affects the linearity and harmonic distortion of the transmitted signals. Contact Microsemi for further help with changing these values.

Table 54 • **Cu PMD Transmit Control, Address 16E2 (0x10)**

Bit	Name	Access	Description	Default
15:12	1000BASE-T signal amplitude trim	R/W	Change 1000BASE-T signal amplitude	0000
11:8	100BASE-TX signal amplitude trim	R/W	Change 100BASE-TX signal amplitude	0010
7:4	10BASE-T signal amplitude trim	R/W	Change 10BASE-T signal amplitude	1111
3:0	10BASE-Te signal amplitude trim	R/W	Change 10BASE-Te signal amplitude	0000

5.4.2 EEE Control

The register at address 17E2 consists of the bits that provide additional control over the chip behavior in Energy Efficient Ethernet (IEEE 802.3az) mode for debug and to allow interoperation with legacy MACs that do not support IEEE 802.3az.

Table 55 • **EEE Control, Address 17E2 (0x11)**

Bit	Name	Access	Description	Default
15	Enable 10BASE-Te	R/W	Enable Energy Efficient (IEEE 802.3az) 10BASE-Te operating mode.	0
14	Enable LED in fiber unidirectional mode	R/W	1: Enable LED functions in fiber unidirectional mode.	0
13:10	Invert LED polarity	R/W	Invert polarity of LED[3:0] signals. Default is to drive an active low signal on the LED pins. This also applies to enhanced serial LED mode. For more information, see Enhanced Serial LED Mode, page 26.	0000
9:6	Reserved	R/O	Reserved.	
5	Enable 1000BASE-T force mode	R/W	1: Enable 1000BASE-T force mode to allow PHY to link up in 1000BASE-T mode without forcing master/slave when register 0, bits 6 and 13 are set to 2'b10.	0
4	Force transmit LPI	R/W	1: Enable the EPG to transmit LPI on the MDI instead of normal idles when receiving normal idles from the MAC. 0: Transmit idles being received from the MAC.	0
3	Inhibit 100BASE-TX transmit EEE LPI	R/W	1: Disable transmission of EEE LPI on transmit path MDI in 100BASE-TX mode when receiving LPI from MAC.	0
2	Inhibit 100BASE-TX receive EEE LPI	R/W	1: Disable transmission of EEE LPI on receive path MAC interface in 100BASE-TX mode when receiving LPI from the MDI.	0
1	Inhibit 1000BASE-T transmit EEE LPI	R/W	1: Disable transmission of EEE LPI on transmit path MDI in 1000BASE-T mode when receiving LPI from MAC.	0

Table 55 • **EEE Control, Address 17E2 (0x11)** *(continued)*

Bit	Name	Access	Description	Default
0	Inhibit 1000BASE-T receive EEE LPI	R/W	1: Disable transmission of EEE LPI on receive path MAC interface in 1000BASE-T mode when receiving LPI from the MDI.	0

5.5 Extended Page 3 Registers

To access the extended page 3 registers (16E3–30E3), enable extended register access by writing 0x0003 to register 31. For more information, see Table 44, page 56.

When extended page 3 register access is enabled, reads and writes to registers 16–30 affect the extended registers 16E3–30E3 instead of those same registers in the IEEE-specified register space. Registers 0–15 are not affected by the state of the extended page register access.

Writing 0x0000 to register 31 restores the main register access.

The following table lists the addresses and register names in the extended register page 3 space. These registers are accessible only when the device register 31 is set to 0x0003.

Table 56 • **Extended Registers Page 3 Space**

Address	Name
16E3	MAC SerDes PCS Control
17E3	MAC SerDes PCS Status
18E3	MAC SerDes Clause 37 Advertised Ability
19E3	MAC SerDes Clause 37 Link Partner Ability
20E3	MAC SerDes Status
21E3	Media SerDes Transmit Good Packet Counter
22E3	Media SerDes Transmit CRC Error Counter
23E3	Media SerDes PCS Control
24E3	Media SerDes PCS Status
25E3	Media SerDes Clause 37 Advertised Ability
26E3	Media SerDes Clause 37 Link Partner Ability
27E3	Media SerDes status
28E3	Fiber Media CRC Good Counter
29E3	Fiber Media CRC Error Counter
30E3	Reserved

5.5.1 MAC SerDes PCS Control

The register at address 16E3 consists of the bits that provide access to and control over MAC SerDes PCS block. The following table shows the settings available.

Table 57 • **MAC SerDes PCS Control, Address 16E3 (0x10)**

Bit	Name	Access	Description	Default
15	MAC interface disable	R/W	Sticky bit. 1: 1000BASE-X MAC interface disable when media link down.	0

Table 57 • **MAC SerDes PCS Control, Address 16E3 (0x10)** *(continued)*

Bit	Name	Access	Description	Default
14	MAC interface restart	R/W	Sticky bit. 1: 1000BASE-X MAC interface restart on media link change.	0
13	MAC interface PD enable	R/W	Sticky bit. 1: MAC interface autonegotiation parallel detect enable.	0
12	MAC interface autonegotiation restart	R/W	Self-clearing bit. 1: Restart MAC interface autonegotiation.	0
11	Force advertised ability	R/W	1: Force 16-bit advertised ability from register 18E3.	0
10:8	SGMII preamble control	R/W	000 = No effect on the start of packet. 001 = If both the first two nibbles of the 10/100 packet are not 0x5, a byte of 0x55 must be prefixed to the output, otherwise there will be no effect on the start of packet. 010 = If both the first two nibbles of the 10/100 packet are not 0x5, a byte of 0x55 must be prefixed to the output. An additional byte of 0x55 must be prefixed to the output if the next two nibbles are also not 0x5. 011–111 = Reserved.	001
7	MAC SerDes autonegotiation enable	R/W	1: MAC SerDes ANEG enable.	0
6	SerDes polarity at input of MAC	R/W	1: Invert polarity of signal received at input of MAC.	0
5	SerDes polarity at output of MAC	R/W	1: Invert polarity of signal at output of MAC.	
4	Fast link status enable	R/W	1: Use fast link fail indication as link status indication to MAC SerDes 0: Use normal link status indication to MAC SerDes	0
3	Unidirectional enable	R/W	1: Enable transmit on MAC interface regardless of whether the PHY has determined that a valid link has been established. 0: Enable transmit on MAC interface only when the PHY has determined that a valid link has been established.	0
2:0	Reserved	RO	Reserved.	

5.5.2 MAC SerDes PCS Status

The register at address 17E3 consists of the bits that provide status from the MAC SerDes PCS block. The following table shows the settings available.

Table 58 • **MAC SerDes PCS Status, Address 17E3 (0x11)**

Bit	Name	Access	Description
15:13	Reserved	RO	Reserved

Table 58 • **MAC SerDes PCS Status, Address 17E3 (0x11)** *(continued)*

Bit	Name	Access	Description
12	SGMII alignment error	RO	1: SGMII alignment error occurred
11	MAC interface LP autonegotiation restart	RO	1: MAC interface link partner autonegotiation restart request occurred
10	Reserved	RO	Reserved
9:8	MAC remote fault	RO	01, 10, and 11: Remote fault detected from MAC 00: No remote fault detected from MAC
7	Asymmetric pause advertisement	RO	1: Asymmetric pause advertised by MAC
6	Symmetric pause advertisement	RO	1: Symmetric pause advertised by MAC
5	Full duplex advertisement	RO	1: Full duplex advertised by MAC
4	Half duplex advertisement	RO	1: Half duplex advertised by MAC
3	MAC interface LP autonegotiation capable	RO	1: MAC interface link partner autonegotiation capable
2	MAC interface link status	RO	1: MAC interface link status connected
1	MAC interface autonegotiation complete	RO	1: MAC interface autonegotiation complete
0	MAC interface PCS signal detect	RO	1: MAC interface PCS signal detect present

5.5.3   MAC SerDes Clause 37 Advertised Ability

The register at address 18E3 consists of the bits that provide access to and control over MAC SerDes Clause 37 advertised ability. The following table shows the settings available.

Table 59 • **MAC SerDes CI37 Advertised Ability, Address 18E3 (0x12)**

Bit	Name	Access	Description	Default
15:0	MAC SerDes advertised ability	R/W	Current configuration code word being advertised (this register is read/write if 16E3.11 = 1)	0x0000

5.5.4   MAC SerDes Clause 37 Link Partner Ability

The register at address 19E3 consists of the bits that provide status of the MAC SerDes link partner's Clause 37 advertised ability. The following table shows the settings available.

Table 60 • **MAC SerDes CI37 LP Ability, Address 19E3 (0x13)**

Bit	Name	Access	Description
15:0	MAC SerDes LP ability	RO	Last configuration code word received from link partner

5.5.5 MAC SerDes Status

The register at address 20E3 consists of the bits that provide access to MAC SerDes status. The following table shows the settings available.

Table 61 • **MAC SerDes Status, Address 20E3 (0x14)**

Bit	Name	Access	Description
15	K28.5 comma realignment	RO	Self-clearing bit. 1: a K28.5 comma re-alignment has occurred
14	SerDes signal detect	RO	Self-clearing bit. Sticky bit. 1: SerDes signal detection occurred
13:0	Reserved	RO	Reserved

5.5.6 Media SerDes Transmit Good Packet Counter

The register at address 21E3 consists of the bits that provide status of the media SerDes transmit good packet counter. The following table shows the settings available.

Table 62 • **Media SerDes Tx Good Packet Counter, Address 21E3 (0x15)**

Bit	Name	Access	Description
15	Tx good packet counter active	RO	1: Transmit good packet counter active
14	Reserved	RO	Reserved
13:0	Tx good packet count	RO	Transmit good packet count modulo 10000

5.5.7 Media SerDes Transmit CRC Error Counter

The register at address 22E3 consists of the bits that provide status of the media SerDes transmit packet count that had a CRC error. The following table shows the settings available.

Table 63 • **Media SerDes Tx CRC Error Counter, Address 22E3 (0x16)**

Bit	Name	Access	Description
15:8	Reserved	RO	Reserved
7:0	Tx CRC packet count	RO	Transmit CRC packet count (saturates at 255)

5.5.8 Media SerDes PCS Control

The register at address 23E3 consists of the bits that provide access to and control over Media SerDes PCS control. The following table shows the settings available.

Table 64 • **Media SerDes PCS Control, Address 23E3 (0x17)**

Bit	Name	Access	Description	Default
15:14	Reserved	RO	Reserved	
13	Media interface autonegotiation parallel-detection	R/W	Sticky bit. 1: SerDes media autonegotiation parallel detect enabled	0
12	Reserved	RO	Reserved	
11	Force advertised ability	R/W	1: Force 16-bit advertised ability from register 25E3.15:0	0
10:0	Reserved	RO	Reserved	

5.5.9   Media SerDes PCS Status

The register at address 24E3 consists of the bits that provide status of the Media SerDes PCS block. The following table shows the settings available.

Table 65 •   **Media SerDes PCS Status, Address 24E3 (0x18)**

Bit	Name	Access	Description
15:12	Reserved	RO	Reserved
11	Media interface link partner autonegotiation restart	RO	1: Media interface link partner autonegotiation restart request occurred
10	Reserved	RO	Reserved
9:8	Remote fault detected	RO	01, 10, 11: Remote fault detected from link partner
7	Link partner asymmetric pause	RO	1: Asymmetric pause advertised by link partner
6	Link partner symmetric pause	RO	1: Symmetric pause advertised by link partner
5	Link partner full duplex advertisement	RO	1: Full duplex advertised by link partner
4	Link partner half duplex advertisement	RO	1: Half duplex advertised by link partner
3	Link partner autonegotiation capable	RO	1: Media interface link partner autonegotiation capable
2	Media interface link status	RO	1: Media interface link status
1	Media interface autonegotiation complete	RO	1: Media interface autonegotiation complete
0	Media interface signal detect	RO	1: Media interface signal detect

5.5.10   Media SerDes Clause 37 Advertised Ability

The register at address 25E3 consists of the bits that provide access to and control over Media SerDes Clause 37 advertised ability. The following table shows the settings available.

Table 66 •   **Media SerDes Cl37 Advertised Ability, Address 25E3 (0x19)**

Bit	Name	Access	Description	Default
15:0	Media SerDes advertised ability	R/W	Current configuration code word being advertised. This register is read/write if 23E3.11 = 1.	0x0000

5.5.11   Media SerDes Clause 37 Link Partner Ability

The register at address 26E3 consists of the bits that provide status of the media SerDes link partner's Clause 37 advertised ability. The following table shows the settings available.

Table 67 •   **MAC SerDes Cl37 LP Ability, Address 26E3 (0x1A)**

Bit	Name	Access	Description
15:0	Media SerDes LP ability	RO	Last configuration code word received from link partner

5.5.12 Media SerDes Status

The register at address 27E3 consists of the bits that provide access to Media SerDes status. The following table shows the settings available.

Table 68 • **Media SerDes Status, Address 27E3 (0x1B)**

Bit	Name	Access	Description
15	K28.5 comma realignment	RO	Self-clearing bit. 1: K28.5 comma re-alignment has occurred
14	Signal detect	RO	Self-clearing bit. Sticky bit. 1: SerDes media signal detect
13:0	Reserved	RO	Reserved

5.5.13 Fiber Media CRC Good Counter

Register 28E3 makes it possible to read the contents of the CRC good counter for packets that are received on the Fiber media interface; the number of CRC routines that have executed successfully. The following table shows the expected readouts.

Table 69 • **Fiber Media CRC Good Counter, Address 28E3 (0x1C)**

Bit	Name	Access	Description	Default
15	Packet since last read	RO	Self-clearing bit. 1: Packet received since last read.	0
14	Reserved	RO	Reserved.	
13:0	Fiber media CRC good counter contents	RO	Self-clearing bit. Counter containing the number of packets with valid CRCs. This counter does not saturate and will roll over.	0x000

5.5.14 Fiber Media CRC Error Counter

Register 29E3 makes it possible to read the contents of the CRC error counter for packets that are received on the Fiber media interface. The following table shows the expected readouts.

Table 70 • **Fiber Media CRC Error Counter, Address 29E3 (0x1D)**

Bit	Name	Access	Description	Default
15:8	Reserved	RO	Reserved.	
7:0	Fiber Media CRC error counter	RO	Self-clearing bit. CRC error counter for packets received on the Fiber media interface. The value saturates at 0xFF and subsequently clears when read and restarts count.	0x00

5.6 General Purpose Registers

Accessing the General Purpose register space is similar to accessing the extended page registers. Set register 31 to 0x0010. This sets all 32 registers to the general purpose register space.

To restore main register page access, write 0x0000 to register 31.

The following table lists the addresses and register names in the general purpose register page space. These registers are accessible only when the device register 31 is set to 0x0010.

Table 71 • **General Purpose Registers Page Space**

Address	Name
0G–12G	Reserved
13G	SIGDET/LED vs. GPIO Control
14G	COMA_MODE and CLK_SQUELCH_IN Control
15G	GPIO Input
16G	GPIO Output
17G	GPIO Output Enable
18G	Global Command and SerDes Configuration
19G	MAC Mode and Fast Link Configuration
20G	I2C MUX Control 1
21G	I2C MUX Control 2
22G	I2C MUX Data Read/Write
23G	Recovered Clock 0 Control
24G	Recovered Clock 1 Control
25G	Enhanced LED Control
26G–28G	Reserved
29G	Global Interrupt Status
30G	Reserved

5.6.1 SIGDET/LED vs. GPIO Control

The SIGDET/LED control register configures the multipurpose pins to be either signal detect pins for each fiber media port, or to be general purpose I/O pins. It also controls LED1 pins for PHYs 8, 9, 10, and 11 to be either LED1 pins or GPIO pins. The following table shows the values that can be written.

Table 72 • **SIGDET/LED vs. GPIO Control, Address 13G (0x0D)**

Bit	Name	Access	Description	Default
15:14	GPIO_16 control	R/W	00: LED1 operation for PHY11 01, 10: Reserved 11: GPIO controlled by MII registers 15G–17G	00
13:12	GPIO_15 control	R/W	00: LED1 operation for PHY10 01, 10: Reserved 11: GPIO controlled by MII registers 15G–17G	00
11:10	GPIO_14 control	R/W	00: LED1 operation for PHY9 01, 10: Reserved 11: GPIO controlled by MII registers 15G–17G	00
9:8	GPIO_13 control	R/W	00: LED1 operation for PHY8 01, 10: Reserved 11: GPIO controlled by MII registers 15G–17G	00
7:6	SFP3_SD control	R/W	00: SIGDET operation 01, 10: Reserved 11: GPIO controlled by MII registers 15G–17G	00

Table 72 • **SIGDET/LED vs. GPIO Control, Address 13G (0x0D)** *(continued)*

Bit	Name	Access	Description	Default
5:4	SFP2_SD control	R/W	00: SIGDET operation 01, 10: Reserved 11: GPIO controlled by MII registers 15G–17G	00
3:2	SFP1_SD control	R/W	00: SIGDET operation 01, 10: Reserved 11: GPIO controlled by MII registers 15G–17G	00
1:0	SFP0_SD control	R/W	00: SIGDET operation 01, 10: Reserved 11: GPIO controlled by MII registers 15G–17G	00

5.6.2 COMA_MODE and CLK_SQUELCH_IN Control

Register 14G configures the functionality of the COMA_MODE and CLK_SQUELCH_IN input pins.

Table 73 • **COMA_MODE and CLK_SQUELCH_IN Control, Address 14G (0x0E)**

Bit	Name	Access	Description	Default
15	Reserved	RO	Reserved	
14	Clock squelch input enable	R/W	Configure PHY4_LED1 pin as CLK_SQUELCH_IN and enable clock squelch control from that pin	0
13	COMA_MODE output enable (active low)	R/W	1: COMA_MODE pin is an input 0: COMA_MODE pin is an output	1
12	COMA_MODE output data	R/W	Value to output on the COMA_MODE pin when it is configured as an output	0
11	COMA_MODE input data	RO	Data read from the COMA_MODE pin	
10	Tri-state enable for I2C bus	R/W	1: Tri-state I2C bus output signals instead of driving them high. This allows those signals to be pulled above VDDIO using an external pull-up resistor. 0: Drive I2C bus output signals to high and low values as appropriate	0
9	Tri-state enable for LEDs	R/W	1: Tri-state LED output signals instead of driving them high. This allows those signals to be pulled above VDDIO using an external pull-up resistor. 0: Drive LED bus output signals to high and low values as appropriate.	0
8:0	Reserved	RO	Reserved.	0

5.6.3 GPIO Input

The input register contains information about the input to the device GPIO pins. Read from this register to access the data on the device GPIO pins. The following table shows the readout you can expect.

Table 74 • **GPIO Input, Address 15G (0x0F)**

Bit	Name	Access	Description	Default
15:8	Reserved	RO	Reserved	

Table 74 •   **GPIO Input, Address 15G (0x0F)** *(continued)*

Bit	Name	Access	Description	Default
7:0	GPIO input	RO	Data read from the SFP[3:0]_SD and GPIO[16:13] pins	

5.6.4   GPIO Output

The output register allows you to access and control the output from the device GPIO pins. The following table shows the values you can write.

Table 75 •   **GPIO Output, Address 16G (0x10)**

Bit	Name	Access	Description	Default
15:8	Reserved	RO	Reserved	
7:0	GPIO output	R/W	Data written to the SFP[3:0]_SD and GPIO[16:13] pins	0x00

5.6.5   GPIO Pin Configuration

Register 17G in the GPIO register space controls whether a particular GPIO pin functions as an input or an output. The following table shows the settings available.

Table 76 •   **GPIO Input/Output Configuration, Address 17G (0x11)**

Bit	Name	Access	Description	Default
15:8	Reserved	RO	Reserved	
7:0	SFP[3:0]_SD and GPIO[16:13] pin input or output enable	R/W	1: Pin is configured as an output. 0: Pin is configured as an input.	0x00

5.6.6   Global Command and SerDes Configuration

Register 18G is a command window. Bit 15 tells the internal processor to execute the command. When bit 15 is cleared the command has completed. Software needs to wait until bit 15 = 0 before proceeding with the next PHY register access. The following table lists the values to write to register 18G to execute the various commands.

Table 77 •   **Global Command and SerDes Configuration, Address 18G (0x12)**

Command	Value
Enable 12 PHYs MAC SGMII	0x80B0
Enable 12 PHYs MAC QSGMII	0x80A0
Enable 4 PHYs (PHY8 to PHY11) media 1000BASE-X	0x8F81[1]
Enable 4 PHYs (PHY8 to PHY11) media 100BASE-FX	0x8F91[1]

1. The "F" in the command has a bit representing each of the four PHYs. To exclude a PHY from the configuration, set its bit to 0. For example, the configuration of PHY 3 and PHY 2 to 1000BASE-X would be 1100 or a "C" and the command would be 0x8CC1.

5.6.7 MAC Mode and Fast Link Configuration

Register 19G controls the MAC interface mode and the selection of the source PHY for the fast link failure indication. The following table shows the settings available for the FAST_LINK_STATUS pin.

Table 78 • **MAC Mode and Fast Link Configuration, Address 19G (0x13)**

Bit	Name	Access	Description	Default
15:14	MAC interface mode select for all PHYs in the VSC8512-02	R/W	Select MAC interface mode 00: QSGMII to CAT5 mode 01: SGMII to CAT5 mode 10: QSGMII to CAT5 and Fiber mode 11: Reserved	00
13:4	Reserved	RO	Reserved	
3:0	Fast link failure port setting	R/W	0000: PHY0 0001: PHY1 0010: PHY2 0011: PHY3 0100: PHY4 0101: PHY5 0110: PHY6 0111: PHY7 1000: PHY8 1001: PHY9 1010: PHY10 1011: PHY11 1100–1111: Output disabled	0xF

5.6.8 I2C MUX Control 1

The following table shows the settings available to control the integrated I2C MUX.

Table 79 • **I2C MUX Control 1, Address 20G (0x14)**

Bit	Name	Access	Description	Default
15:9	I2C device address	R/W	Top 7 bits of the 8-bit address sent out on the two wire serial stream. The bottom bit is the read/write signal, which is controlled by register 21G, bit 8. SFPs use 0xA0.	0xA0
8:6	Reserved	RO	Reserved.	
5:4	I2C SCL clock frequency	R/W	00: 50 kHz 01: 100 kHz 10: 400 kHz 11: 2 MHz	01
3	I2C MUX port 3 enable	R/W	1: Enabled. 0: I2C disabled. Becomes PHY5_LED1 pin.	0
2	I2C MUX port 2 enable	R/W	1: Enabled. 0: I2C disabled. Becomes PHY6_LED1 pin.	0
1	I2C MUX port 1 enable	R/W	1: Enabled. 0: I2C disabled. Becomes PHY7_LED1 pin.	0
0	I2C MUX port 0 enable	R/W	0: SFP_SERIALCLK0 1: ESLED_CLK	0

5.6.9 I2C MUX Control 2

Register 21G is used to control the I2C MUX for status and control of I2C slave devices.

Table 80 • **I2C MUX Interface Status and Control, Address 21G (0x15)**

Bit	Name	Access	Description	Default
15	I2C MUX ready	RO	1: I2C MUX is ready for read or write.	
14:12	Reserved	RO	Reserved	
11:10	PHY port Address	R/W	Specific VSC8512-02 PHY port being addressed.	00
9	Enable I2C MUX access	R/W	Self-clearing bit. 1: Execute read or write through the I2C MUX based on the settings of register bit 21G.8.	0
8	I2C MUX read or write	R/W	1: Read from I2C MUX. 0: Write to I2C MUX.	1
7:0	I2C MUX address	R/W	Sets the address of the I2C MUX used to direct read or write operations.	0x00

5.6.10 I2C MUX Data Read/Write

Register 22G in the extended register space enables access to the I2C MUX.

Table 81 • **I2C MUX Data Read/Write, Address 22G (0x16)**

Bit	Name	Access	Description	Default
15:8	I2C MUX read data	RO	Eight-bit data read from I2C MUX; requires setting both register 21G.9 and 21G.8 to 1.	
7:0	I2C MUX write data	R/W	Eight-bit data to be written to I2C MUX.	0x00

5.6.11 Recovered Clock 0 Control

Register 23G in the extended register space controls the functionality of the recovered clock 0 output signal.

Table 82 • **Recovered Clock 0 Control, Address 23G (0x17)**

Bit	Name	Access	Description	Default
15	Enable RCVRD_CLK[0]	R/W	1: Enable recovered clock 0 output 0: Disable recovered clock 0 output	0

Table 82 • **Recovered Clock 0 Control, Address 23G (0x17)** *(continued)*

Bit	Name	Access	Description	Default
14:11	Clock source select	R/W	Select bits for source PHY for recovered clock: 0000: PHY0 0001: PHY1 0010: PHY2 0011: PHY3 0100: PHY4 0101: PHY5 0110: PHY6 0111: PHY7 1000: PHY8 1001: PHY9 1010: PHY10 1011: PHY11 1100–1111: Reserved	0000
10:8	Clock frequency select	R/W	Select output clock frequency: 000: 25 MHz output clock 001: 125 MHz output clock 010: 31.25 MHz output clock 011–111: Reserved	000
7:6	Reserved	RO	Reserved.	
5:4	Clock squelch level	R/W	Select clock squelch level 00: Automatically squelch clock to low when the link is not up, is unstable, is up in a mode that does not support the generation of a recovered clock (1000BASE-T master or 10BASE-T), or is up in EEE mode (100BASE-TX or 1000BASE-T slave). 01: Same as 00 except that the clock is also generated in 1000BASE-T master and 10BASE-T link-up modes. This mode also generates a recovered clock output in EEE mode during reception of LP_IDLE. 10: Squelch only when the link is not up. 11: Disable clock squelch. **Note:** A clock from the SerDes or Cu PHY will be output on the recovered clock output in this mode when the link is down.	
3	Reserved	RO	Reserved.	
2:0	Clock selection for specified PHY	R/W	000: Serial media recovered clock (only valid for PHYs 8, 9, 10, and 11 that support dual-media functionality) 001: Copper PHY recovered clock 010: Copper PHY transmitter TCLK 011–111: Reserved	000

5.6.12 Recovered Clock 1 Control

Register 24G in the extended register space controls the functionality of the recovered clock 1 output signal.

Table 83 • **Recovered Clock 1 Control, Address 24G (0x18)**

Bit	Name	Access	Description	Default
15	Enable RCVRD_CLK[1]	R/W	Enable recovered clock 1 output	0
14:11	Clock source select	R/W	Select bits for source PHY for recovered clock: 0000: PHY0 0001: PHY1 0010: PHY2 0011: PHY3 0100: PHY4 0101: PHY5 0110: PHY6 0111: PHY7 1000: PHY8 1001: PHY9 1010: PHY10 1011: PHY11 1100–1111: Reserved	0000
10:8	Clock frequency select	R/W	Select output clock frequency: 000: 25 MHz output clock 001: 125 MHz output clock 010: 31.25 MHz output clock 011–111: Reserved	000
7:6	Reserved	RO	Reserved.	
5:4	Clock squelch level	R/W	Select clock squelch level: 00: Automatically squelch clock to low when the link is not up, is unstable, is up in a mode that does not support the generation of a recovered clock (1000BASE-T master or 10BASE-T), or is up in EEE mode (100BASE-TX or 1000BASE-T slave). 01: Same as 00 except that the clock is also generated in 1000BASE-T master and 10BASE-T link-up modes. This mode also generates a recovered clock output in EEE mode during reception of LP_IDLE 10: Squelch only when the link is not up 11: Disable clock squelch. **Note:** A clock from the SerDes or Cu PHY will be output on the recovered clock output in this mode when the link is down.	
3	Reserved	RO	Reserved	
2:0	Clock selection for specified PHY	R/W	000: Serial media recovered clock (only valid for PHYs 8, 9, 10, and 11 that support dual-media functionality). 001: Copper PHY recovered clock 010–111: Reserved.	000

5.6.13 Enhanced LED Control

The following table contains the bits to control advanced functionality of the parallel and serial LED signals.

Table 84 • **Enhanced LED Control, Address 25G (0x19)**

Bit	Name	Access	Description	Default
15:8	LED pulsing duty cycle control	R/W	Programmable control for LED pulsing duty cycle when bit 30.12 is set to 1. Valid settings are between 0 and 198. A setting of 0 corresponds to a 0.5% duty cycle and 198 corresponds to a 99.5% duty cycle. Intermediate values change the duty cycle in 0.5% increments	00
7	Serial LED output 2 enable	R/W	Enable the serial LED output functionality for GPIO_5, GPIO_6, GPIO_7, and GPIO_8 pins 1: Pins function as serial LED outputs 0: Pins retain their normal function	0
6	Serial LED output 1 enable	R/W	Enable the serial LED output functionality for GPIO_[3:0] pins 1: Pins function as serial LED outputs 0: Pins retain their normal function	0
5:3	Serial LED frame rate selection	R/W	Select frame rate of serial LED stream 000: 2500 Hz frame rate 001: 1000 Hz frame rate 010: 500 Hz frame rate 011: 250 Hz frame rate 100: 200 Hz frame rate 101: 125 Hz frame rate 110: 40 Hz frame rate 111: Output basic serial LED stream. See Table 10, page 25.	
2:1	Serial LED select	R/W	Select which LEDs from each PHY to enable on the serial stream 00: Enable all 4 LEDs of each PHY 01: Enable LEDs 2, 1 and 0 of each PHY 10: Enable LEDs 1 and 0 of each PHY 11: Enable LED 0 of each PHY	00
0	LED port swapping	R/W	See LED Port Swapping, page 26.	

5.6.14 Global Interrupt Status

The following table contains the interrupt status from the various sources to indicate which one caused that last interrupt on the pin.

Table 85 • **Global Interrupt Status, Address 29G (0x1D)**

Bit	Name	Access	Description
15:12	Reserved	RO	Reserved
11	PHY11 interrupt source[1]	RO	PHY11 interrupt source indication 0: PHY caused the interrupt 1: PHY did not cause an interrupt

Table 85 • **Global Interrupt Status, Address 29G (0x1D)** *(continued)*

Bit	Name	Access	Description
10	PHY10 interrupt source[1]	RO	PHY10 interrupt source indication 0: PHY caused the interrupt 1: PHY did not cause an interrupt
9	PHY9 interrupt source[1]	RO	PHY9 interrupt source indication 0: PHY caused the interrupt 1: PHY did not cause an interrupt
8	PHY8 interrupt source[1]	RO	PHY8 interrupt source indication 0: PHY caused the interrupt 1: PHY did not cause an interrupt
7	PHY7 interrupt source[1]	RO	PHY7 interrupt source indication 0: PHY caused the interrupt 1: PHY did not cause an interrupt
6	PHY6 interrupt source[1]	RO	PHY6 interrupt source indication 0: PHY caused the interrupt 1: PHY did not cause an interrupt
5	PHY5 interrupt source[1]	RO	PHY5 interrupt source indication 0: PHY caused the interrupt 1: PHY did not cause an interrupt
4	PHY4 interrupt source[1]	RO	PHY4 interrupt source indication 0: PHY caused the interrupt 1: PHY did not cause an interrupt
3	PHY3 interrupt source[1]	RO	PHY3 interrupt source indication 0: PHY caused the interrupt 1: PHY did not cause an interrupt
2	PHY2 interrupt source[1]	RO	PHY2 interrupt source indication 0: PHY caused the interrupt 1: PHY did not cause an interrupt
1	PHY1 interrupt source[1]	RO	PHY1 interrupt source indication 0: PHY caused the interrupt 1: PHY did not cause an interrupt
0	PHY0 interrupt source[1]	RO	PHY0 interrupt source indication 0: PHY caused the interrupt 1: PHY did not cause an interrupt

1. This bit is set to 1 when the corresponding PHY's Interrupt Status register 26 (0x1A) is read.

5.7 Clause 45 Registers to Support Energy Efficient Ethernet

This section describes the Clause 45 registers that are required to support Energy Efficient Ethernet. Access to these registers is through the IEEE standard registers 13 and 14 (MMD access control and MMD data or address registers) as described in section 4.2.11 and 4.2.12.

The following table lists the addresses and register names in the Clause 45 register page space.

Table 86 • **Clause 45 Registers Page Space**

Address	Name
3.1	PCS Status 1
3.20	EEE Capability
3.22	EEE Wake Error Counter

Table 86 • **Clause 45 Registers Page Space** *(continued)*

Address	Name
7.60	EEE Advertisement
7.61	EEE Link Partner Advertisement

5.7.1 PCS Status 1

The bits in the PCS Status 1 register provide a status of the EEE operation from the PCS for the link that is currently active.

Table 87 • **PCS Status 1, Address 3.1**

Bit	Name	Access	Description
15:12	Reserved	RO	Reserved
11	Tx LPI received	RO/LH	1: Tx PCS has received LPI 0: LPI not received
10	Rx LPI received	RO/LH	1: Rx PCS has received LPI 0: LPI not received
9	Tx LPI indication	RO	1: Tx PCS is currently receiving LPI 0: PCS is not currently receiving LPI
8	Rx LPI indication	RO	1: Rx PCS is currently receiving LPI 0: PCS is not currently receiving LPI
7:3	Reserved	RO	Reserved
2	PCS receive link status	RO	1: PCS receive link up 0: PCS receive link down
1:0	Reserved	RO	Reserved

5.7.2 EEE Capability

This register is used to indicate the capability of the PCS to support EEE functions for each PHY type. The following table shows the bit assignments for the EEE capability register.

Table 88 • **EEE Capability, Address 3.20**

Bit	Name	Access	Description
15:3	Reserved	RO	Reserved
2	1000BASE-T EEE	RO	1: EEE is supported for 1000BASE-T 0: EEE is not supported for 1000BASE-T
1	100BASE-TX EEE	RO	1: EEE is supported for 100BASE-TX 0: EEE is not supported for 100BASE-TX
0	Reserved	RO	Reserved

5.7.3 EEE Wake Error Counter

This register is used by PHY types that support EEE to count wake time faults where the PHY fails to complete its normal wake sequence within the time required for the specific PHY type. The definition of the fault event to be counted is defined for each PHY and can occur during a refresh or a wakeup as

defined by the PHY. This 16-bit counter is reset to all zeros when the EEE wake error counter is read or when the PHY undergoes hardware or software reset.

Table 89 • **EEE Wake Error Counter, Address 3.22**

Bit	Name	Access	Description
15:0	Wake error counter	RO	Count of wake time faults for a PHY

5.7.4   EEE Advertisement

This register defines the EEE advertisement that is sent in the unformatted next page following a EEE technology message code. The following table shows the bit assignments for the EEE advertisement register.

Table 90 • **EEE Advertisement, Address 7.60**

Bit	Name	Access	Description	Default
15:3	Reserved	RO	Reserved	
2	1000BASE-T EEE	R/W	1: Advertise that the 1000BASE-T has EEE capability 0: Do not advertise that the 1000BASE-T has EEE capability	0
1	100BASE-TX EEE	R/W	1: Advertise that the 100BASE-TX has EEE capability 0: Do not advertise that the 100BASE-TX has EEE capability	0
0	Reserved	RO	Reserved	

5.7.5   EEE Link Partner Advertisement

All the bits in the EEE LP Advertisement register are read only. A write to the EEE LP advertisement register has no effect. When the AN process has been completed, this register will reflect the contents of the link partner's EEE advertisement register. The following table shows the bit assignments for the EEE advertisement register.

Table 91 • **EEE Advertisement, Address 7.61**

Bit	Name	Access	Description
15:3	Reserved	RO	Reserved
2	1000BASE-T EEE	RO	1: Link partner is advertising EEE capability for 1000BASE-T 0: Link partner is not advertising EEE capability for 1000BASE-T
1	100BASE-TX EEE	RO	1: Link partner is advertising EEE capability for 100BASE-TX 0: Link partner is not advertising EEE capability for 100BASE-TX
0	Reserved	RO	Reserved

6 Electrical Specifications

This section provides the DC characteristics, AC characteristics, recommended operating conditions, and stress ratings for the VSC8512-02 device.

6.1 DC Characteristics

This section contains the DC specifications for the VSC8512-02 device.

6.1.1 VDD_IO

The following table shows the DC specifications for the pins referenced to VDD_IO. The specifications listed in the following table are valid only when VDD = 1.0 V, VDD_VS = 1.0 V, VDD_AL = 1.0 V, or VDD_AH = 2.5 V.

Table 92 • **VDD_IO DC Characteristics**

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Output high voltage	V_{OH}	2.0	2.8	V	I_{OH} = −1.0 mA
Output low voltage	V_{OL}	−0.3	0.4	V	I_{OL} = 1.0 mA
Input high voltage	V_{IH}	1.85	3.0	V	
Input low voltage	V_{IL}	−0.3	0.7	V	
Input leakage current	I_{ILEAK}	−32	32	µA	Internal resistor included
Output leakage current	I_{OLEAK}	−32	32	µA	Internal resistor included
Output low current drive strength	I_{OL}		6	mA	
Output high current drive strength	I_{OH}	−6		mA	

6.1.2 Internal Pull-Up or Pull-Down Resistors

Internal pull-up or pull-down resistors are specified in the following table. For more information about signals with internal pull-up or pull-down resistors, see Pins by Function, page 98.

All internal pull-up resistors are connected to their respective I/O supply.

Table 93 • **Internal Pull-Up or Pull-Down Resistors**

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Internal pull-up resistor, GPIO pins	R_{PU}	33	53	90	kΩ
Internal pull-up resistor, all other pins	R_{PU}	96	120	144	kΩ
Internal pull-down resistor	R_{PD}	96	120	144	kΩ

6.1.3 Reference Clock

The following table shows the DC specifications for a differential reference clock input signal.

Table 94 • **Reference Clock DC Characteristics**

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Input voltage range	V_{IP}, V_{IN}	−25		1260	mV
Input differential voltage	V_{ID}	150[1]		1000	mV

Table 94 •   **Reference Clock DC Characteristics** *(continued)*

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Input common-mode voltage	V_{ICM}	0		1200[2]	mV
Differential input impedance	R_I		100		Ω

1.   To meet jitter specifications, the minimum input differential voltage must be 400 mV. When using a single-ended clock input, the REFCLK_P low voltage must be less than V_{DDA} – 200 mV, and the high voltage level must be greater than V_{DDA} + 200 mV.
2.   The maximum common-mode voltage is provided without a differential signal. The common-mode voltage is only limited by the maximum and minimum input voltage range and by the differential amplitude of the input signal.

6.1.4   Enhanced SerDes Interface (QSGMII)

All DC specifications for the enhanced SerDes interface are compliant with QSGMII Specification Revision 1.3 and meet or exceed the requirements in the standard. They are also compliant with OIF-CEI-02.0 requirements where applicable.

The enhanced SerDes interface supports the following operating modes: SGMII, QSGMII, and SFP. The values in the following table apply to the modes specified in the condition column.

Table 95 •   **Enhanced SerDes Driver DC Specifications**

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Output differential peak voltage, SFP and QSGMII modes	$|V_{ODp}|$	250	400	mV	V_{DD_VS} = 1.0 V R_L = 100 Ω ±1% maximum drive
Output differential peak voltage, SGMII mode[1]	$|V_{ODp}|$	150	400	mV	V_{DD_VS} = 1.0 V R_L = 100 Ω ±1%
DC output impedance, single-ended, SGMII mode	R_O	40	140	Ω	V_C = 1.0 V See Figure 29, page 83
R_O mismatch between A and B, SGMII mode[2]	ΔR_O		10	%	V_C = 1.0 V See Figure 29, page 83
Change in $|V_{OD}|$ between 0 and 1, SGMII mode	$\Delta|V_{OD}|$		25	mV	R_L = 100 Ω ±1%
Change in V_{OS} between 0 and 1, SGMII mode	ΔV_{OS}		25	mV	R_L = 100 Ω ±1%
Output current, drivers shorted to ground, SGMII and QSGMII modes	$|I_{OSA}|$, $|I_{OSB}|$		40	mA	
Output current, drivers shorted together, SGMII and QSGMII modes	$|I_{OSAB}|$		12	mA	

1.   Voltage is adjustable in 64 steps.
2.   Matching of reflection coefficients. For more information about test methods, see IEEE Std 1596.3-1996.

The following table lists the DC specifications for the enhanced SerDes receiver.

Table 96 •   **Enhanced SerDes Receiver DC Specifications**

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Input voltage range, V_{IA} or V_{IB}[1]	V_I	–0.25		1.2	V

Table 96 • **Enhanced SerDes Receiver DC Specifications** *(continued)*

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Input differential peak-to-peak voltage	$|V_{ID}|$	100		1600	mV
Input common-mode voltage	V_{ICM}	0		1200	mV
Receiver differential input impedance	R_I	80	100	120	Ω

1. QSGMII DC input sensitivity is less than 400 mV.

6.1.5   SerDes Interface (SGMII)

The SerDes output drivers are designed to operate in SGMII/LVDS mode. The SGMII/LVDS mode meets or exceeds the DC requirements of Serial-GMII Specification Revision 1.9 (ENG-46158), unless otherwise noted. The following table lists the DC specifications for the SGMII driver. The values are valid for all configurations, unless stated otherwise.

Table 97 • **SerDes Driver DC Specifications**

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Output high voltage, V_{OA} or V_{OB}	V_{OH}		1250	mV	R_L = 100 Ω ±1%
Output low voltage, V_{OA} or V_{OB}	V_{OL}	0		mV	R_L = 100 Ω ±1%
Output differential peak voltage[1]	$|V_{OD}|$	150	400	mV	V_{DD_VS} = 1.0 V R_L = 100 Ω ±1%
Output differential peak voltage, SGMII mode[1]	$|V_{OD}|$	150	400	mV	V_{DD_VS} = 1.0 V R_L = 100 Ω ±1%
Output offset voltage[2]	V_{OS}	420	580	mV	V_{DD_VS} = 1.0 V R_L = 100 Ω ±1%
DC output impedance, single-ended, SGMII mode	R_O	40	140	Ω	V_C = 1.0 V See Figure 29, page 83
R_O mismatch between A and B, SGMII mode[3]	ΔR_O		10	%	V_C = 1.0 V See Figure 29, page 83
Change in $|V_{OD}|$ between 0 and 1, SGMII mode	$\Delta|V_{OD}|$		25	mV	R_L = 100 Ω ±1%
Change in V_{OS} between 0 and 1, SGMII mode	ΔV_{OS}		25	mV	R_L = 100 Ω ±1%
Output current, driver shorted to GND, SGMII mode	$|I_{OSA}|$, $|I_{OSB}|$		40	mA	
Output current, drivers shorted together, SGMII mode	$|I_{OSAB}|$		12	mA	

1. Voltage is adjustable in 14 steps.
2. Requires AC-coupling for SGMII compliance.
3. Matching of reflection coefficients. For more information about test methods, see IEEE Std 1596.3-1996.

Figure 27 • **SGMII DC Transmit Test Circuit**

$$V_{OD} = V_{OA} - V_{OB}$$
$$V_{OS} = \tfrac{1}{2}\,(V_{OA} + V_{OB})$$
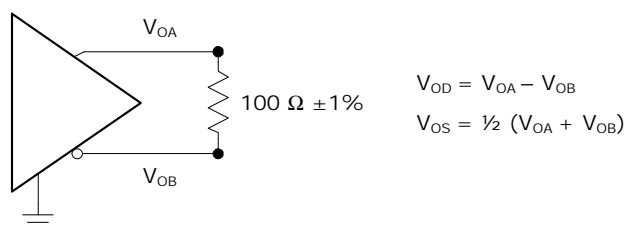
Figure 28 • **SGMII DC Definitions**
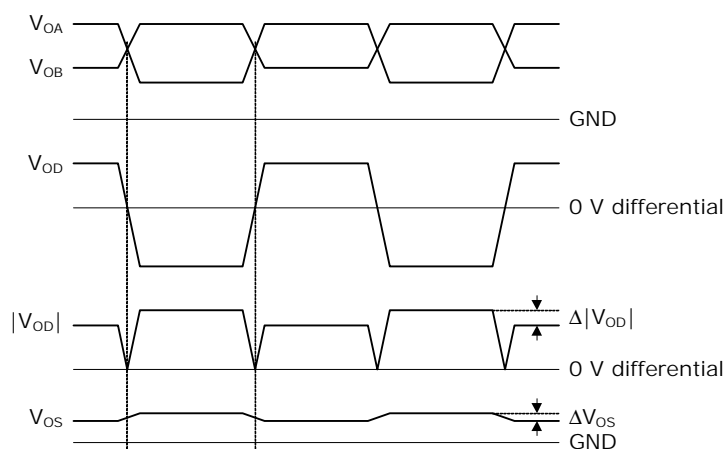
$$\Delta|V_{OD}| = |\,|V_{OAH} - V_{OBL}| - |V_{OBH} - V_{OAL}|\,|$$
$$\Delta V_{OS} = |\,\tfrac{1}{2}(V_{OAH} + V_{OBL}) - \tfrac{1}{2}(V_{OAL} + V_{OBH})\,|$$

Figure 29 • **SGMII DC Driver Output Impedance Test Circuit**
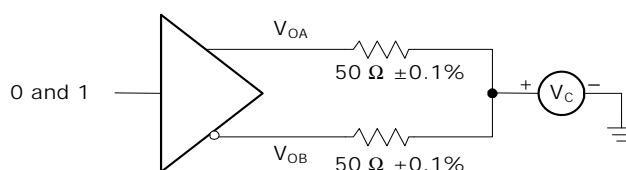
The following table lists the DC specifications for the SGMII receivers.

Table 98 • **SerDes Receiver DC Specifications**

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Input voltage range, V_{IA} or V_{IB}	V_I	–25	1250	mV	
Input differential peak-to-peak voltage	$|V_{ID}|$	100	2000	mV	
Input common-mode voltage[1]	V_{ICM}	0	V_{DD_A}[2]	mV	Without any differential signal (internally AC-coupled)
Receiver differential input impedance	R_I	80	120	Ω	
Input differential hysteresis, SGMII mode	V_{HYST}	25		mV	

1. SGMII compliancy requires external AC-coupling. When interfacing with specific Microsemi devices, DC-coupling is possible. For more information, contact your local Microsemi sales representative.
2. The maximum common-mode voltage is provided without a differential signal, because the input is internally AC-coupled. The common-mode voltage is only limited by the maximum and minimum input voltage range and the input signal's differential amplitude.

Figure 30 • **SGMII DC Input Definitions**

$$V_{ID} = V_{IA} - V_{IB}$$
$$V_{IC} = \tfrac{1}{2}\,(V_{IA} + V_{IB})$$
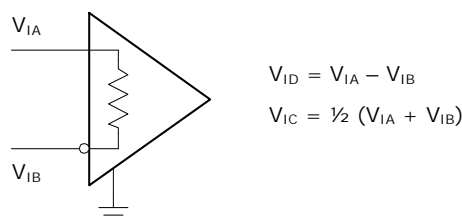
6.1.6 Current Consumption

Current consumption is determined under the following operating conditions:

- QSGMII to 1000BASE-T mode
- QSGMII to 1000BASE-X dual media mode
- QSGMII to 100BASE-FX dual media mode
- SGMII to 1000BASE-T mode

The typical current consumption values in QSGMII to 1000BASE-T mode are based on nominal voltages with the MAC interface operating in QSGMII mode, and all media side ports operating in 1000BASE-T with full-duplex enabled. Data traffic is a 64-bit random data pattern at 100% utilization.

Table 99 • **QSGMII to 1000BASE-T Current Consumption**

Parameter	Symbol	Typical	Maximum	Unit
Worst-case power consumption	P_D		6.75	W
Current with V_{DD} at 1.0 V	I_{VDD}	1.15		A
Current with V_{DD_A} at 1.0 V	I_{VDD_A}	0.18		A
Current with V_{DD_AH} at 2.5 V	I_{VDD_AH}	1.37		A
Current with V_{DD_AL} at 1.0 V	I_{VDD_AL}	0.19		A
Current with V_{DD_IO} at 2.5 V	I_{VDD_IO}	0.06		A
Current with V_{DD_VS} at 1.0 V	I_{VDD_VS}	0.09		A

The typical current consumption values in QSGMII to 1000BASE-X dual media mode are based on nominal voltages with the MAC interface operating in QSGMII mode, 8 media side ports operating in 1000BASE-T with full-duplex enabled and 4 dual media ports operating in 1000BASE-X mode. Data traffic is a 64-bit random data pattern at 100% utilization.

Table 100 • **QSGMII to 1000BASE-X Current Consumption**

Parameter	Symbol	Typical	Maximum	Unit
Worst-case power consumption	P_D		5.25	W
Current with V_{DD} at 1.0 V	I_{VDD}	0.95		A
Current with V_{DD_A} at 1.0 V	I_{VDD_A}	0.2		A
Current with V_{DD_AH} at 2.5 V	I_{VDD_AH}	0.93		A
Current with V_{DD_AL} at 1.0 V	I_{VDD_AL}	0.16		A
Current with V_{DD_IO} at 2.5 V	I_{VDD_IO}	0.06		A

Table 100 • **QSGMII to 1000BASE-X Current Consumption** *(continued)*

Parameter	Symbol	Typical	Maximum	Unit
Current with V_{DD_VS} at 1.0 V	I_{VDD_VS}	0.13		A

The typical current consumption values in QSGMII to 100BASE-FX dual media mode are based on nominal voltages with the MAC interface operating in QSGMII mode, 8 media side ports operating in 1000BASE-T with full-duplex enabled, and 4 dual media ports operating in 100BASE-FX mode. Data traffic is a 64-bit random data pattern at 100% utilization.

Table 101 • **QSGMII to 100BASE-FX Current Consumption**

Parameter	Symbol	Typical	Maximum	Unit
Worst-case power consumption	P_D		5.25	W
Current with V_{DD} at 1.0 V	I_{VDD}	0.95		A
Current with V_{DD_A} at 1.0 V	I_{VDD_A}	0.2		A
Current with V_{DD_AH} at 2.5 V	I_{VDD_AH}	0.93		A
Current with V_{DD_AL} at 1.0 V	I_{VDD_AL}	0.16		A
Current with V_{DD_IO} at 2.5 V	I_{VDD_IO}	0.06		A
Current with V_{DD_VS} at 1.0 V	I_{VDD_VS}	0.13		A

The typical current consumption values in SGMII to 1000BASE-T mode are based on nominal voltages with the MAC interface operating in SGMII mode and all media side ports operating in 1000BASE-T with full-duplex enabled. Data traffic is a 64-bit random data pattern at 100% utilization.

Table 102 • **SGMII to 1000BASE-T Current Consumption**

Parameter	Symbol	Typical	Maximum	Unit
Worst-case power consumption	P_D		6.85	W
Current with V_{DD} at 1.0 V	I_{VDD}	1.18		A
Current with V_{DD_A} at 1.0 V	I_{VDD_A}	0.25		A
Current with V_{DD_AH} at 2.5 V	I_{VDD_AH}	1.37		A
Current with V_{DD_AL} at 1.0 V	I_{VDD_AL}	0.19		A
Current with V_{DD_IO} at 2.5 V	I_{VDD_IO}	0.06		A
Current with V_{DD_VS} at 1.0 V	I_{VDD_VS}	0.19		A

6.2 AC Characteristics

This section provides the AC specifications for the VSC8512-02 device.

6.2.1 Reference Clock

To meet QSGMII jitter generation requirements, Microsemi requires the use of a differential reference clock source. Use of a 25 MHz single-ended reference clock is not recommended. However, to implement a QSGMII chip interconnect using a 25 MHz single-ended reference clock and achieve error-free data transfer on that interface, use an Ethernet switch with higher jitter tolerance than specified in the standard, such as Microsemi VSC742*x* family of products. For more information about QSGMII interoperability when using a 25 MHz single-ended reference clock, contact your Microsemi representative.

The following table shows the AC specifications for a differential reference clock input. Performance is guaranteed for 156.25 MHz and 125 MHz differential clocks only, however 25 MHz and single-ended clocks are also supported.

Table 103 • **Reference Clock AC Characteristics**

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
Reference clock frequency, REFCLK_SEL[2:0] = 100	f	−100 ppm	25.00	100 ppm	MHz	
Reference clock frequency, REFCLK_SEL[2:0] = 000	f	−100 ppm	125.00	100 ppm	MHz	
Reference clock frequency, REFCLK_SEL[2:0] = 001	f	−100 ppm	156.25	100 ppm	MHz	
Duty cycle	DC	40	50	60	%	
Rise time and fall time	t_R, t_F			1.5	ns	20% to 80% threshold
REFCLK input RMS jitter, bandwidth from 12 kHz to 500 kHz				20	ps	
REFCLK input RMS jitter, bandwidth from 500 kHz to 15 MHz				4	ps	
REFCLK input RMS jitter, bandwidth from 15 MHz to 40 MHz				20	ps	
REFCLK input RMS jitter, bandwidth from 40 MHz to 80 MHz				100	ps	
Jitter gain from REFCLK to SerDes output, bandwidth from 0 MHz to 0.1 MHz				0.3	dB	
Jitter gain from REFCLK to SerDes output, bandwidth from 0.1 MHz to 7 MHz				3	dB	
Jitter gain from REFCLK to SerDes output, bandwidth greater than 7 MHz				$3 - 20 \times \log (f/7 \text{ MHz})$	dB	

6.2.2 Recovered Clock Outputs

The following table shows the AC specifications for the RCVRD_CLK1 and RCVRD_CLK0 outputs.

Table 104 • **Recovered Clock AC Characteristics**

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
Recovered clock frequency, registers 23G or 24G bits 10:8 = 001	f		125.00		MHz	
Recovered clock frequency, registers 23G or 24G bits 10:8 = 010	f		31.25		MHz	

Table 104 • **Recovered Clock AC Characteristics** *(continued)*

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
Recovered clock frequency, registers 23G or 24G bits 10:8 = 000	f		25.00		MHz	
Duty cycle	DC	40	50	60	%	
Clock rise and fall time, 20% to 80%	t_R, t_F			1.5	ns	Measured at 50% threshold
Peak-to-peak jitter, copper media interface	JPP_{CLK_Cu}			200	ps	Jitter bandwidth from 12 kHz to 10 MHz
Peak-to-peak jitter, fiber media interface	JPP_{CLK_Fi}			200	ps	Jitter bandwidth from 10 kHz to 80 MHz

6.2.3 SerDes Outputs

The values listed in the following table are valid for all configurations, unless otherwise noted.

Table 105 • **SerDes Output AC Specifications**

Parameter	Symbol	Minimum	Maximum	Unit	Condition
V_{OD} ringing compared to V_S, SGMII mode	V_{RING}		±10	%	R_L = 100 Ω ±1%
V_{OD} rise time and fall time, SGMII mode	t_R, t_F	100	200	ps	20% to 80% of V_S R_L = 100 Ω ±1%
Differential peak-to-peak output voltage	V_{OD}		30	mV	Tx disabled
Differential output return loss, 50 MHz to 625 MHz	RL_{O_DIFF}	≥10		dB	R_L = 100 Ω ±1%
Differential output return loss, 625 MHz to 1250 MHz	RL_{O_DIFF}	10–10 × log (f/625 MHz)		dB	R_L = 100 Ω ±1%
Common-mode return loss, 50 MHz to 625 MHz	RL_{OCM}	6		dB	
Intrapair skew, SGMII mode	t_{SKEW}		20	ps	

6.2.4 SerDes Driver Jitter

The following table lists the jitter characteristics for the SerDes output driver.

Table 106 • **SerDes Driver Jitter Characteristics**

Parameter	Symbol	Maximum	Unit	Condition
Total jitter	TJ_O	192	ps	Measured according to IEEE 802.3.38.5.
Deterministic jitter	DJ_O	80	ps	Measured according to IEEE 802.3.38.5.

6.2.5 SerDes Inputs

The following table lists the AC specifications for the SerDes inputs.

Table 107 • **SerDes Input AC Specifications**

Parameter	Maximum	Unit	Condition
Differential input return loss, 50 MHz to 625 MHz	≥ 10	dB	$R_L = 100\ \Omega\ \pm 1\%$
Differential input return loss, 625 MHz to 1250 MHz	$10 - 10 \times \log(f/625\ \text{MHz})$	dB	$R_L = 100\ \Omega\ \pm 1\%$

6.2.6 SerDes Receiver Jitter Tolerance

The following table lists jitter tolerances for the SerDes receiver.

Table 108 • **SerDes Receiver Jitter Tolerance**

Parameter	Symbol	Minimum	Unit	Condition
Total jitter tolerance, greater than 637 kHz, SFP mode	TJT_I	600	ps	Measured according to IEEE 802.3 38.6.8
Deterministic jitter tolerance, greater than 637 kHz, SFP mode	DJT_I	370	ps	Measured according to IEEE 802.3 38.6.8
Cycle distortion jitter tolerance, 100BASE-FX mode	JT_{CD}	1.4	ns	Measured according to ISO/IEC 9314-3:1990
Data-dependent jitter tolerance, 100BASE-FX mode	DDJ	2.2	ns	Measured according to ISO/IEC 9314-3:1990
Random peak-to-peak jitter tolerance, 100BASE-FX mode	RJT	2.27	ns	Measured according to ISO/IEC 9314-3:1990

6.2.7 Enhanced SerDes Interface

All AC specifications for the enhanced SerDes interface are compliant with QSGMII Specification Revision 1.3 and meet or exceed the requirements in the standard. They are also compliant with the OIF-CEI-02.0 requirements where applicable.

The enhanced SerDes interface supports the following modes of operation: SGMII, QSGMII, and SFP. The values in the tables in the following sections apply to the modes listed in the condition column and are based on the test circuit shown in Figure 27, page 83. The transmit and receive eye specifications relate to the eye diagrams shown in the following illustration, with the compliance load as defined in the test circuit.

Figure 31 • **QSGMII Transient Parameters**
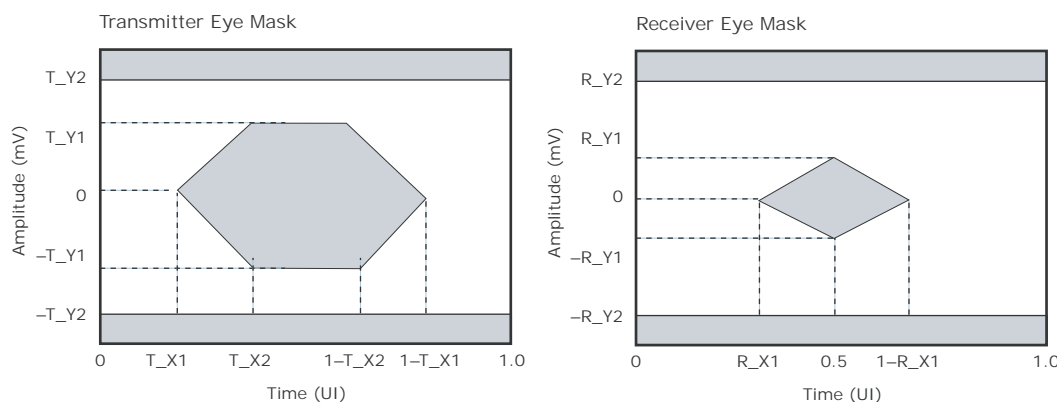
6.2.8 Enhanced SerDes Outputs

The following table provides the AC specifications for the enhanced SerDes outputs in SGMII mode.

Table 109 • **Enhanced SerDes Outputs AC Specifications, SGMII Mode**

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Unit interval, 1.25G mode	UI				800 ps
V_{OD} ringing compared to V_S	V_{RING}		±10	%	R_L = 100 Ω ±1%
V_{OD} rise time and fall time	t_R, t_F	100	200	ps	20% to 80% of V_S R_L = 100 Ω ±1%
Differential peak-to-peak output voltage	V_{OD}		30	mV	Tx disabled
Differential output return loss, 50 MHz to 625 MHz	RL_{O_DIFF}	≥10		dB	R_L = 100 Ω ±1%
Differential output return loss, 625 MHz to 1250 MHz	RL_{O_DIFF}	10–10 × log (f/625 MHz)		dB	R_L = 100 Ω ±1%
Common-mode return loss, 50 MHz to 625 MHz	RL_{OCM}	6		dB	
Intrapair skew	t_{SKEW}		20	ps	

The following table provides the AC specifications for the enhanced SerDes outputs in QSGMII mode.

Table 110 • **Enhanced SerDes Outputs AC Specifications, QSGMII Mode**

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Unit interval, 5G	UI				200 ps
V_{OD} rise time and fall time	t_R, t_F	30	96	ps	20% to 80% of V_S R_L = 100 Ω ±1%
Differential peak-to-peak output voltage	V_{OD}		30	mV	Tx disabled
Differential output return loss, 100 MHz to 2.5 GHz	RL_{O_DIFF}	8		dB	R_L = 100 Ω ±1%
Differential output return loss, 2.5 GHz to 5 GHz	RL_{O_DIFF}	8 dB – 16.6 log (f/2.5 GHz)		dB	R_L = 100 Ω ±1%
Eye mask X1	T_X1		0.15	UI	
Eye mask X2	T_X2		0.4	UI	
Eye mask Y1	T_Y1	200		mV	
Eye mask Y2	T_Y2		450	mV	

6.2.9 Enhanced Serial LEDs

This section contains the AC specifications for the enhanced serial LEDs. The duty cycle of the LED_PULSE signal is programmable and can be varied from 0.5% to 99.5%.

Table 111 • **Enhanced Serial LEDs AC Characteristics**

Parameter	Symbol	Minimum	Maximum	Unit
LED_CLK cycle time	t_{CYC}	255	257	ns
Pause between LED_DATA bit sequences	t_{PAUSE}	387.712	24987	µs

Table 111 • **Enhanced Serial LEDs AC Characteristics** *(continued)*

Parameter	Symbol	Minimum	Maximum	Unit
LED_CLK to LED_DATA	t_{CO}	127	129	ns
LED_CLK to LED_LD	t_{CL}	255	257	ns
LED_LD pulse width	t_{LW}	127	129	ns
LED_PULSE cycle time	t_{PULSE}	199	201	µs

Figure 32 • **Enhanced Serial LED Timing**
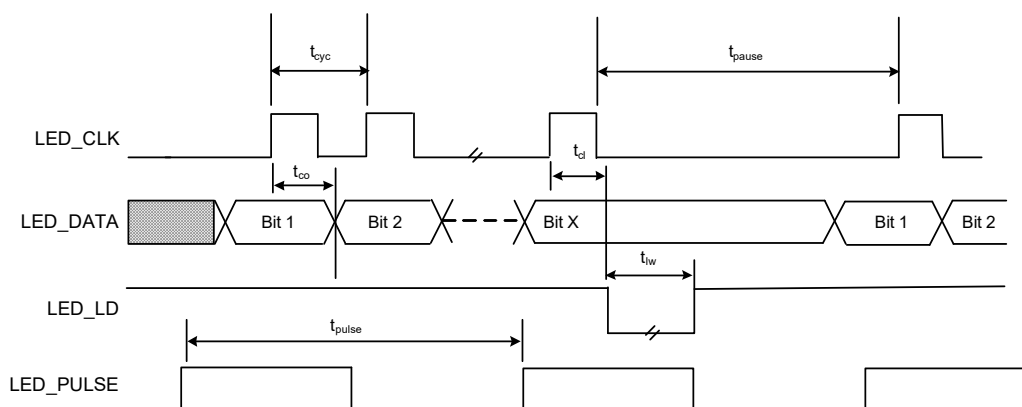
6.2.10 Enhanced SerDes Driver Jitter Characteristics

The following table lists the jitter characteristics for the enhanced SerDes driver in QSGMII mode. For information about jitter characteristics for the enhanced SerDes driver in SGMII mode, see Table 106, page 87.

Table 112 • **Enhanced SerDes Driver Jitter Characteristics, QSGMII Mode**

Parameter	Symbol	Maximum	Unit	Condition
Total output jitter	TJ_O	60	ps	Measured according to IEEE 802.3.38.5.
Deterministic output jitter	DJ_O	10	ps	Measured according to IEEE 802.3.38.5.

6.2.11 Enhanced SerDes Inputs

The following table lists the AC specifications for the enhanced SerDes inputs in SGMII mode.

Table 113 • **Enhanced SerDes Input AC Specifications, SGMII Mode**

Parameter	Symbol	Minimum	Unit	Condition
Unit interval, 1.25G	UI		ps	800 ps
Differential input return loss, 50 MHz to 625 MHz	RL_{I_DIFF}	10	dB	R_L = 100 Ω ±1%
Common-mode input return loss, 50 MHz to 625 MHz	RL_{ICM}	6	dB	

The following table lists the AC specifications for the enhanced SerDes inputs in QSGMII mode.

Table 114 • **Enhanced SerDes Inputs AC Specifications, QSGMII Mode**

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Unit interval, 5G	UI				200 ps
Differential input return loss, 100 MHz to 2.5 GHz	RL_{I_DIFF}	8		dB	R_L = 100 Ω ±1%
Differential input return loss, 2.5 GHz to 5 GHz	RL_{I_DIFF}	8 dB – 16.6 log (f/2.5 GHz)		dB	R_L = 100 Ω ±1%
Common-mode input return loss, 100 MHz to 2.5 GHz	RL_{ICM}	6		dB	
Eye mask X1	R_X1		0.3	UI	
Eye mask Y1	R_Y1		50	mV	
Eye mask Y2	R_Y2		450	mV	

6.2.12 Enhanced SerDes Receiver Jitter Tolerance

The following table lists the jitter tolerance for the enhanced SerDes receiver in QSGMII mode. For information about jitter tolerance for the enhanced SerDes receiver in SGMII mode, see Table 108, page 88.

Table 115 • **Enhanced SerDes Receiver Jitter Tolerance, QSGMII Mode**

Parameter	Symbol	Maximum	Unit	Condition
Bounded high-probability jitter[1]	BHPJ	90	ps	92 ps peak-to-peak random jitter and 38 ps sinusoidal jitter (SJHF).
Sinusoidal jitter, maximum	SJ_{MAX}	1000	ps	
Sinusoidal jitter, high frequency	SJ_{HF}	10	ps	
Total jitter tolerance	TJT_I	120	ps	92 ps peak-to-peak random jitter and 38 ps sinusoidal jitter (SJHF).

1. This is the sum of uncorrelated bounded high probability jitter (0.15 UI), and correlated bounded high probability jitter (0.30 UI). Uncorrelated bounded high probability jitter is distribution where the value of the jitter shows no correlation to any signal level being transmitted, formally defined as deterministic jitter (DJ). Correlated bounded high probability jitter is jitter distribution where the value of the jitter shows a strong correlation to the signal level being transmitted.

6.2.13 JTAG Interface

This section provides the AC specifications for the JTAG interface. The specifications meet or exceed the requirements of IEEE 1149.1-2001. The JTAG receive signal requirements are requested at the pin of the device. The JTAG_TRST signal is asynchronous to the clock, and does not have a setup or hold time requirement.

Table 116 • **JTAG Interface AC Specifications**

Parameter	Symbol	Minimum	Maximum	Unit	Condition
TCK frequency	f		10	MHz	
TCK cycle time	t_C	100		ns	
TCK high time	$t_{W(CH)}$	40		ns	

Table 116 • **JTAG Interface AC Specifications** *(continued)*

Parameter	Symbol	Minimum	Maximum	Unit	Condition
TCK low time	$t_{W(CL)}$	40		ns	
Setup time to TCK rising	t_{SU}	10		ns	
Hold time from TCK rising	t_H	10		ns	
TDO valid after TCK falling	$t_{V(C)}$		28	ns	C_L = 10 pF
TDO hold time from TCK falling	$t_{H(TDO)}$	0		ns	C_L = 0 pF
TDO disable time[1]	t_{DIS}		30	ns	See Figure 34, page 92.
nTRST time low	$t_{W(TL)}$	30		ns	

1. The pin begins to float when a 300 mV change from the actual V_{OH}/V_{OL} level occurs.

Figure 33 • **JTAG Interface Timing Diagram**
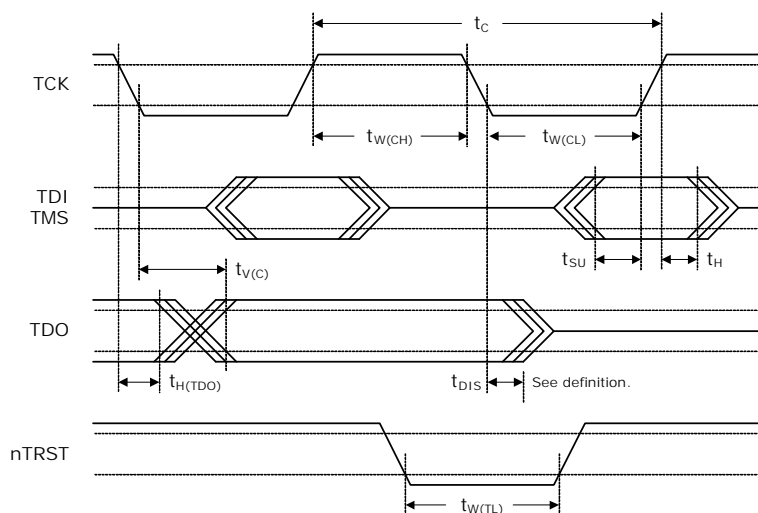
Figure 34 • **Test Circuit for TDO Disable Time**
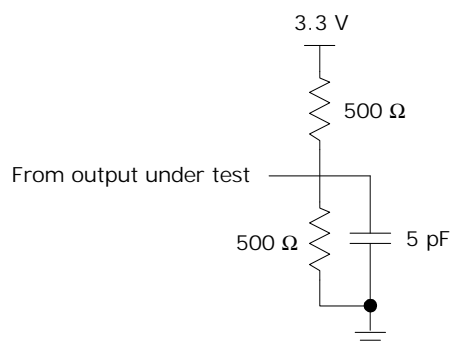
6.2.14   Serial Management Interface

This section contains the AC specifications for the serial management interface (SMI).

Table 117 • **SMI Interface AC Characteristics**

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
MDC frequency[1]	f_{CLK}	0.488		20.83	MHz	

Table 117 • **SMI Interface AC Characteristics** *(continued)*

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
MDC cycle time	t_{CYC}	48		2048	ns	
MDC time high	t_{WH}	20			ns	C_L = 50 pF
MDC time low	t_{WL}	20			ns	C_L = 50 pF
MDIO setup time to MDC on write	t_{SU}	10			ns	
MDIO hold time to MDC on write	t_H	10			ns	
MDC rise time, MDC = 0: 1 MHz	t_R			100	ns	
MDC rise time, MDC = 1 MHz: f_{CLK} maximum	t_R			t_{CYC} × 10%[1]	ns	
MDC fall time, MDC = 0: 1 MHz	t_F			100	ns	
MDC fall time, MDC = 1 MHz: f_{CLK} maximum	t_F			t_{CYC} × 10%[1]	ns	
MDC to MDIO valid	t_{CO}		10	300	ns	Time-dependant on the value of the external pull-up resistor on the MDIO pin

1. For f_{CLK} greater than 1 MHz, the minimum rise time and fall time is in relation to the frequency of the MDC clock period. For example, if f_{CLK} is 2 MHz, the minimum clock rise time and fall time is 50 ns.

Figure 35 • **SMI Interface Timing**
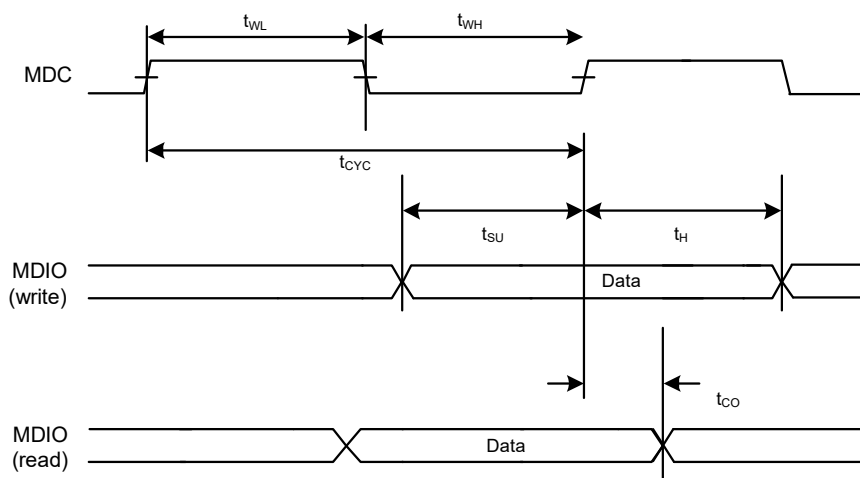
6.2.15 Reset Timing

This section contains the AC specifications that apply to device reset functionality. The signal applied to the NRESET input must comply with the specifications listed in the following table.

Table 118 • **NRESET Timing Specifications**

Parameter	Symbol	Minimum	Maximum	Unit
NRESET assertion time after power supplies and clock stabilize	t_W	2		ms
Recovery time from reset inactive to device fully active	t_{REC}		105	ms
NRESET pulse width	$t_{W(RL)}$	100		ns
Wait time between NRESET de-assert and access of the SMI interface	t_{WAIT}	105		ms

Figure 36 • **Reset Timing**
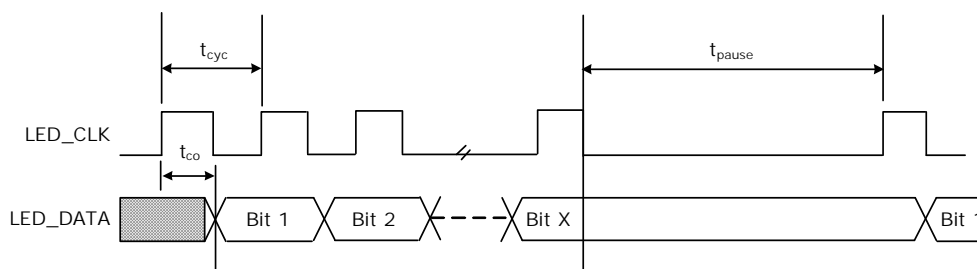
6.2.16 Serial LEDs

This section contains the AC specifications for the serial LEDs.

Table 119 • **Serial LEDs AC Characteristics**

Parameter	Symbol	Minimum	Maximum	Unit
LED_CLK cycle time	t_{CYC}	1		µs
Pause between LED bit sequences	t_{PAUSE}	25		ms
LED_CLK to LED_DATA	t_{CO}		1	ns

Figure 37 • **Serial LED Timing**
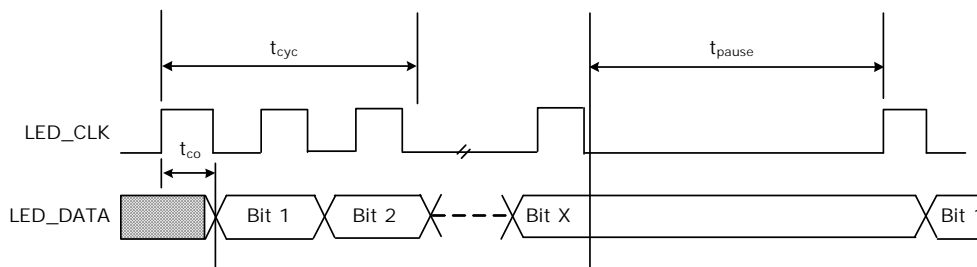
6.2.17 Power Supply Sequencing

During power on and off, V_{DD_A} and V_{DD_VS} must never be more than 300 mV above V_{DD}. V_{DD_VS} must be powered, even if the associated interface is not used. These power supplies must not remain at ground or left floating.

There are no sequencing requirements for V_{DD_AL}, V_{DD_AH}, or V_{DD_IO}. These power supplies can remain at ground or left floating if not used.

The NRESET and JTAG_nTRST inputs must be held low until all power supply voltages

have reached their recommended operating condition values.

6.3 Operating Conditions

The following table shows the recommended operating conditions for the device.

Table 120 • **Recommended Operating Conditions**

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Power supply voltage for V_{DD}	V_{DD}	0.95	1.00	1.05	V
Power supply voltage for V_{DD_A}	V_{DD_A}	0.95	1.00	1.05	V
Power supply voltage for V_{DD_AH}	V_{DD_AH}	2.38	2.50	2.62	V
Power supply voltage for V_{DD_AL}	V_{DD_AL}	0.95	1.00	1.05	V
Power supply voltage for V_{DD_IO}	V_{DD_IO}	2.38	2.50	2.62	V
Power supply voltage for V_{DD_VS}	V_{DD_VS}	0.95	1.00	1.05	V
VSC8512-02 operating temperature[1]	T	0		125	°C
VSC8512-03 operating temperature[1]	T	–40		125	°C

1. Minimum specification is ambient temperature, and the maximum is junction temperature.

6.4 Stress Ratings

This section contains the stress ratings for the VSC8512-02 device.

Warning Stresses listed in the following table may be applied to devices one at a time without causing permanent damage. Functionality at or exceeding the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

Table 121 • **Stress Ratings**

Parameter	Symbol	Minimum	Maximum	Unit
Power supply voltage for core supply	V_{DD}	–0.3	1.10	V
Power supply voltage for SerDes and Enhanced SerDes interfaces	V_{DD_VS}	–0.3	1.32	V
Power supply voltage for analog circuits in twisted pair interface	V_{DD_AL}	–0.3	1.10	V
Power supply voltage for analog circuits in twisted pair interface	V_{DD_AH}	–0.3	2.75	V
Power supply voltage for MIIM, PI, and miscellaneous I/O	V_{DD_IO}	–0.3	2.75	V
Input voltage for GPIO and logic input pins			3.3	V
Storage temperature	T_S	–55	125	°C
Electrostatic discharge voltage, charged device model	V_{ESD_CDM}	–250	250	V
Electrostatic discharge voltage, human body model	V_{ESD_HBM}	–1750	1750	V

Warning This device can be damaged by electrostatic discharge (ESD) voltage. Microsemi recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures may adversely affect reliability of the device.

7 Pin Descriptions

The VSC8512-02 device has 672 pins, which are described in this section.

The pin information is also provided as an attached Microsoft Excel file, so that you can copy it electronically. In Adobe Reader, double-click the attachment icon.

7.1 Pin Diagrams

The following illustrations show the pin diagrams for the VSC8512-02 device.

Figure 38 • **Pin Diagram, Left**

	1	2	3	4	5	6	7	8	9	10	11	12	13
A		P8_D0P	P8_D1P	P8_D2P	P8_D3P	P7_D0P	P7_D1P	P7_D2P	P7_D3P	P6_D0P	P6_D1P	P6_D2P	P6_D3P
B	VSS_1	P8_D0N	P8_D1N	P8_D2N	P8_D3N	P7_D0N	P7_D1N	P7_D2N	P7_D3N	P6_D0N	P6_D1N	P6_D2N	P6_D3N
C	P9_D3P	P9_D3N	COMA_MODE	NRESET	NO CONNECT	VSS	PHYADD3	PHYADD4	RESERVED_3	RESERVED_29	RESERVED_4	REFCLK_SEL0	REFCLK_SEL1
D	P9_D2P	P9_D2N	RESERVED_205	VDD_AH_1	VDD_AH_2	RESERVED_206	RESERVED_207	RESERVED_208	RESERVED_209	RESERVED_248	VDD_AH_4	RESERVED_211	RESERVED_13
E	P9_D1P	P9_D1N	RESERVED_216	VDD_AH_7	VDD_AH_8	VDD_IO_1	VDD_IO_2	VDD_AH_9	VDD_AL_1	VDD_AL_2	VDD_AH_10	VDD_AH_11	REF_REXT_1
F	P9_D0P	P9_D0N	RESERVED_218	VDD_AH_17	VDD_AH_18	VDD_IO_5	VDD_AH_3	VDD_AH_19	VDD_AL_5	VDD_AL_6	VDD_AH_20	VDD_AH_21	RESERVED_219
G	P10_D3P	P10_D3N	VSS_3	RESERVED_15	VSS_4	VDD_1	VDD_2	VDD_3	VDD_AL_9	VDD_AL_10	VDD_4	VDD_5	RESERVED_247
H	P10_D2P	P10_D2N	VSS_7	RESERVED_14	VSS_8	VDD_11	VDD_12	VDD_13	VDD_14	VDD_15	VDD_16	VDD_17	RESERVED_246
J	P10_D1P	P10_D1N	VDD_AH_27	VDD_AH_28	VDD_AL_13	VDD_AL_14	VDD_AL_15	RESERVED_240	RESERVED_241	RESERVED_242	RESERVED_243	RESERVED_244	RESERVED_245
K	P10_D0P	P10_D0N	VSS_11	REF_REXT_2	VDD_AL_19	VDD_AL_20	VDD_AL_21	VSS_12	VSS_13	VSS_14	VSS_15	VSS_16	VSS_17
L	P11_D3P	P11_D3N	VSS_25	REF_FILT_2	VSS_26	VDD_25	VDD_26	VSS_27	VSS_28	VSS_29	VSS_30	VSS_31	VSS_32
M	P11_D2P	P11_D2N	VDD_AH_31	VDD_AH_32	VDD_AH_33	VDD_29	VDD_30	VSS_41	VSS_42	VSS_43	VSS_44	VSS_45	VSS_46
N	P11_D1P	P11_D1N	VSS_53	VSS_54	VSS_55	VDD_33	VDD_34	VSS_56	VSS_57	VSS_58	VSS_59	VSS_60	VSS_61
P	P11_D0P	P11_D0N	VSS_71	RESERVED_24	VDD_IO_7	VDD_37	VDD_38	VSS_72	VSS_73	VSS_74	VSS_75	VSS_76	VSS_77
R	FAST_LINK_STATUS	MDINT	SFP3_SD / GPIO_29	PHY11_LED0	VDD_IO_8	VDD_41	VDD_42	VSS_86	VSS_87	VSS_88	VSS_89	VSS_90	VSS_91
T	PHY10_LED0	PHY9_LED0	PHY8_LED0	PHY7_LED0	VDD_IO_9	VDD_45	VDD_46	VSS_98	VSS_99	VSS_100	VSS_101	VSS_102	VSS_103
U	PHY6_LED0	PHY5_LED0	PHY4_LED0	PHY3_LED0	VDD_IO_10	VSS_110	VSS_111	VSS_112	VSS_113	VSS_114	VSS_115	VSS_116	VSS_117
V	PHY2_LED0	PHY1_LED0	PHY0_LED0 / MDC32_SLED_DATA	PHY11_LED1 / GPIO_16	VDD_IO_11	VDD_49	VDD_50	VDD_51	VDD_52	VDD_53	VDD_54	VDD_55	VDD_56
W	PHY10_LED1 / GPIO_15	PHY9_LED1 / GPIO_14	PHY8_LED1 / GPIO_13	PHY7_LED1 / SFP_SERIALCLK1	VDD_IO_12	VDD_65	VDD_66	VDD_67	VDD_68	VDD_69	VDD_70	VDD_71	VDD_72
Y	PHY6_LED1 / SFP_SERIALCLK2	PHY5_LED1 / SFP_SERIALCLK3	PHY4_LED1 / CLK_SQUELCH_IN	PHY0_LED1 / ESLED1_PULSE	VDD_IO_13	SERDES7_TXP	SERDES6_TXP	REFCLK_P	SERDES_E3_TXP	SERDES5_TXP	SERDES4_TXP	VSS_126	SERDES_E2_TXP
AA	PHY2_LED1 / ESLED1_DO	PHY1_LED1 / ESLED1_LD	PHY3_LED1 / SFP_SERIALCLK0	SFP2_SD / GPIO_4	VDD_IO_14	SERDES7_TXN	SERDES6_TXN	REFCLK_N	SERDES_E3_TXN	SERDES5_TXN	SERDES4_TXN	VSS_145	SERDES_E2_TXN
AB	SFP1_SD / ESLED0_PULSE / GPIO_3	SFP0_SD / ESLED0_DO / GPIO_2	SFP_SERIALDATA / ESLED0_LD	VDD_IO_15	VSS_129	VSS_130	VSS_131	VSS_132	VSS_133	VSS_134	VSS_135	VSS_136
AC	RESERVED_27	RESERVED_28	VSS_148	VDD_IO_16	VDD_IO_17	VDD_A_1	VDD_A_2	VDD_A_3	VDD_A_4	VDD_A_5	VDD_A_6	VDD_A_7	VDD_A_8
AD	RESERVED_25	RESERVED_26	RCVRD_CLK1	VDD_IO_18	VDD_VS_1	VDD_VS_2	VDD_VS_3	VDD_VS_4	VDD_VS_5	VDD_VS_6	VDD_VS_7	VDD_VS_8
AE	VSS_151	RCVRD_CLK0	VDD_IO_19	VSS_163	VSS_152	SERDES7_RXP	SERDES6_RXP	RESERVED_22	SERDES_E3_RXP	SERDES5_RXP	SERDES4_RXP	VSS_153	SERDES_E2_RXP
AF		VDD_IO_20	MDIO	MDC	VSS_158	SERDES7_RXN	SERDES6_RXN	RESERVED_23	SERDES_E3_RXN	SERDES5_RXN	SERDES4_RXN	VSS_159	SERDES_E2_RXN

Figure 39 • **Pin Diagram, Right**

	14	15	16	17	18	19	20	21	22	23	24	25	26	
	P5_D0P	P5_D1P	P5_D2P	P5_D3P	P4_D0P	P4_D1P	P4_D2P	P4_D3P	P3_D0P	P3_D1P	P3_D2P	P3_D3P		A
	P5_D0N	P5_D1N	P5_D2N	P5_D3N	P4_D0N	P4_D1N	P4_D2N	P4_D3N	P3_D0N	P3_D1N	P3_D2N	P3_D3N	VSS_2	B
	REFCLK_SEL2	RESERVED_8	RESERVED_7	RESERVED_6	RESERVED_5	RESERVED_201	RESERVED_202	RESERVED_203	THERMDC_VSS	THERMDA	RESERVED_204	P2_D0N	P2_D0P	C
	RESERVED_12	RESERVED_212	VDD_AH_5	JTAG_CLK	JTAG_DI	JTAG_DO	JTAG_TMS	JTAG_TRST	RESERVED_213	RESERVED_214	RESERVED_215	P2_D1N	P2_D1P	D
	REF_FILT_1	VDD_AH_12	VDD_AH_13	VDD_AL_3	VDD_AL_4	VDD_AH_14	VDD_IO_3	VDD_IO_4	VDD_AH_15	VDD_AH_16	RESERVED_217	P2_D2N	P2_D2P	E
	RESERVED_220	VDD_AH_22	VDD_AH_23	VDD_AL_7	VDD_AL_8	VDD_AH_24	VDD_AH_6	VDD_IO_6	VDD_AH_25	VDD_AH_26	RESERVED_221	P2_D3N	P2_D3P	F
	RESERVED_223	VDD_6	VDD_7	VDD_AL_11	VDD_AL_12	VDD_8	VDD_9	VDD_10	VSS_5	RESERVED_10	VSS_6	P1_D0N	P1_D0P	G
	RESERVED_225	VDD_18	VDD_19	VDD_20	VDD_21	VDD_22	VDD_23	VDD_24	VSS_9	RESERVED_11	VSS_10	P1_D1N	P1_D1P	H
	RESERVED_232	RESERVED_233	RESERVED_234	RESERVED_235	RESERVED_236	RESERVED_237	VDD_AL_16	VDD_AL_17	VDD_AL_18	VDD_AH_29	VDD_AH_30	P1_D2N	P1_D2P	J
	VSS_18	VSS_19	VSS_20	VSS_21	VSS_22	VSS_23	VDD_AL_22	VDD_AL_23	VDD_AL_24	REF_REXT_0	VSS_24	P1_D3N	P1_D3P	K
	VSS_33	VSS_34	VSS_35	VSS_36	VSS_37	VSS_38	VDD_27	VDD_28	VSS_39	REF_FILT_0	VSS_40	P0_D0N	P0_D0P	L
	VSS_47	VSS_48	VSS_49	VSS_50	VSS_51	VSS_52	VDD_31	VDD_32	VDD_AH_34	VDD_AH_35	VDD_AH_36	P0_D1N	P0_D1P	M
	VSS_62	VSS_63	VSS_64	VSS_65	VSS_66	VSS_67	VDD_35	VDD_36	VSS_68	VSS_69	VSS_70	P0_D2N	P0_D2P	N
	VSS_78	VSS_79	VSS_80	VSS_81	VSS_82	VSS_83	VDD_39	VDD_40	VDD_IODDR_1	VSS_84	VSS_85	P0_D3N	P0_D3P	P
	VSS_92	VSS_93	VSS_94	VSS_95	VSS_96	VSS_97	VDD_43	VDD_44	VDD_IODDR_2	NO CONNECT	NO CONNECT	NO CONNECT	NO CONNECT	R
	VSS_104	VSS_105	VSS_106	VSS_107	VSS_108	VSS_109	VDD_47	VDD_48	VDD_IODDR_3	NO CONNECT	NO CONNECT	NO CONNECT	NO CONNECT	T
	VSS_118	VSS_119	VSS_120	VSS_121	VSS_122	VSS_123	VSS_124	VSS_125	VDD_IODDR_4	NO CONNECT	NO CONNECT	NO CONNECT	NO CONNECT	U
	VDD_57	VDD_58	VDD_59	VDD_60	VDD_61	VDD_62	VDD_63	VDD_64	VDD_IODDR_5	NO CONNECT	NO CONNECT	NO CONNECT	NO CONNECT	V
	VDD_73	VDD_74	VDD_75	VDD_76	VDD_77	VDD_78	VDD_79	VDD_80	VDD_IODDR_6	NO CONNECT	NO CONNECT	NO CONNECT	NO CONNECT	W
	SERDES3_TXP	SERDES2_TXP	VSS_127	SERDES_E1_TXP	SERDES1_TXP	SERDES0_TXP	VSS_128	SERDES_E0_TXP	VDD_IODDR_7	NO CONNECT	NO CONNECT	NO CONNECT	NO CONNECT	Y
	SERDES3_TXN	SERDES2_TXN	VSS_146	SERDES_E1_TXN	SERDES1_TXN	SERDES0_TXN	VSS_147	SERDES_E0_TXN	VDD_IODDR_8	NO CONNECT	NO CONNECT	NO CONNECT	NO CONNECT	AA
	VSS_137	VSS_138	VSS_139	VSS_140	VSS_141	VSS_142	VSS_143	VSS_144	VDD_IODDR_9	NO CONNECT	NO CONNECT	NO CONNECT	NO CONNECT	AB
	VDD_A_9	VDD_A_10	VDD_A_11	VDD_A_12	VDD_A_13	VDD_A_14	VDD_A_15	VDD_A_16	VDD_IODDR_10	NO CONNECT	NO CONNECT	NO CONNECT	NO CONNECT	AC
	VDD_VS_9	VDD_VS_10	VDD_VS_11	VDD_VS_12	VDD_VS_13	VDD_VS_14	VDD_VS_15	VDD_VS_16	VSS_150	VDD_IODDR_11	NO CONNECT	NO CONNECT	NO CONNECT	AD
	SERDES3_RXP	SERDES2_RXP	VSS_154	SERDES_E1_RXP	SERDES1_RXP	SERDES0_RXP	VSS_155	SERDES_E0_RXP	SERDES_REXT_0	VSS_156	VDD_IODDR_12	NO CONNECT	VSS_157	AE
	SERDES3_RXN	SERDES2_RXN	VSS_160	SERDES_E1_RXN	SERDES1_RXN	SERDES0_RXN	VSS_161	SERDES_E0_RXN	SERDES_REXT_1	VSS_162	VDD_IODDR_14	VDD_IODDR_13		AF

7.2 Pins by Function

This section contains the functional pin descriptions for the VSC8512-02 device. The following table lists the definitions for the pin type symbols.

Table 122 • **Pin Type Symbol Definitions**

Symbol	Pin Type	Description
3V		3.3 V-tolerant pin.
ABIAS	Analog bias	Analog bias pin.
ADIFF	Analog differential	Analog differential signal pair.
I	Input	Input without on-chip pull-up or pull-down resistor.
I/O	Bidirectional	Bidirectional input or output signal.
NC	No connect	No connect pins must be left floating.
O	Output	Output signal.
OD	Open drain	Open drain output.
OS	Open source	Open source output.
PD	Pull-down	On-chip pull-down resistor to VSS.

Table 122 • **Pin Type Symbol Definitions** *(continued)*

Symbol	Pin Type	Description
PU	Pull-up	On-chip pull-up resistor to VDD_IO.
ST	Schmitt-trigger	Input has Schmitt-trigger circuitry.

7.2.1   JTAG Pins

The following table shows the functional pins for the JTAG interface.

Table 123 • **JTAG Pins**

Name	Pin	Type	Description
JTAG_CLK	D17	I, PU, ST, 3V	JTAG clock pin
JTAG_DI	D18	I, PU, ST, 3V	JTAG data input pin
JTAG_DO	D19	O	JTAG data output pin
JTAG_TMS	D20	I, PU, ST, 3V	JTAG test mode select pin
JTAG_TRST	D21	I, PU, ST, 3V	JTAG reset pin

7.2.2   LED and Multi/General Purpose Input and Output Pins

The following table lists the descriptions for the multifunction LED pins, the multipurpose pins, and the general purpose input/output (GPIO) pins. For more information about configuring these pins, see LED Interface, page 22, and Table 89, page 79.

Table 124 • **LED, Multipurpose, and GPIO Pins**

Name	Pin	Type	Description
PHY[1:11]_LED0	V2, V1, U4, U3, U2, U1, T4, T3, T2, R4	I/O, PU, 3V	LED direct-drive output
PHY0_LED0 / BASIC_SLED_DATA	V3	I/O, PU, 3V	LED direct-drive output Basic serial LED data
PHY0_LED1 / ESLED1_CLK / BASIC_SLED_CLK	AA3	I/O, PU, 3V	LED direct-drive output Enhanced serial LED clock Basic serial LED clock
PHY1_LED1 / ESLED1_LD	AA2	I/O, PU, 3V	LED direct-drive output Enhanced serial LED load
PHY2_LED1 / ESLED1_DO	AA1	I/O, PU, 3V	LED direct-drive output Enhanced serial LED data
PHY3_LED1 / ESLED1_PULSE	Y4	I/O, PU, 3V	LED direct-drive output Enhanced serial LED pulse
PHY4_LED1 / CLK_SQUELCH_IN	Y3	I/O, PU, 3V	LED direct-drive output Clock squelch input
PHY5_LED1 / SFP_SERIALCLK3	Y2	I/O, PU, 3V	LED direct-drive output SFP serial clock
PHY6_LED1 / SFP_SERIALCLK2	Y1	I/O, PU, 3V	LED direct-drive output SFP serial clock
PHY7_LED1 / SFP_SERIALCLK1	W4	I/O, PU, 3V	LED direct-drive output SFP serial clock

Table 124 • **LED, Multipurpose, and GPIO Pins** *(continued)*

Name	Pin	Type	Description
PHY8_LED1 / GPIO_13	W3	I/O, PU, 3V	LED direct-drive output General purpose I/O
PHY9_LED1 / GPIO_14	W2	I/O, PU, 3V	LED direct-drive output General purpose I/O
PHY10_LED1 / GPIO_15	W1	I/O, PU, 3V	LED direct-drive output General purpose I/O
PHY11_LED1 / GPIO_16	V4	I/O, PU, 3V	LED direct-drive output General purpose I/O
SFP_SERIALCLK0 / ESLED0_CLK	AB4	I/O, PU, 3V	SFP serial clock Enhanced serial LED clock
SFP_SERIALDATA / ESLED0_LD	AB3	I/O, PU, 3V	SFP serial data Enhanced serial LED load
SFP0_SD / ESLED0_DO / GPIO_2	AB2	I/O, PU, 3V	SFP Signal Detect Enhanced serial LED data General purpose I/O
SFP1_SD / ESLED0_PULSE / GPIO_3	AB1	I/O, PU, 3V	SFP Signal Detect Enhanced serial LED pulse General purpose I/O
SFP2_SD / GPIO_4	AA4	I/O, PU, 3V	SFP Signal Detect General purpose I/O
SFP3_SD / GPIO_29	R3	I/O, PU, 3V	SFP Signal Detect General purpose I/O

7.2.3   MAC SerDes/QSGMII Interface Pins

The following table shows the functional pins for the MAC SerDes/QSGMII interface.

Table 125 • **MAC SerDes Interface Pins**

Name	Pin	Type	Description
SERDES_E[0:3]_RXN	AF21, AF17, AF13, AF9	ADIFF	Enhanced SerDes receive negative polarity pins
SERDES_E[0:3]_RXP	AE21, AE17, AE13, AE9	ADIFF	Enhanced SerDes receive positive polarity pins
SERDES_E[0:3]_TXN	AA21, AA17, AA13, AA9	ADIFF	Enhanced SerDes transmit negative polarity pins
SERDES_E[0:3]_TXP	Y21, Y17, Y13, Y9	ADIFF	Enhanced SerDes transmit positive polarity pins
SERDES_REXT_[0:1]	AE22, AF22	ABIAS	SerDes bias pins
SERDES[0:7]_RXN	AF19, AF18, AF15, AF14, AF11, AF10, AF7, AF6	ADIFF	SerDes receive negative polarity pins
SERDES[0:7]_RXP	AE19, AE18, AE15, AE14, AE11, AE10, AE7, AE6	ADIFF	SerDes receive positive polarity pins
SERDES[0:7]_TXN	AA19, AA18, AA15, AA14, AA11, AA10, AA7, AA6	ADIFF	SerDes transmit negative polarity pins
SERDES[0:7]_TXP	Y19, Y18, Y15, Y14, Y11, Y10, Y7, Y6	ADIFF	SerDes transmit positive polarity pins

7.2.4 Miscellaneous Pins

The following table shows the miscellaneous pins.

Table 126 • **Miscellaneous Pins**

Name	Pin	Type	Description
FAST_LINK_STATUS	R1	I/O	Fast link failure indication.
PHYADD[3:4]	C7, C8	I, PD	PHY address range select.
RCVRD_CLK[0:1]	AE2, AD3	O	Recovered clock frequency select. These pins are not active when NRESET is asserted. Clock outputs can be enabled or disabled using registers 23G and 24G. When disabled, the pin is held low. 000: 25 MHz output clock 001: 125 MHz output clock 010: 31.25 MHz output clock
REFCLK_N REFCLK_P	AA8 Y8	I, ADIFF	Reference clock input. The input can be either differential or single-ended. In differential mode, REFCLK_P is the true part of the differential signal, and REFCLK_N is the complement part of the differential signal. In single-ended mode, REFCLK_P is used as single-ended LVTTL input, and the REFCLK_N should be pulled to VDD_A. Required applied frequency depends on REFCLK_SEL[2:0] input state.
REFCLK_SEL[0:2]	C12, C13, C14	I, PD	Reference clock frequency select. 0: Connect to pull-down or leave floating. 1: Connect to pull-up to VDD_IO. 000: 125 MHz (default). 001: 156.25 MHz. 100: 25 MHz.
RESERVED_5	C18	I/O	Connect to VDD_IO for correct functioning of fiber media ports.
THERMDA	C23	A	Thermal diode anode.
THERMDC_VSS	C22	A	Thermal diode cathode.

7.2.5 No Connect and Reserved Pins

The following table lists the reserved pins. Not all of the pins are labeled "reserved," but all pins listed should not be connected.

Table 127 • **No Connect and Reserved**

Name	Pin	Type	Description
NO CONNECT	AA23, AA24, AA25, AA26, AB23, AB24, AB25, AB26, AC23, AC24, AC25, AC26, AD24, AD25, AD26, AE25, C5, R23, R24, R25, R26, T23, T24, T25, T26, U23, U24, U25, U26, V23, V24, V25, V26, W23, W24, W25, W26, Y23, Y24, Y25, Y26	NC	Reserved. Leave unconnected.
RESERVED_[3:4]	C9, C11	NC	Reserved. Leave unconnected.
RESERVED_[6:8]	C17, C16, C15	NC	Reserved. Leave unconnected.
RESERVED_[10:15]	G23, H23, D14, D13, H4, G4	NC	Reserved. Leave unconnected.
RESERVED_[22:29]	AE8, AF8, P4, AD1, AD2, AC1, AC2, C10	NC	Reserved. Leave unconnected.
RESERVED_[201:209]	C19, C20, C21, C24, D3, D6, D7, D8, D9	NC	Reserved. Leave unconnected.
RESERVED_[211:221]	D12, D15, D22, D23, D24, E3, E24, F3, F13, F14, F24	NC	Reserved. Leave unconnected.
RESERVED_223	G14	NC	Reserved. Leave unconnected.
RESERVED_225	H14	NC	Reserved. Leave unconnected.
RESERVED_[232:237]	J14, J15, J16, J17, J18, J19	NC	Reserved. Leave unconnected.
RESERVED_[240:248]	J8, J9, J10, J11, J12, J13, H13, G13, D10	NC	Reserved. Leave unconnected.0

7.2.6 Power Supply Pins

The following table lists the power supply pins. All power supply pins must be connected to their respective voltage input, even though certain pin functions may not be used for a specific application.

Table 128 • **Power Supply Pins**

Name	Pin	Type	Description
VDD_[1:80]	G6, G7, G8, G11, G12, G15, G16, G19, G20, G21, H6, H7, H8, H9, H10, H11, H12, H15, H16, H17, H18, H19, H20, H21, L6, L7, L20, L21, M6, M7, M20, M21, N6, N7, N20, N21, P6, P7, P20, P21, R6, R7, R20, R21, T6, T7, T20, T21, V6, V7, V8, V9, V10, V11, V12, V13, V14, V15, V16, V17, V18, V19, V20, V21, W6, W7, W8, W9, W10, W11, W12, W13, W14, W15, W16, W17, W18, W19, W20, W21	1.0V	Connect to 1.0 V

Table 128 • **Power Supply Pins** *(continued)*

Name	Pin	Type	Description
VDD_A_[1:16]	AC6, AC7, AC8, AC9, AC10, AC11, AC12, AC13, AC14, AC15, AC16, AC17, AC18, AC19, AC20, AC21	1.0V	Analog SerDes 1.0 V
VDD_AH_[1:36]	D4, D5, D11, D16, E4, E5, E8, E11, E12, E15, E16, E19, E22, E23, F4, F5, F7, F8, F11, F12, F15, F16, F19, F20, F22, F23, J3, J4, J23, J24, M3, M4, M5, M22, M23, M24	2.5V	Analog 2.5 V
VDD_AL_[1:24]	E9, E10, E17, E18, F9, F10, F17, F18, G9, G10, G17, G18, J5, J6, J7, J20, J21, J22, K5, K6, K7, K20, K21, K22	1.0V	Analog 1.0 V
VDD_IO_[1:20]	E6, E7, E20, E21, F6, F21, P5, R5, T5, U5, V5, W5, Y5, AA5, AB5, AC4, AC5, AD4, AE3, AF2	2.5V	Connect to 2.5 V
VDD_IODDR_[1:14]	P22, R22, T22, U22, V22, W22, Y22, AA22, AB22, AC22, AD23, AE24, AF25, AF24	0V	Ground
VDD_VS_[1:16]	AD6, AD7, AD8, AD9, AD10, AD11, AD12, AD13, AD14, AD15, AD16, AD17, AD18, AD19, AD20, AD21	1.0V	Analog SerDes 1.0 V
VSS	C6	0V	Ground
VSS_[1:163]	B1, B26, G3, G5, G22, G24, H3, H5, H22, H24, K3, K8, K9, K10, K11, K12, K13, K14, K15, K16, K17, K18, K19, K24, L3, L5, L8, L9, L10, L11, L12, L13, L14, L15, L16, L17, L18, L19, L22, L24, M8, M9, M10, M11, M12, M13, M14, M15, M16, M17, M18, M19, N3, N4, N5, N8, N9, N10, N11, N12, N13, N14, N15, N16, N17, N18, N19, N22, N23, N24, P3, P8, P9, P10, P11, P12, P13, P14, P15, P16, P17, P18, P19, P23, P24, R8, R9, R10, R11, R12, R13, R14, R15, R16, R17, R18, R19, T8, T9, T10, T11, T12, T13, T14, T15, T16, T17, T18, T19, U6, U7, U8, U9, U10, U11, U12, U13, U14, U15, U16, U17, U18, U19, U20, U21, Y12, Y16, Y20, AB6, AB7, AB8, AB9, AB10, AB11, AB12, AB13, AB14, AB15, AB16, AB17, AB18, AB19, AB20, AB21, AA12, AA16, AA20, AC3, AD5, AD22, AE1, AE5, AE12, AE16, AE20, AE23, AE26, AF5, AF12, AF16, AF20, AF23, AE4	0V	Ground

7.2.7 Serial Management Interface Pins

The following table shows the functional pins for the serial management interface.

Table 129 • **Serial Management Interface Pins**

Name	Pin	Type	Description
COMA_MODE	C3	I/O, PU, ST, 3V	When this pin is asserted high, all PHYs are held in a powered down state. When this pin is deasserted low, all PHYs are powered up and resume normal operation. This signal is also used to synchronize the operation of multiple chips on the same PCB to provide visual synchronization for LEDs driven from the separate chips.
MDC	AF4	I	Management data clock pin.
MDINT	R2	I/O, OS, OD	Management interrupt signal.
MDIO	AF3	I/O, OD	Management data input/output pin.
nRESET	C4	I, PD, ST, 3V	Device reset pin, active low.

7.2.8 Twisted Pair Interface Pins

The following table shows the functional pins for the twisted pair interface.

Table 130 • **Twisted Pair Interface Pins**

Name	Pin	Type	Description
P0_D[0:3]N	L25, M25, N25, P25	ADIFF	Connects to RJ45 Pin 2 through a magnetic.
P0_D[0:3]P	L26, M26, N26, P26	ADIFF	Connects to RJ45 Pin 1 through a magnetic.
P[0:11]_D0N	L25, G25, C25, B22, B18, B14, B10, B6, B2, F2, K2, P2	ADIFF	Connects to RJ45 Pin 2 through a magnetic.
P[0:11]_D0P	L26, G26, C26, A22, A18, A14, A10, A6, A2, F1, K1, P1	ADIFF	Connects to RJ45 Pin 1 through a magnetic.
P[0:11]_D1N	M25, H25, D25, B23, B19, B15, B11, B7, B3, E2, J2, N2	ADIFF	Connects to RJ45 Pin 6 through a magnetic.
P[0:11]_D1P	M26, H26, D26, A23, A19, A15, A11, A7, A3, E1, J1, N1	ADIFF	Connects to RJ45 Pin 3 through a magnetic.
P[0:11]_D2N	N25, J25, E25, B24, B20, B16, B12, B8, B4, D2, H2, M2	ADIFF	Connects to RJ45 Pin 5 through a magnetic.
P[0:11]_D2P	N26 J26, E26, A24, A20, A16, A12, A8, A4, D1, H1, M1	ADIFF	Connects to RJ45 Pin 4 through a magnetic.
P[0:11]_D3N	P25, K25, F25, B25, B21, B17, B13, B9, B5, C2, G2, L2	ADIFF	Connect to RJ45 pin 8 through a magnetic.
P[0:11}_D3P	P26, K26, F26, A25, A21, A17, A13, A9, A5, C1, G1, L1	ADIFF	Connects to RJ45 pin 7 through a magnetic.

Table 130 • **Twisted Pair Interface Pins** *(continued)*

Name	Pin	Type	Description
REF_FILT_[2:0]	18, 148, 193	ABIAS	Copper media reference filter pins. Connect each of these pins to one external 1 µF capacitor each and then all going to ground.
REF_REXT_[2:0]	19, 149, 194	ABIAS	Copper media reference external pins. Connect each of these pins to one external 2.0 kΩ (1%) resistor each and then all going to ground.

7.3 Pins by Number

This section provides a numeric list of the VSC8512-02 pins.

A2	P8_D0P
A3	P8_D1P
A4	P8_D2P
A5	P8_D3P
A6	P7_D0P
A7	P7_D1P
A8	P7_D2P
A9	P7_D3P
A10	P6_D0P
A11	P6_D1P
A12	P6_D2P
A13	P6_D3P
A14	P5_D0P
A15	P5_D1P
A16	P5_D2P
A17	P5_D3P
A18	P4_D0P
A19	P4_D1P
A20	P4_D2P
A21	P4_D3P
A22	P3_D0P
A23	P3_D1P
A24	P3_D2P
A25	P3_D3P
AA1	PHY2_LED1 / ESLED1_DO
AA2	PHY1_LED1 / ESLED1_LD
AA3	PHY0_LED1 / ESLED1_CLK / BASIC_SLED_CLK
AA4	SFP2_SD / GPIO_4
AA5	VDD_IO_14
AA6	SERDES7_TXN
AA7	SERDES6_TXN
AA8	REFCLK_N
AA9	SERDES_E3_TXN
AA10	SERDES5_TXN
AA11	SERDES4_TXN
AA12	VSS_145

AA13	SERDES_E2_TXN
AA14	SERDES3_TXN
AA15	SERDES2_TXN
AA16	VSS_146
AA17	SERDES_E1_TXN
AA18	SERDES1_TXN
AA19	SERDES0_TXN
AA20	VSS_147
AA21	SERDES_E0_TXN
AA22	VDD_IODDR_8
AA23	NO CONNECT
AA24	NO CONNECT
AA25	NO CONNECT
AA26	NO CONNECT
AB1	SFP1_SD / ESLED0_PULSE /
AB2	SFP0_SD / ESLED0_DO / GPIO_2
AB3	SFP_SERIALDATA / ESLED0_LD
AB4	SFP_SERIALCLK0 / ESLED0_CLK
AB5	VDD_IO_15
AB6	VSS_129
AB7	VSS_130
AB8	VSS_131
AB9	VSS_132
AB10	VSS_133
AB11	VSS_134
AB12	VSS_135
AB13	VSS_136
AB14	VSS_137
AB15	VSS_138
AB16	VSS_139
AB17	VSS_140
AB18	VSS_141
AB19	VSS_142
AB20	VSS_143
AB21	VSS_144
AB22	VDD_IODDR_9
AB23	NO CONNECT
AB24	NO CONNECT

AB25	NO CONNECT		AD11	VDD_VS_6
AB26	NO CONNECT		AD12	VDD_VS_7
AC1	RESERVED_27		AD13	VDD_VS_8
AC2	RESERVED_28		AD14	VDD_VS_9
AC3	VSS_148		AD15	VDD_VS_10
AC4	VDD_IO_16		AD16	VDD_VS_11
AC5	VDD_IO_17		AD17	VDD_VS_12
AC6	VDD_A_1		AD18	VDD_VS_13
AC7	VDD_A_2		AD19	VDD_VS_14
AC8	VDD_A_3		AD20	VDD_VS_15
AC9	VDD_A_4		AD21	VDD_VS_16
AC10	VDD_A_5		AD22	VSS_150
AC11	VDD_A_6		AD23	VDD_IODDR_11
AC12	VDD_A_7		AD24	NO CONNECT
AC13	VDD_A_8		AD25	NO CONNECT
AC14	VDD_A_9		AD26	NO CONNECT
AC15	VDD_A_10		AE1	VSS_151
AC16	VDD_A_11		AE2	RCVRD_CLK0
AC17	VDD_A_12		AE3	VDD_IO_19
AC18	VDD_A_13		AE4	VSS_163
AC19	VDD_A_14		AE5	VSS_152
AC20	VDD_A_15		AE6	SERDES7_RXP
AC21	VDD_A_16		AE7	SERDES6_RXP
AC22	VDD_IODDR_10		AE8	RESERVED_22
AC23	NO CONNECT		AE9	SERDES_E3_RXP
AC24	NO CONNECT		AE10	SERDES5_RXP
AC25	NO CONNECT		AE11	SERDES4_RXP
AC26	NO CONNECT		AE12	VSS_153
AD1	RESERVED_25		AE13	SERDES_E2_RXP
AD2	RESERVED_26		AE14	SERDES3_RXP
AD3	RCVRD_CLK1		AE15	SERDES2_RXP
AD4	VDD_IO_18		AE16	VSS_154
AD5	VSS_149		AE17	SERDES_E1_RXP
AD6	VDD_VS_1		AE18	SERDES1_RXP
AD7	VDD_VS_2		AE19	SERDES0_RXP
AD8	VDD_VS_3		AE20	VSS_155
AD9	VDD_VS_4		AE21	SERDES_E0_RXP
AD10	VDD_VS_5		AE22	SERDES_REXT_0

AE23	VSS_156		B11	P6_D1N
AE24	VDD_IODDR_12		B12	P6_D2N
AE25	NO CONNECT		B13	P6_D3N
AE26	VSS_157		B14	P5_D0N
AF2	VDD_IO_20		B15	P5_D1N
AF3	MDIO		B16	P5_D2N
AF4	MDC		B17	P5_D3N
AF5	VSS_158		B18	P4_D0N
AF6	SERDES7_RXN		B19	P4_D1N
AF7	SERDES6_RXN		B20	P4_D2N
AF8	RESERVED_23		B21	P4_D3N
AF9	SERDES_E3_RXN		B22	P3_D0N
AF10	SERDES5_RXN		B23	P3_D1N
AF11	SERDES4_RXN		B24	P3_D2N
AF12	VSS_159		B25	P3_D3N
AF13	SERDES_E2_RXN		B26	VSS_2
AF14	SERDES3_RXN		C1	P9_D3P
AF15	SERDES2_RXN		C2	P9_D3N
AF16	VSS_160		C3	COMA_MODE
AF17	SERDES_E1_RXN		C4	NRESET
AF18	SERDES1_RXN		C5	NO CONNECT
AF19	SERDES0_RXN		C6	VSS
AF20	VSS_161		C7	PHYADD3
AF21	SERDES_E0_RXN		C8	PHYADD4
AF22	SERDES_REXT_1		C9	RESERVED_3
AF23	VSS_162		C10	RESERVED_29
AF24	VDD_IODDR_14		C11	RESERVED_4
AF25	VDD_IODDR_13		C12	REFCLK_SEL0
B1	VSS_1		C13	REFCLK_SEL1
B2	P8_D0N		C14	REFCLK_SEL2
B3	P8_D1N		C15	RESERVED_8
B4	P8_D2N		C16	RESERVED_7
B5	P8_D3N		C17	RESERVED_6
B6	P7_D0N		C18	RESERVED_5
B7	P7_D1N		C19	RESERVED_201
B8	P7_D2N		C20	RESERVED_202
B9	P7_D3N		C21	RESERVED_203
B10	P6_D0N		C22	THERMDC_VSS

C23	THERMDA		E9	VDD_AL_1
C24	RESERVED_204		E10	VDD_AL_2
C25	P2_D0N		E11	VDD_AH_10
C26	P2_D0P		E12	VDD_AH_11
D1	P9_D2P		E13	REF_REXT_1
D2	P9_D2N		E14	REF_FILT_1
D3	RESERVED_205		E15	VDD_AH_12
D4	VDD_AH_1		E16	VDD_AH_13
D5	VDD_AH_2		E17	VDD_AL_3
D6	RESERVED_206		E18	VDD_AL_4
D7	RESERVED_207		E19	VDD_AH_14
D8	RESERVED_208		E20	VDD_IO_3
D9	RESERVED_209		E21	VDD_IO_4
D10	RESERVED_248		E22	VDD_AH_15
D11	VDD_AH_4		E23	VDD_AH_16
D12	RESERVED_211		E24	RESERVED_217
D13	RESERVED_13		E25	P2_D2N
D14	RESERVED_12		E26	P2_D2P
D15	RESERVED_212		F1	P9_D0P
D16	VDD_AH_5		F2	P9_D0N
D17	JTAG_CLK		F3	RESERVED_218
D18	JTAG_DI		F4	VDD_AH_17
D19	JTAG_DO		F5	VDD_AH_18
D20	JTAG_TMS		F6	VDD_IO_5
D21	JTAG_TRST		F7	VDD_AH_3
D22	RESERVED_213		F8	VDD_AH_19
D23	RESERVED_214		F9	VDD_AL_5
D24	RESERVED_215		F10	VDD_AL_6
D25	P2_D1N		F11	VDD_AH_20
D26	P2_D1P		F12	VDD_AH_21
E1	P9_D1P		F13	RESERVED_219
E2	P9_D1N		F14	RESERVED_220
E3	RESERVED_216		F15	VDD_AH_22
E4	VDD_AH_7		F16	VDD_AH_23
E5	VDD_AH_8		F17	VDD_AL_7
E6	VDD_IO_1		F18	VDD_AL_8
E7	VDD_IO_2		F19	VDD_AH_24
E8	VDD_AH_9		F20	VDD_AH_6

F21	VDD_IO_6
F22	VDD_AH_25
F23	VDD_AH_26
F24	RESERVED_221
F25	P2_D3N
F26	P2_D3P
G1	P10_D3P
G2	P10_D3N
G3	VSS_3
G4	RESERVED_15
G5	VSS_4
G6	VDD_1
G7	VDD_2
G8	VDD_3
G9	VDD_AL_9
G10	VDD_AL_10
G11	VDD_4
G12	VDD_5
G13	RESERVED_247
G14	RESERVED_223
G15	VDD_6
G16	VDD_7
G17	VDD_AL_11
G18	VDD_AL_12
G19	VDD_8
G20	VDD_9
G21	VDD_10
G22	VSS_5
G23	RESERVED_10
G24	VSS_6
G25	P1_D0N
G26	P1_D0P
H1	P10_D2P
H2	P10_D2N
H3	VSS_7
H4	RESERVED_14
H5	VSS_8
H6	VDD_11

H7	VDD_12
H8	VDD_13
H9	VDD_14
H10	VDD_15
H11	VDD_16
H12	VDD_17
H13	RESERVED_246
H14	RESERVED_225
H15	VDD_18
H16	VDD_19
H17	VDD_20
H18	VDD_21
H19	VDD_22
H20	VDD_23
H21	VDD_24
H22	VSS_9
H23	RESERVED_11
H24	VSS_10
H25	P1_D1N
H26	P1_D1P
J1	P10_D1P
J2	P10_D1N
J3	VDD_AH_27
J4	VDD_AH_28
J5	VDD_AL_13
J6	VDD_AL_14
J7	VDD_AL_15
J8	RESERVED_240
J9	RESERVED_241
J10	RESERVED_242
J11	RESERVED_243
J12	RESERVED_244
J13	RESERVED_245
J14	RESERVED_232
J15	RESERVED_233
J16	RESERVED_234
J17	RESERVED_235
J18	RESERVED_236

J19	RESERVED_237	L5	VSS_26
J20	VDD_AL_16	L6	VDD_25
J21	VDD_AL_17	L7	VDD_26
J22	VDD_AL_18	L8	VSS_27
J23	VDD_AH_29	L9	VSS_28
J24	VDD_AH_30	L10	VSS_29
J25	P1_D2N	L11	VSS_30
J26	P1_D2P	L12	VSS_31
K1	P10_D0P	L13	VSS_32
K2	P10_D0N	L14	VSS_33
K3	VSS_11	L15	VSS_34
K4	REF_REXT_2	L16	VSS_35
K5	VDD_AL_19	L17	VSS_36
K6	VDD_AL_20	L18	VSS_37
K7	VDD_AL_21	L19	VSS_38
K8	VSS_12	L20	VDD_27
K9	VSS_13	L21	VDD_28
K10	VSS_14	L22	VSS_39
K11	VSS_15	L23	REF_FILT_0
K12	VSS_16	L24	VSS_40
K13	VSS_17	L25	P0_D0N
K14	VSS_18	L26	P0_D0P
K15	VSS_19	M1	P11_D2P
K16	VSS_20	M2	P11_D2N
K17	VSS_21	M3	VDD_AH_31
K18	VSS_22	M4	VDD_AH_32
K19	VSS_23	M5	VDD_AH_33
K20	VDD_AL_22	M6	VDD_29
K21	VDD_AL_23	M7	VDD_30
K22	VDD_AL_24	M8	VSS_41
K23	REF_REXT_0	M9	VSS_42
K24	VSS_24	M10	VSS_43
K25	P1_D3N	M11	VSS_44
K26	P1_D3P	M12	VSS_45
L1	P11_D3P	M13	VSS_46
L2	P11_D3N	M14	VSS_47
L3	VSS_25	M15	VSS_48
L4	REF_FILT_2	M16	VSS_49

M17	VSS_50		P3	VSS_71
M18	VSS_51		P4	RESERVED_24
M19	VSS_52		P5	VDD_IO_7
M20	VDD_31		P6	VDD_37
M21	VDD_32		P7	VDD_38
M22	VDD_AH_34		P8	VSS_72
M23	VDD_AH_35		P9	VSS_73
M24	VDD_AH_36		P10	VSS_74
M25	P0_D1N		P11	VSS_75
M26	P0_D1P		P12	VSS_76
N1	P11_D1P		P13	VSS_77
N2	P11_D1N		P14	VSS_78
N3	VSS_53		P15	VSS_79
N4	VSS_54		P16	VSS_80
N5	VSS_55		P17	VSS_81
N6	VDD_33		P18	VSS_82
N7	VDD_34		P19	VSS_83
N8	VSS_56		P20	VDD_39
N9	VSS_57		P21	VDD_40
N10	VSS_58		P22	VDD_IODDR_1
N11	VSS_59		P23	VSS_84
N12	VSS_60		P24	VSS_85
N13	VSS_61		P25	P0_D3N
N14	VSS_62		P26	P0_D3P
N15	VSS_63		R1	FAST_LINK_STATUS
N16	VSS_64		R2	MDINT
N17	VSS_65		R3	SFP3_SD / GPIO_29
N18	VSS_66		R4	PHY11_LED0
N19	VSS_67		R5	VDD_IO_8
N20	VDD_35		R6	VDD_41
N21	VDD_36		R7	VDD_42
N22	VSS_68		R8	VSS_86
N23	VSS_69		R9	VSS_87
N24	VSS_70		R10	VSS_88
N25	P0_D2N		R11	VSS_89
N26	P0_D2P		R12	VSS_90
P1	P11_D0P		R13	VSS_91
P2	P11_D0N		R14	VSS_92

R15	VSS_93	U1	PHY6_LED0
R16	VSS_94	U2	PHY5_LED0
R17	VSS_95	U3	PHY4_LED0
R18	VSS_96	U4	PHY3_LED0
R19	VSS_97	U5	VDD_IO_10
R20	VDD_43	U6	VSS_110
R21	VDD_44	U7	VSS_111
R22	VDD_IODDR_2	U8	VSS_112
R23	NO CONNECT	U9	VSS_113
R24	NO CONNECT	U10	VSS_114
R25	NO CONNECT	U11	VSS_115
R26	NO CONNECT	U12	VSS_116
T1	PHY10_LED0	U13	VSS_117
T2	PHY9_LED0	U14	VSS_118
T3	PHY8_LED0	U15	VSS_119
T4	PHY7_LED0	U16	VSS_120
T5	VDD_IO_9	U17	VSS_121
T6	VDD_45	U18	VSS_122
T7	VDD_46	U19	VSS_123
T8	VSS_98	U20	VSS_124
T9	VSS_99	U21	VSS_125
T10	VSS_100	U22	VDD_IODDR_4
T11	VSS_101	U23	NO CONNECT
T12	VSS_102	U24	NO CONNECT
T13	VSS_103	U25	NO CONNECT
T14	VSS_104	U26	NO CONNECT
T15	VSS_105	V1	PHY2_LED0
T16	VSS_106	V2	PHY1_LED0
T17	VSS_107	V3	PHY0_LED0 / BASIC_SLED_DATA
T18	VSS_108	V4	PHY11_LED1 / GPIO_16
T19	VSS_109	V5	VDD_IO_11
T20	VDD_47	V6	VDD_49
T21	VDD_48	V7	VDD_50
T22	VDD_IODDR_3	V8	VDD_51
T23	NO CONNECT	V9	VDD_52
T24	NO CONNECT	V10	VDD_53
T25	NO CONNECT	V11	VDD_54
T26	NO CONNECT	V12	VDD_55

V13	VDD_56	W25	NO CONNECT
V14	VDD_57	W26	NO CONNECT
V15	VDD_58	Y1	PHY6_LED1 / SFP_SERIALCLK2
V16	VDD_59	Y2	PHY5_LED1 / SFP_SERIALCLK3
V17	VDD_60	Y3	PHY4_LED1 / CLK_SQUELCH_IN
V18	VDD_61	Y4	PHY3_LED1 / ESLED1_PULSE
V19	VDD_62	Y5	VDD_IO_13
V20	VDD_63	Y6	SERDES7_TXP
V21	VDD_64	Y7	SERDES6_TXP
V22	VDD_IODDR_5	Y8	REFCLK_P
V23	NO CONNECT	Y9	SERDES_E3_TXP
V24	NO CONNECT	Y10	SERDES5_TXP
V25	NO CONNECT	Y11	SERDES4_TXP
V26	NO CONNECT	Y12	VSS_126
W1	PHY10_LED1 / GPIO_15	Y13	SERDES_E2_TXP
W2	PHY9_LED1 / GPIO_14	Y14	SERDES3_TXP
W3	PHY8_LED1 / GPIO_13	Y15	SERDES2_TXP
W4	PHY7_LED1 / SFP_SERIALCLK1	Y16	VSS_127
W5	VDD_IO_12	Y17	SERDES_E1_TXP
W6	VDD_65	Y18	SERDES1_TXP
W7	VDD_66	Y19	SERDES0_TXP
W8	VDD_67	Y20	VSS_128
W9	VDD_68	Y21	SERDES_E0_TXP
W10	VDD_69	Y22	VDD_IODDR_7
W11	VDD_70	Y23	NO CONNECT
W12	VDD_71	Y24	NO CONNECT
W13	VDD_72	Y25	NO CONNECT
W14	VDD_73	Y26	NO CONNECT
W15	VDD_74		
W16	VDD_75		
W17	VDD_76		
W18	VDD_77		
W19	VDD_78		
W20	VDD_79		
W21	VDD_80		
W22	VDD_IODDR_6		
W23	NO CONNECT		
W24	NO CONNECT		

7.4   Pins by Name

This section provides an alphabetical list of the VSC8512-02 pins.

COMA_MODE	C3
FAST_LINK_STATUS	R1
JTAG_CLK	D17
JTAG_DI	D18
JTAG_DO	D19
JTAG_TMS	D20
JTAG_TRST	D21
MDC	AF4
MDINT	R2
MDIO	AF3
NO CONNECT	AA23
NO CONNECT	AA24
NO CONNECT	AA25
NO CONNECT	AA26
NO CONNECT	AB23
NO CONNECT	AB24
NO CONNECT	AB25
NO CONNECT	AB26
NO CONNECT	AC23
NO CONNECT	AC24
NO CONNECT	AC25
NO CONNECT	AC26
NO CONNECT	AD24
NO CONNECT	AD25
NO CONNECT	AD26
NO CONNECT	AE25
NO CONNECT	C5
NO CONNECT	R23
NO CONNECT	R24
NO CONNECT	R25
NO CONNECT	R26
NO CONNECT	T23
NO CONNECT	T24
NO CONNECT	T25
NO CONNECT	T26
NO CONNECT	U23

NO CONNECT	U24
NO CONNECT	U25
NO CONNECT	U26
NO CONNECT	V23
NO CONNECT	V24
NO CONNECT	V25
NO CONNECT	V26
NO CONNECT	W23
NO CONNECT	W24
NO CONNECT	W25
NO CONNECT	W26
NO CONNECT	Y23
NO CONNECT	Y24
NO CONNECT	Y25
NO CONNECT	Y26
NRESET	C4
P0_D0N	L25
P0_D0P	L26
P0_D1N	M25
P0_D1P	M26
P0_D2N	N25
P0_D2P	N26
P0_D3N	P25
P0_D3P	P26
P1_D0N	G25
P1_D0P	G26
P1_D1N	H25
P1_D1P	H26
P1_D2N	J25
P1_D2P	J26
P1_D3N	K25
P1_D3P	K26
P10_D0N	K2
P10_D0P	K1
P10_D1N	J2
P10_D1P	J1
P10_D2N	H2
P10_D2P	H1

P10_D3N	G2	P5_D2N	B16
P10_D3P	G1	P5_D2P	A16
P11_D0N	P2	P5_D3N	B17
P11_D0P	P1	P5_D3P	A17
P11_D1N	N2	P6_D0N	B10
P11_D1P	N1	P6_D0P	A10
P11_D2N	M2	P6_D1N	B11
P11_D2P	M1	P6_D1P	A11
P11_D3N	L2	P6_D2N	B12
P11_D3P	L1	P6_D2P	A12
P2_D0N	C25	P6_D3N	B13
P2_D0P	C26	P6_D3P	A13
P2_D1N	D25	P7_D0N	B6
P2_D1P	D26	P7_D0P	A6
P2_D2N	E25	P7_D1N	B7
P2_D2P	E26	P7_D1P	A7
P2_D3N	F25	P7_D2N	B8
P2_D3P	F26	P7_D2P	A8
P3_D0N	B22	P7_D3N	B9
P3_D0P	A22	P7_D3P	A9
P3_D1N	B23	P8_D0N	B2
P3_D1P	A23	P8_D0P	A2
P3_D2N	B24	P8_D1N	B3
P3_D2P	A24	P8_D1P	A3
P3_D3N	B25	P8_D2N	B4
P3_D3P	A25	P8_D2P	A4
P4_D0N	B18	P8_D3N	B5
P4_D0P	A18	P8_D3P	A5
P4_D1N	B19	P9_D0N	F2
P4_D1P	A19	P9_D0P	F1
P4_D2N	B20	P9_D1N	E2
P4_D2P	A20	P9_D1P	E1
P4_D3N	B21	P9_D2N	D2
P4_D3P	A21	P9_D2P	D1
P5_D0N	B14	P9_D3N	C2
P5_D0P	A14	P9_D3P	C1
P5_D1N	B15	PHY0_LED0 / BASIC_SLED_DATA	V3
P5_D1P	A15	PHY0_LED1 / ESLED1_CLK / BASIC_SLED_CLK	AA3

PHY1_LED0	V2	RESERVED_4	C11
PHY1_LED1 / ESLED1_LD	AA2	RESERVED_5	C18
PHY10_LED0	T1	RESERVED_6	C17
PHY10_LED1 / GPIO_15	W1	RESERVED_7	C16
PHY11_LED0	R4	RESERVED_8	C15
PHY11_LED1 / GPIO_16	V4	RESERVED_10	G23
PHY2_LED0	V1	RESERVED_11	H23
PHY2_LED1 / ESLED1_DO	AA1	RESERVED_12	D14
PHY3_LED0	U4	RESERVED_13	D13
PHY3_LED1 / ESLED1_PULSE	Y4	RESERVED_14	H4
PHY4_LED0	U3	RESERVED_15	G4
PHY4_LED1 / CLK_SQUELCH_IN	Y3	RESERVED_22	AE8
PHY5_LED0	U2	RESERVED_23	AF8
PHY5_LED1 / SFP_SERIALCLK3	Y2	RESERVED_24	P4
PHY6_LED0	U1	RESERVED_25	AD1
PHY6_LED1 / SFP_SERIALCLK2	Y1	RESERVED_26	AD2
PHY7_LED0	T4	RESERVED_27	AC1
PHY7_LED1 / SFP_SERIALCLK1	W4	RESERVED_28	AC2
PHY8_LED0	T3	RESERVED_29	C10
PHY8_LED1 / GPIO_13	W3	RESERVED_211	D12
PHY9_LED0	T2	RESERVED_212	D15
PHY9_LED1 / GPIO_14	W2	RESERVED_213	D22
PHYADD3	C7	RESERVED_214	D23
PHYADD4	C8	RESERVED_215	D24
RCVRD_CLK0	AE2	RESERVED_216	E3
RCVRD_CLK1	AD3	RESERVED_217	E24
REF_FILT_0	L23	RESERVED_218	F3
REF_FILT_1	E14	RESERVED_219	F13
REF_FILT_2	L4	RESERVED_220	F14
REF_REXT_0	K23	RESERVED_221	F24
REF_REXT_1	E13	RESERVED_223	G14
REF_REXT_2	K4	RESERVED_225	H14
REFCLK_N	AA8	RESERVED_232	J14
REFCLK_P	Y8	RESERVED_233	J15
REFCLK_SEL0	C12	RESERVED_234	J16
REFCLK_SEL1	C13	RESERVED_235	J17
REFCLK_SEL2	C14	RESERVED_236	J18
RESERVED_3	C9	RESERVED_237	J19

RESERVED_240	J8	SERDES0_TXN	AA19
RESERVED_241	J9	SERDES0_TXP	Y19
RESERVED_242	J10	SERDES1_RXN	AF18
RESERVED_243	J11	SERDES1_RXP	AE18
RESERVED_244	J12	SERDES1_TXN	AA18
RESERVED_245	J13	SERDES1_TXP	Y18
RESERVED_246	H13	SERDES2_RXN	AF15
RESERVED_247	G13	SERDES2_RXP	AE15
RESERVED_248	D10	SERDES2_TXN	AA15
RESERVED_201	C19	SERDES2_TXP	Y15
RESERVED_202	C20	SERDES3_RXN	AF14
RESERVED_203	C21	SERDES3_RXP	AE14
RESERVED_204	C24	SERDES3_TXN	AA14
RESERVED_205	D3	SERDES3_TXP	Y14
RESERVED_206	D6	SERDES4_RXN	AF11
RESERVED_207	D7	SERDES4_RXP	AE11
RESERVED_208	D8	SERDES4_TXN	AA11
RESERVED_209	D9	SERDES4_TXP	Y11
SERDES_E0_RXN	AF21	SERDES5_RXN	AF10
SERDES_E0_RXP	AE21	SERDES5_RXP	AE10
SERDES_E0_TXN	AA21	SERDES5_TXN	AA10
SERDES_E0_TXP	Y21	SERDES5_TXP	Y10
SERDES_E1_RXN	AF17	SERDES6_RXN	AF7
SERDES_E1_RXP	AE17	SERDES6_RXP	AE7
SERDES_E1_TXN	AA17	SERDES6_TXN	AA7
SERDES_E1_TXP	Y17	SERDES6_TXP	Y7
SERDES_E2_RXN	AF13	SERDES7_RXN	AF6
SERDES_E2_RXP	AE13	SERDES7_RXP	AE6
SERDES_E2_TXN	AA13	SERDES7_TXN	AA6
SERDES_E2_TXP	Y13	SERDES7_TXP	Y6
SERDES_E3_RXN	AF9	SFP_SERIALCLK0 / ESLED0_CLK	AB4
SERDES_E3_RXP	AE9	SFP_SERIALDATA / ESLED0_LD	AB3
SERDES_E3_TXN	AA9	SFP0_SD / ESLED0_DO / GPIO_2	AB2
SERDES_E3_TXP	Y9	SFP1_SD / ESLED0_PULSE / GPIO_3	AB1
SERDES_REXT_0	AE22	SFP2_SD / GPIO_4	AA4
SERDES_REXT_1	AF22	SFP3_SD / GPIO_29	R3
SERDES0_RXN	AF19	THERMDA	C23
SERDES0_RXP	AE19	THERMDC_VSS	C22

VDD_1	G6	VDD_39	P20
VDD_2	G7	VDD_40	P21
VDD_3	G8	VDD_41	R6
VDD_4	G11	VDD_42	R7
VDD_5	G12	VDD_43	R20
VDD_6	G15	VDD_44	R21
VDD_7	G16	VDD_45	T6
VDD_8	G19	VDD_46	T7
VDD_9	G20	VDD_47	T20
VDD_10	G21	VDD_48	T21
VDD_11	H6	VDD_49	V6
VDD_12	H7	VDD_50	V7
VDD_13	H8	VDD_51	V8
VDD_14	H9	VDD_52	V9
VDD_15	H10	VDD_53	V10
VDD_16	H11	VDD_54	V11
VDD_17	H12	VDD_55	V12
VDD_18	H15	VDD_56	V13
VDD_19	H16	VDD_57	V14
VDD_20	H17	VDD_58	V15
VDD_21	H18	VDD_59	V16
VDD_22	H19	VDD_60	V17
VDD_23	H20	VDD_61	V18
VDD_24	H21	VDD_62	V19
VDD_25	L6	VDD_63	V20
VDD_26	L7	VDD_64	V21
VDD_27	L20	VDD_65	W6
VDD_28	L21	VDD_66	W7
VDD_29	M6	VDD_67	W8
VDD_30	M7	VDD_68	W9
VDD_31	M20	VDD_69	W10
VDD_32	M21	VDD_70	W11
VDD_33	N6	VDD_71	W12
VDD_34	N7	VDD_72	W13
VDD_35	N20	VDD_73	W14
VDD_36	N21	VDD_74	W15
VDD_37	P6	VDD_75	W16
VDD_38	P7	VDD_76	W17

VDD_77	W18	VDD_AH_19	F8
VDD_78	W19	VDD_AH_20	F11
VDD_79	W20	VDD_AH_21	F12
VDD_80	W21	VDD_AH_22	F15
VDD_A_1	AC6	VDD_AH_23	F16
VDD_A_2	AC7	VDD_AH_24	F19
VDD_A_3	AC8	VDD_AH_25	F22
VDD_A_4	AC9	VDD_AH_26	F23
VDD_A_5	AC10	VDD_AH_27	J3
VDD_A_6	AC11	VDD_AH_28	J4
VDD_A_7	AC12	VDD_AH_29	J23
VDD_A_8	AC13	VDD_AH_30	J24
VDD_A_9	AC14	VDD_AH_31	M3
VDD_A_10	AC15	VDD_AH_32	M4
VDD_A_11	AC16	VDD_AH_33	M5
VDD_A_12	AC17	VDD_AH_34	M22
VDD_A_13	AC18	VDD_AH_35	M23
VDD_A_14	AC19	VDD_AH_36	M24
VDD_A_15	AC20	VDD_AL_1	E9
VDD_A_16	AC21	VDD_AL_2	E10
VDD_AH_1	D4	VDD_AL_3	E17
VDD_AH_2	D5	VDD_AL_4	E18
VDD_AH_3	F7	VDD_AL_5	F9
VDD_AH_4	D11	VDD_AL_6	F10
VDD_AH_5	D16	VDD_AL_7	F17
VDD_AH_6	F20	VDD_AL_8	F18
VDD_AH_7	E4	VDD_AL_9	G9
VDD_AH_8	E5	VDD_AL_10	G10
VDD_AH_9	E8	VDD_AL_11	G17
VDD_AH_10	E11	VDD_AL_12	G18
VDD_AH_11	E12	VDD_AL_13	J5
VDD_AH_12	E15	VDD_AL_14	J6
VDD_AH_13	E16	VDD_AL_15	J7
VDD_AH_14	E19	VDD_AL_16	J20
VDD_AH_15	E22	VDD_AL_17	J21
VDD_AH_16	E23	VDD_AL_18	J22
VDD_AH_17	F4	VDD_AL_19	K5
VDD_AH_18	F5	VDD_AL_20	K6

VDD_AL_21	K7	VDD_VS_1	AD6
VDD_AL_22	K20	VDD_VS_2	AD7
VDD_AL_23	K21	VDD_VS_3	AD8
VDD_AL_24	K22	VDD_VS_4	AD9
VDD_IO_1	E6	VDD_VS_5	AD10
VDD_IO_2	E7	VDD_VS_6	AD11
VDD_IO_3	E20	VDD_VS_7	AD12
VDD_IO_4	E21	VDD_VS_8	AD13
VDD_IO_5	F6	VDD_VS_9	AD14
VDD_IO_6	F21	VDD_VS_10	AD15
VDD_IO_7	P5	VDD_VS_11	AD16
VDD_IO_8	R5	VDD_VS_12	AD17
VDD_IO_9	T5	VDD_VS_13	AD18
VDD_IO_10	U5	VDD_VS_14	AD19
VDD_IO_11	V5	VDD_VS_15	AD20
VDD_IO_12	W5	VDD_VS_16	AD21
VDD_IO_13	Y5	VSS	C6
VDD_IO_14	AA5	VSS_1	B1
VDD_IO_15	AB5	VSS_2	B26
VDD_IO_16	AC4	VSS_3	G3
VDD_IO_17	AC5	VSS_4	G5
VDD_IO_18	AD4	VSS_5	G22
VDD_IO_19	AE3	VSS_6	G24
VDD_IO_20	AF2	VSS_7	H3
VDD_IODDR_1	P22	VSS_8	H5
VDD_IODDR_2	R22	VSS_9	H22
VDD_IODDR_3	T22	VSS_10	H24
VDD_IODDR_4	U22	VSS_11	K3
VDD_IODDR_5	V22	VSS_12	K8
VDD_IODDR_6	W22	VSS_13	K9
VDD_IODDR_7	Y22	VSS_14	K10
VDD_IODDR_8	AA22	VSS_15	K11
VDD_IODDR_9	AB22	VSS_16	K12
VDD_IODDR_10	AC22	VSS_17	K13
VDD_IODDR_11	AD23	VSS_18	K14
VDD_IODDR_12	AE24	VSS_19	K15
VDD_IODDR_13	AF25	VSS_20	K16
VDD_IODDR_14	AF24	VSS_21	K17

VSS_22	K18	VSS_60	N12
VSS_23	K19	VSS_61	N13
VSS_24	K24	VSS_62	N14
VSS_25	L3	VSS_63	N15
VSS_26	L5	VSS_64	N16
VSS_27	L8	VSS_65	N17
VSS_28	L9	VSS_66	N18
VSS_29	L10	VSS_67	N19
VSS_30	L11	VSS_68	N22
VSS_31	L12	VSS_69	N23
VSS_32	L13	VSS_70	N24
VSS_33	L14	VSS_71	P3
VSS_34	L15	VSS_72	P8
VSS_35	L16	VSS_73	P9
VSS_36	L17	VSS_74	P10
VSS_37	L18	VSS_75	P11
VSS_38	L19	VSS_76	P12
VSS_39	L22	VSS_77	P13
VSS_40	L24	VSS_78	P14
VSS_41	M8	VSS_79	P15
VSS_42	M9	VSS_80	P16
VSS_43	M10	VSS_81	P17
VSS_44	M11	VSS_82	P18
VSS_45	M12	VSS_83	P19
VSS_46	M13	VSS_84	P23
VSS_47	M14	VSS_85	P24
VSS_48	M15	VSS_86	R8
VSS_49	M16	VSS_87	R9
VSS_50	M17	VSS_88	R10
VSS_51	M18	VSS_89	R11
VSS_52	M19	VSS_90	R12
VSS_53	N3	VSS_91	R13
VSS_54	N4	VSS_92	R14
VSS_55	N5	VSS_93	R15
VSS_56	N8	VSS_94	R16
VSS_57	N9	VSS_95	R17
VSS_58	N10	VSS_96	R18
VSS_59	N11	VSS_97	R19

VSS_98	T8	VSS_146	AA16
VSS_99	T9	VSS_147	AA20
VSS_110	U6	VSS_148	AC3
VSS_111	U7	VSS_149	AD5
VSS_112	U8	VSS_150	AD22
VSS_113	U9	VSS_151	AE1
VSS_114	U10	VSS_152	AE5
VSS_115	U11	VSS_153	AE12
VSS_116	U12	VSS_154	AE16
VSS_117	U13	VSS_155	AE20
VSS_118	U14	VSS_156	AE23
VSS_119	U15	VSS_157	AE26
VSS_120	U16	VSS_158	AF5
VSS_121	U17	VSS_159	AF12
VSS_122	U18	VSS_160	AF16
VSS_123	U19	VSS_161	AF20
VSS_124	U20	VSS_162	AF23
VSS_125	U21	VSS_163	AE4
VSS_126	Y12	VSS_100	T10
VSS_127	Y16	VSS_101	T11
VSS_128	Y20	VSS_102	T12
VSS_129	AB6	VSS_103	T13
VSS_130	AB7	VSS_104	T14
VSS_131	AB8	VSS_105	T15
VSS_132	AB9	VSS_106	T16
VSS_133	AB10	VSS_107	T17
VSS_134	AB11	VSS_108	T18
VSS_135	AB12	VSS_109	T19
VSS_136	AB13		
VSS_137	AB14		
VSS_138	AB15		
VSS_139	AB16		
VSS_140	AB17		
VSS_141	AB18		
VSS_142	AB19		
VSS_143	AB20		
VSS_144	AB21		
VSS_145	AA12		

8 Package Information

VSC8512XJG-02 and VSC8512XJG-03 are packaged in a lead-free (Pb-free), 672-pin, thermally enhanced, plastic ball grid array (BGA) with a 27 mm × 27 mm body size, 1 mm pin pitch, and 2.44 mm maximum height.
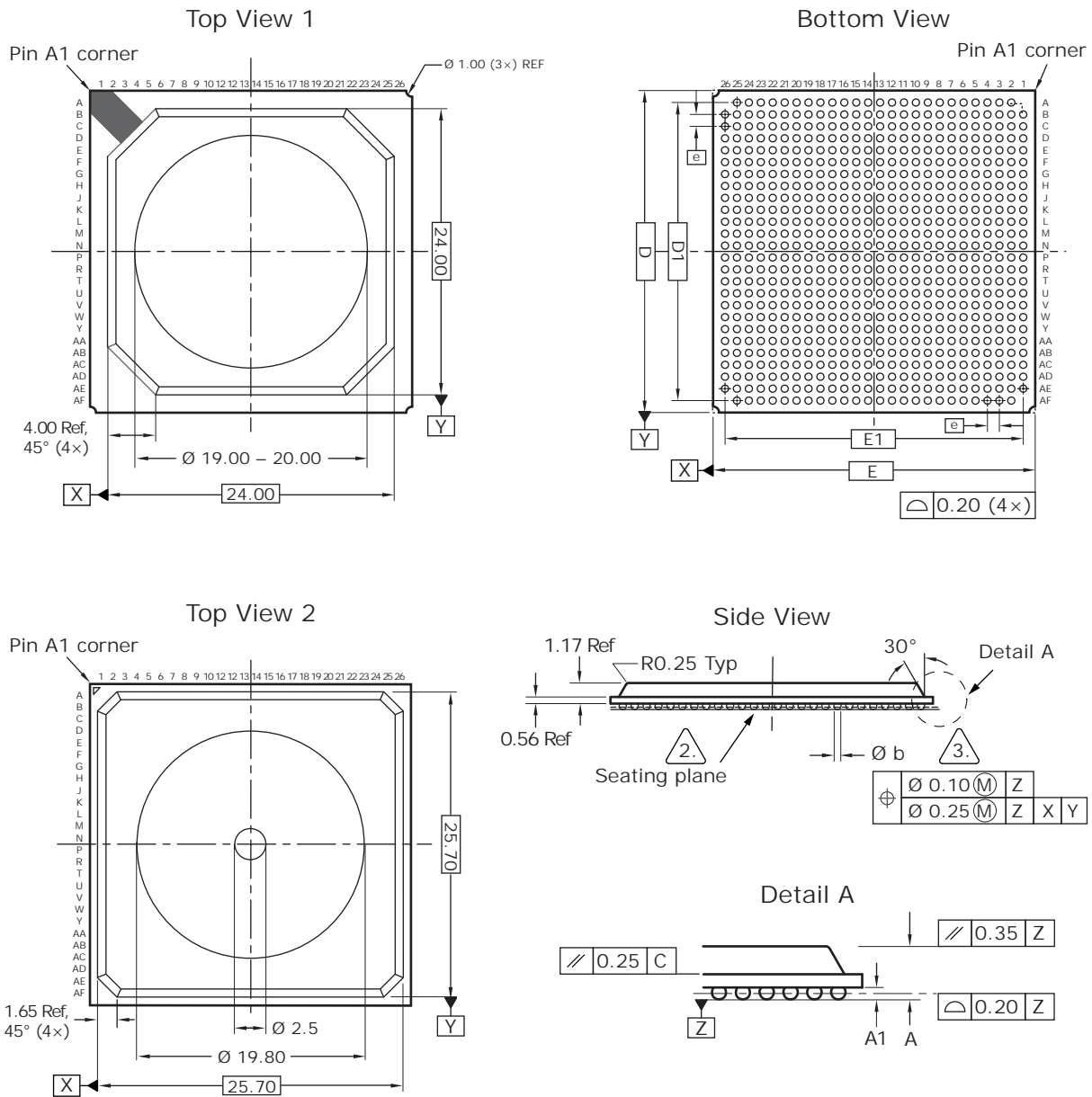
Lead-free products from Microsemi comply with the temperatures and profiles defined in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

This section provides the package drawing, thermal specifications, and moisture sensitivity rating for the device.

8.1 Package Drawing

The following illustration shows the package drawing for the device. The drawing contains two top views, a bottom view, a side view, a detail view, dimensions, tolerances, and notes. The top views reflect one of two packages customers can expect to receive.

Figure 40 • **Package Drawing**

Top View 1

Bottom View

Top View 2

Side View

Detail A

Dimensions and Tolerances

Reference	Minimum	Nominal	Maximum
A	2.10	2.23	2.44
A1	0.40	0.50	0.60
D		27.00	
E		27.00	
D1		25.00	
E1		25.00	
e		1.00	
b	0.50	0.60	0.70

Notes
1. All dimensions and tolerances are in millimeters (mm).
2. Primary datum Z and seating plane are defined by the spherical crowns of the solder balls.
3. Dimension is measured at the maximum solder ball diameter, parallel to primary datum C.
4. Radial true position is represented by typical values.
5. Top view 1 and top view 2 reflect one of two packages customers can expect to receive.

8.2 Thermal Specifications

Thermal specifications for this device are based on the JEDEC JESD51 family of documents. These documents are available on the JEDEC Web site at www.jedec.org. The thermal specifications are

modeled using a four-layer test board with two signal layers, a power plane, and a ground plane (2s2p PCB). For more information about the thermal measurement method used for this device, see the JESD51-1 standard.

Table 131 • **Thermal Resistances**

Symbol	°C/W	Parameter
θ_{JCtop}	3.27	Die junction to package case top
θ_{JB}	6.03	Die junction to printed circuit board
θ_{JA}	12.14	Die junction to ambient
θ_{JMA} at 1 m/s	9.42	Die junction to moving air measured at an air speed of 1 m/s
θ_{JMA} at 2 m/s	8	Die junction to moving air measured at an air speed of 2 m/s

To achieve results similar to the modeled thermal measurements, the guidelines for board design described in the JESD51 family of publications must be applied. For information about applications using BGA packages, see the following:

- JESD51-2A, *Integrated Circuits Thermal Test Method Environmental Conditions, Natural Convection (Still Air)*
- JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions, Forced Convection (Moving Air)*
- JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions, Junction-to-Board*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

8.3 Moisture Sensitivity

This device is rated moisture sensitivity level 4 as specified in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

9　Design Considerations

This section provides information about the design considerations for the VSC8512-02 device.

9.1　10BASE-T mode unable to re-establish link

10BASE-T mode is unable to re-establish link with the following devices if the link drops while sending data: SparX-III™ and Caracal™ family of switches, VSC8512-02, VSC8522-02, VSC8522-12, VSC8504, VSC8552, VSC8572, and VSC8574. No issue is observed for other link partner devices. The probability of this error occurring is low except in a test environment.

The workaround is to contact Microsemi for the current API software release.

This item was previously published in the VSC8512-02 Errata revision 1.0 as EA100054.

9.2　Link status for 100BASE-FX operation

SerDes media link status bit in register 24E3, bit 2 only reflects the status when the media type is 1000BASE-X. This bit is always 0 when the media type is 100BASE-FX.

The workaround is to verify that register 28, bits 1:0 media operating mode status is 10 for fiber media, register 28, bits 4:3 speed status is 01 for 100BASE-FX, and register 16, bit 12 link status is 1 for 100BASE-FX mode.

This item was previously published in the VSC8512-02 Errata revision 1.0 as EA100055.

9.3　Software script for link performance

Software script is required for improved link performance. PHY ports may exhibit suboptimal performance. Contact Microsemi for a script to be applied during system initialization.

This item was previously published in the VSC8512-02 Errata revision 1.0 as EA100034.

9.4　10BASE-T signal amplitude

10BASE-T signal amplitude can be lower than the minimum specified in IEEE 802.3 paragraph 14.3.1.2.1 (2.2 V) at low supply voltages. This issue is not estimated to present any system level impact. Performance is not impaired with cables up to 130 m with various link partners.

This item was previously published in the VSC8512-02 Errata revision 1.0 as EA100036.

9.5　Clause 45 register 7.60

Clause 45, register 7.60, bit 10 reads back as a logic 1. This is a reserved bit in the standard and should be ignored by software.

This item was previously published in the VSC8512-02 Errata revision 1.0 as EA100037.

9.6　Clause 45 register 3.22

Clause 45, register 3.22 is cleared upon read only when extended page access register (register 31) is set to 0. This register cannot be read when page access register is set to a value other than 0.

The workaround is to set the extended page access register to 0 before accessing clause 45, register 3.22.

This item was previously published in the VSC8512-02 Errata revision 1.0 as EA100038.

9.7　Clause 45 register 3.1

Clause 45, register 3.1, Rx and Tx LPI received bits are cleared upon read only when extended page access register (register 31) is set to 0.

The workaround is to set the extended page access register to 0 before accessing clause 45, register 3.1.

This item was previously published in the VSC8512-02 Errata revision 1.0 as EA100039.

9.8 Clause 45 register address post-increment

Clause 45 register address post-increment only works when reading registers and only when the extended page access register (register 31) is set to 0. The estimated impact is low, as there are very few Clause 45 registers in a Gigabit PHY, and they can be addressed individually.

The workaround is to access Clause 45 registers individually.

This item was previously published in the VSC8512-02 Errata revision 1.0 as EA100040.

10 Ordering Information

The VSC8512 device is offered with two operating temperature ranges. The range for VSC8512-02 is 0 °C ambient to 125 °C junction, and the range for VSC8512-03 is –40 °C ambient to 125 °C junction.

VSC8512XJG-02 and VSC8512XJG-03 are packaged in a lead-free (Pb-free), 672-pin, thermally enhanced, plastic ball grid array (BGA) with a 27 mm × 27 mm body size, 1 mm pin pitch, and 2.44 mm maximum height.

Lead-free products from Microsemi comply with the temperatures and profiles defined in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

The following table lists the ordering information for the device.

Table 132 • **Ordering Information**

Part Order Number	Description
VSC8512XJG-02	Lead-free, 672-pin, thermally enhanced, plastic BGA with a 27 mm × 27 mm body size, 1 mm pin pitch, and 2.44 mm maximum height. The operating temperature is 0 °C ambient to 125 °C junction.
VSC8512XJG-03	Lead-free, 672-pin, thermally enhanced, plastic BGA with a 27 mm × 27 mm body size, 1 mm pin pitch, and 2.44 mm maximum height. The operating temperature is –40 °C ambient to 125 °C junction.