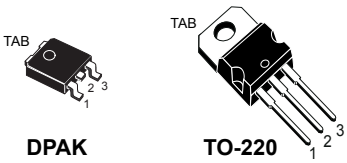
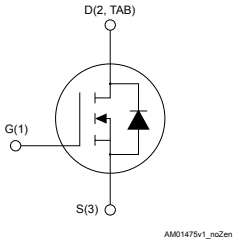
Datasheet

N-channel 550 V, 0.150 Ω typ., 16 A MDmesh M5 Power MOSFETs in a DPAK and TO-220 packages



DPAK **TO-220**



Features

Order code	V_{DS} @ $T_{jmax.}$	$R_{DS(on)}$max.	Package
STD18N55M5	600 V	0.192 Ω	DPAK
STP18N55M5			TO-220

- Extremely low $R_{DS(on)}$
- Low gate charge and input capacitance
- Excellent switching performance
- 100% avalanche tested

Applications

- Switching applications

Description

These devices are N-channel Power MOSFETs based on the MDmesh M5 innovative vertical process technology combined with the well-known PowerMESH horizontal layout. The resulting products offer extremely low on-resistance, making them particularly suitable for applications requiring high power and superior efficiency.

Product status link
STD18N55M5
STP18N55M5

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	±25	V
I_D	Drain current (continuous) at T_C = 25 °C	16	A
I_D	Drain current (continuous) at T_C = 100 °C	10	A
I_{DM} (1)	Drain current (pulsed)	64	A
P_{TOT}	Total power dissipation at T_C = 25 °C	110	W
dv/dt (2)	Peak diode recovery voltage slope	15	V/ns
T_j	Operating junction temperature range	-55 to 150	°C
T_{stg}	Storage temperature range		

1. *Pulse width limited by safe operating area.*
2. *I_{SD} ≤ 16 A, di/dt ≤ 400 A/µs; $V_{DS\ peak}$ < $V_{(BR)DSS}$, V_{DD} = 340 V.*

Table 2. Thermal data

Symbol	Parameter	Value		Unit
		DPAK	TO-220	
R_{thJC}	Thermal resistance, junction-to-case	1.14		°C/W
R_{thJA}	Thermal resistance, junction-to-ambient		62.5	°C/W
R_{thJB} (1)	Thermal resistance, junction-to-board	50		°C/W

1. *When mounted on an 1-inch² FR-4, 2oz Cu board.*

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j Max)	4	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, I_D = I_{AR}, V_{DD} = 50 V)	210	mJ

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown voltage	I_D = 1 mA, V_{GS} = 0 V	550			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 550 V			1	µA
		V_{GS} = 0 V, V_{DS} = 550 V, T_C = 125 °C(1)			100	µA
I_{GSS}	Gate body leakage current	V_{DS} = 0 V, V_{GS} = ±25 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 8 A		0.150	0.192	Ω

1. *Defined by design, not subject to production test.*

Table 5. Dynamic

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 100 V, f = 1 MHz, V_{GS} = 0 V	-	1260	-	pF
C_{oss}	Output capacitance			42		
C_{rss}	Reverse transfer capacitance			3.6		
$C_{o(tr)}$ (1)	Equivalent capacitance time related	V_{DS} = 0 to 440 V, V_{GS} = 0 V	-	103	-	pF
$C_{o(er)}$ (2)	Equivalent capacitance energy related		-	35	-	pF
Rg	Gate input resistance	f = 1 MHz open drain	-	2.8	-	Ω
Q_g	Total gate charge	V_{DD} = 440 V, I_D = 8 A, V_{GS} = 0 to 10 V (see Figure 18. Test circuit for gate charge behavior)	-	31	-	nC
Q_{gs}	Gate-source charge			8.3		
Q_{gd}	Gate-drain charge			14.2		

1. *Time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.*
2. *Energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}.*

Table 6. Switching times

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{d(v)}$	Voltage delay time	V_{DD} = 400 V, I_D = 10.5 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 19. Test circuit for inductive load switching and diode recovery times and Figure 22. Switching time waveform)	-	37	-	ns
$t_{r(v)}$	Voltage rise time			7		
$t_{c(off)}$	Crossing time			10.3		
$t_{f(i)}$	Current fall time			8.3		

Table 7. Source drain diode

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		16	A
I_{SDM} (1)	Source-drain current (pulsed)				64	
V_{SD} (2)	Forward on voltage	I_{SD} = 16 A, V_{GS} = 0 V	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 16 A, di/dt = 100 A/µs	-	244		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 100 V (see Figure 19. Test circuit for inductive load switching and diode recovery times)		2.8		µC
I_{RRM}	Reverse recovery current			23		A
t_{rr}	Reverse recovery time	I_{SD} = 16 A, di/dt = 100 A/µs	-	295		ns
Q_{rr}	Reverse recovery charge	V_{DD} = 100 V, Tj = 150 °C (see Figure 19. Test circuit for inductive load switching and diode recovery times)		3.7		µC
I_{RRM}	Reverse recovery current			25		A

1. *Pulse width limited by safe operating area.*
2. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%.*

2.1 Electrical characteristics curves

Figure 1. Safe operating area for DPAK

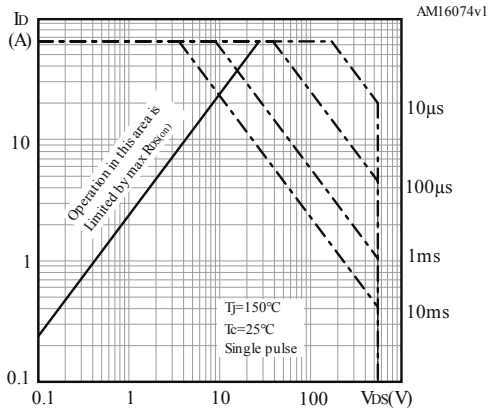


Figure 2. Thermal impedance for DPAK

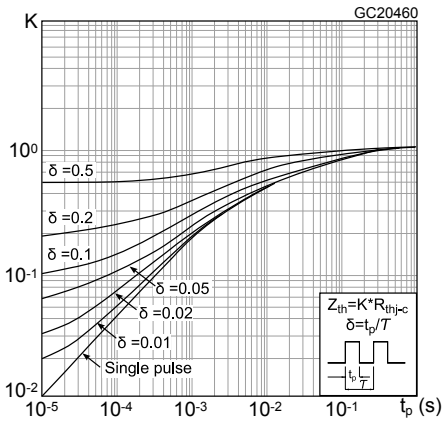


Figure 3. Safe operating area for TO-220

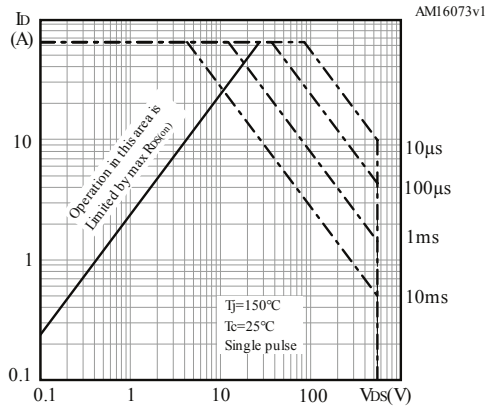


Figure 4. Thermal impedance for TO-220

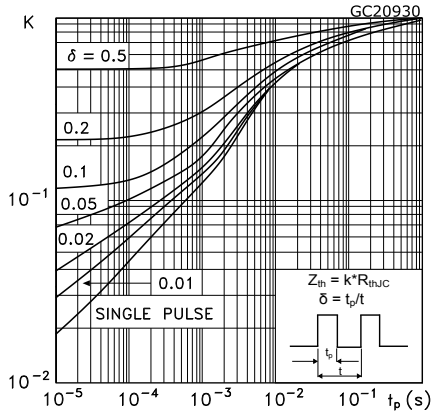


Figure 5. Output characterisics

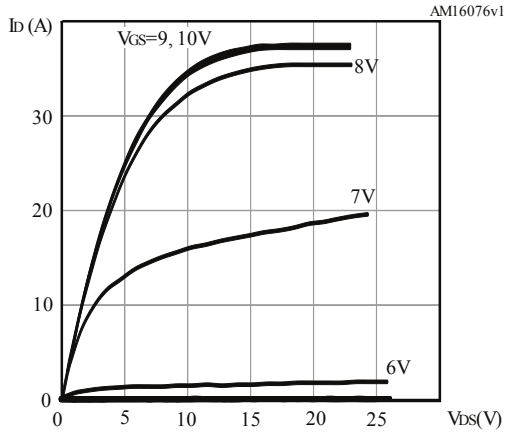


Figure 6. Transfer characteristics

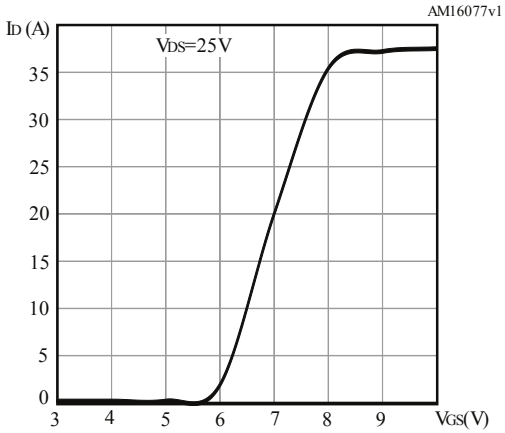


Figure 7. Gate charge vs gate-source voltage

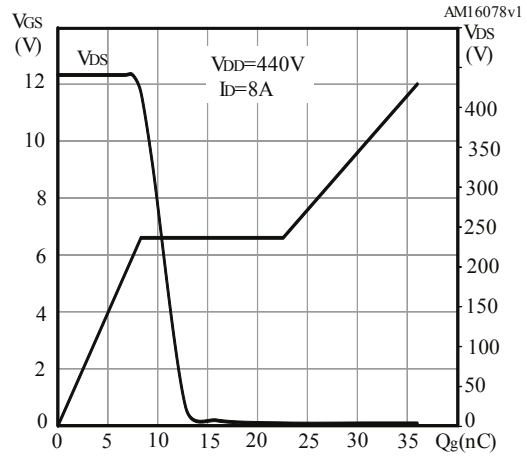


Figure 8. Static drain-source on resistance

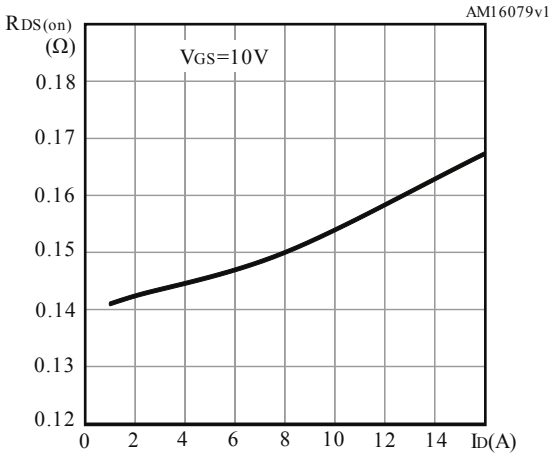


Figure 9. Capacitance variations

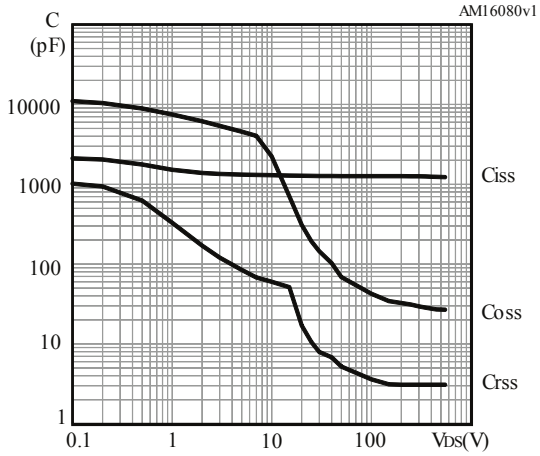


Figure 10. Output capacitance stored energy

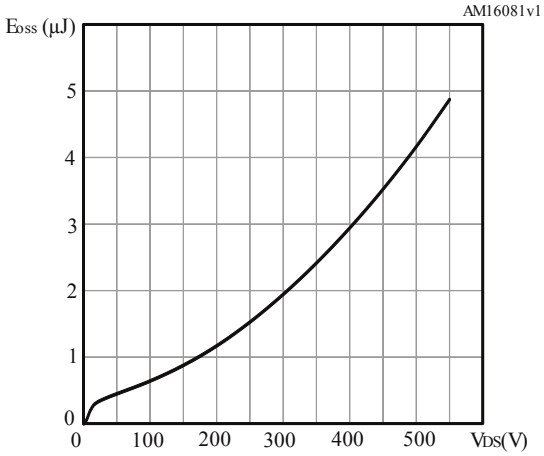


Figure 11. Normalized gate threshold voltage vs temperature

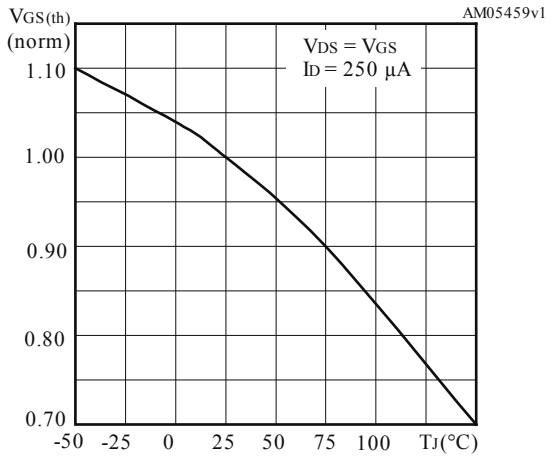


Figure 12. Normalized on-resistance vs temperature

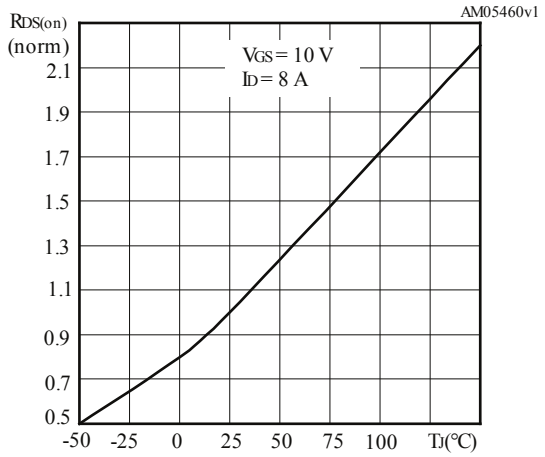


Figure 13. Drain-source diode forward characteristics

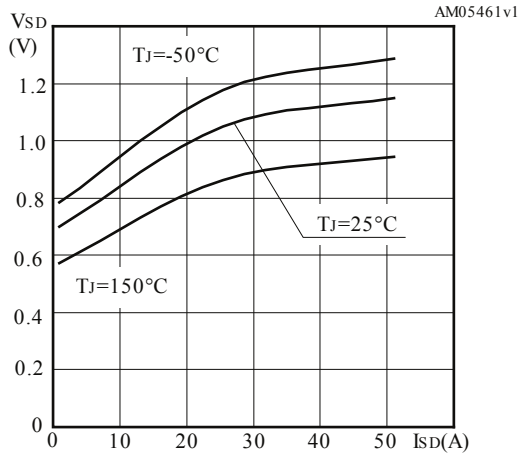


Figure 14. Normalized $V_{(BR)DSS}$ vs temperature

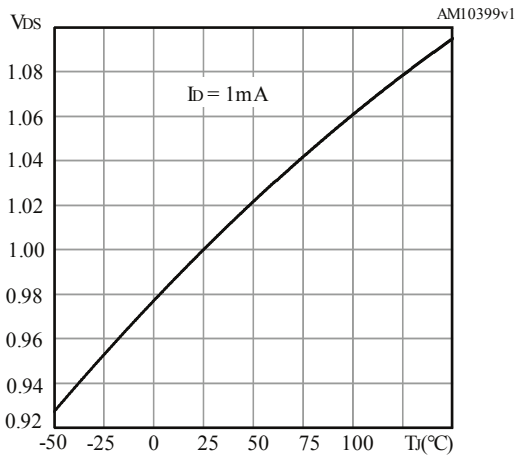
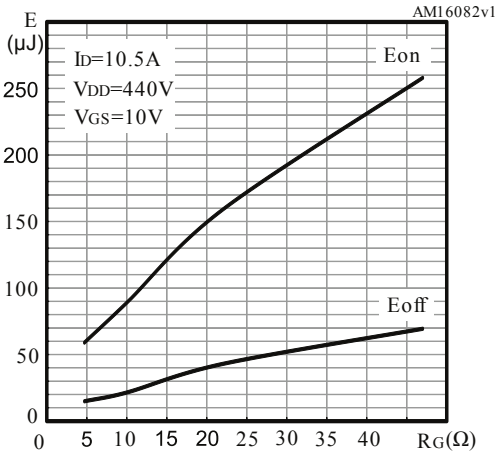


Figure 15. Switching energy vs gate resistance



* Eon including reverse recovery of a SiC diode

3 Test circuits

Figure 16. Test circuit for resistive load switching times

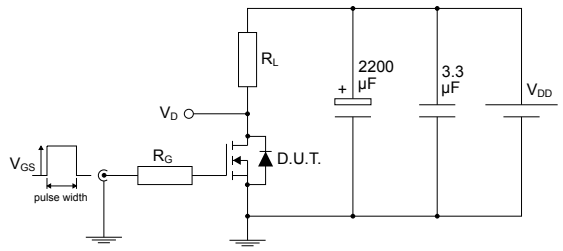


Figure 17. Test circuit for gate charge behavior

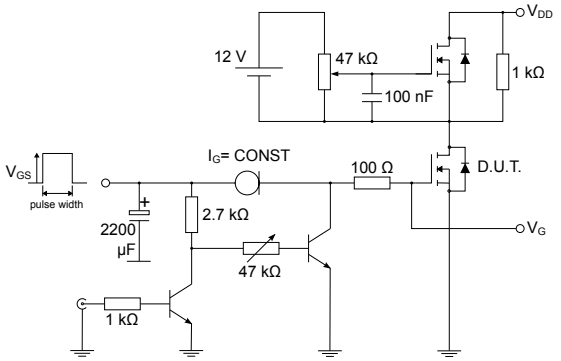


Figure 18. Test circuit for inductive load switching and diode recovery times

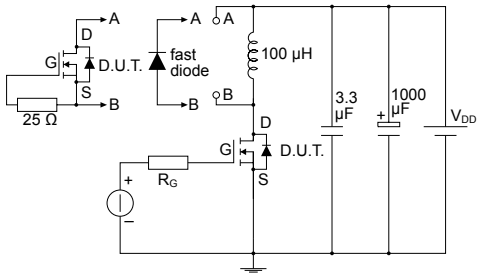


Figure 19. Unclamped inductive load test circuit

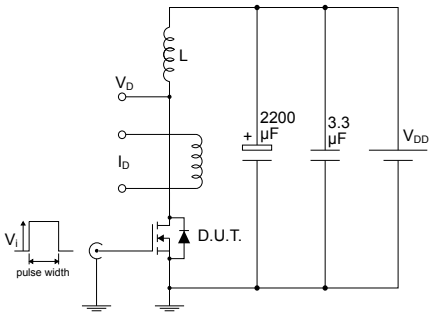


Figure 20. Unclamped inductive waveform

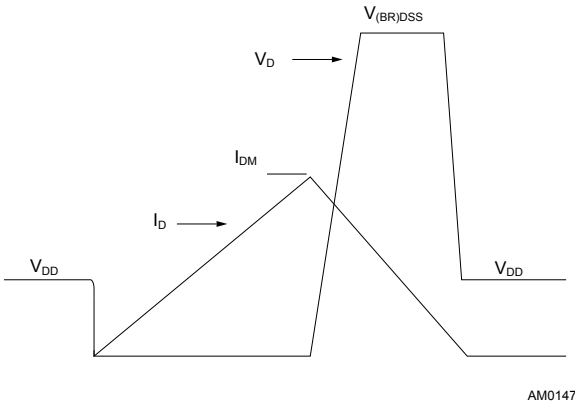
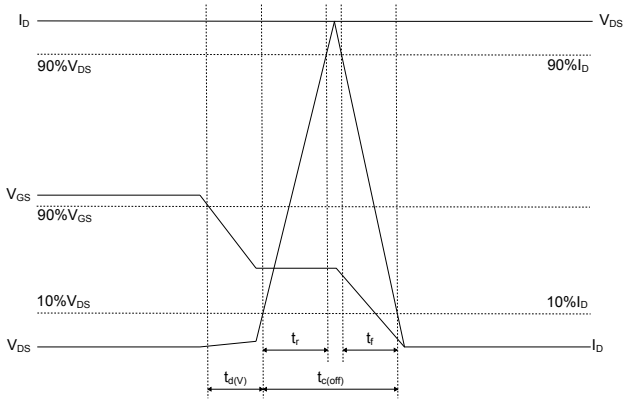


Figure 21. Switching time waveform

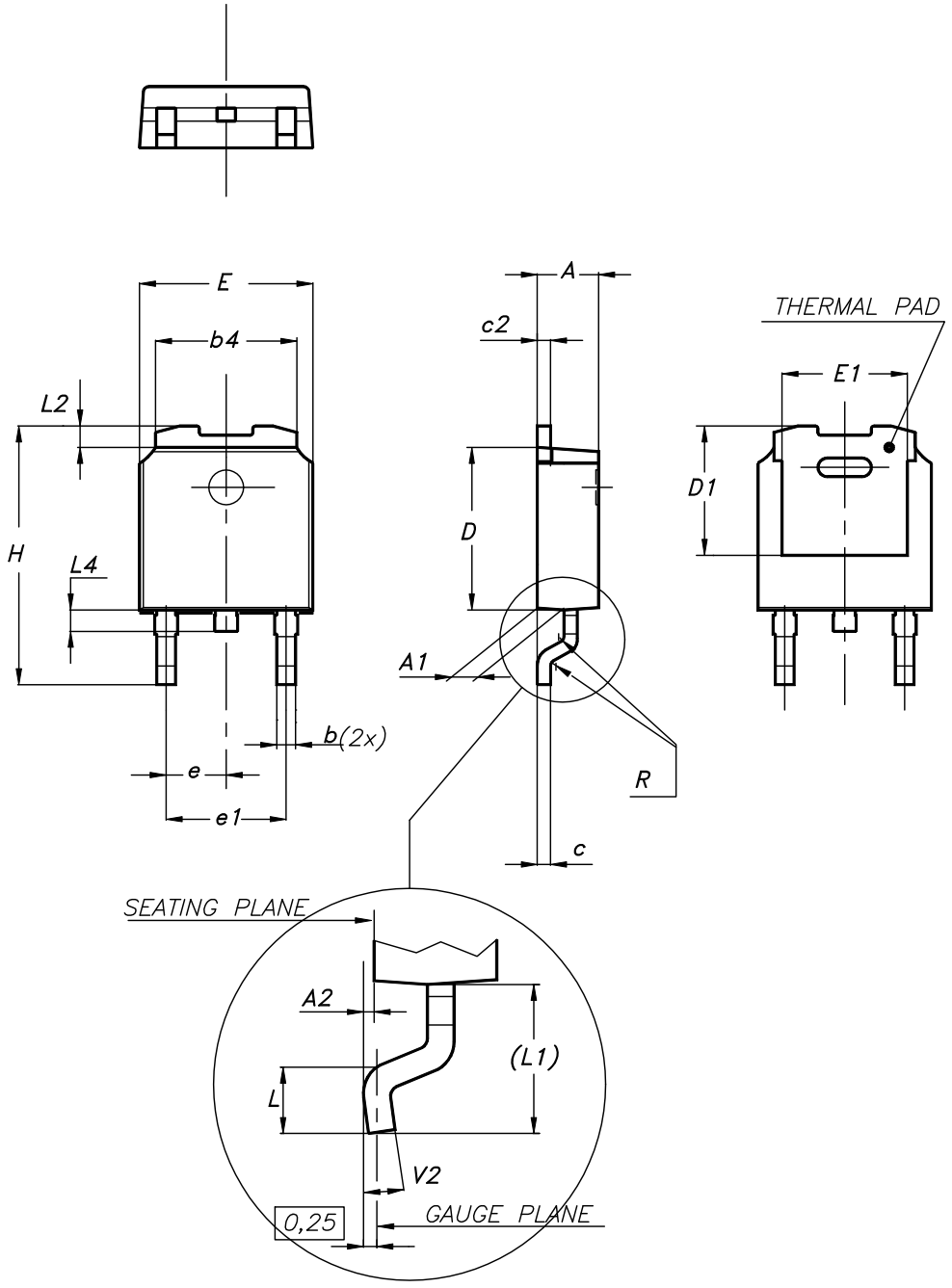


4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 DPAK (TO-252) type A2 package information

Figure 22. **DPAK (TO-252) type A2 package outline**



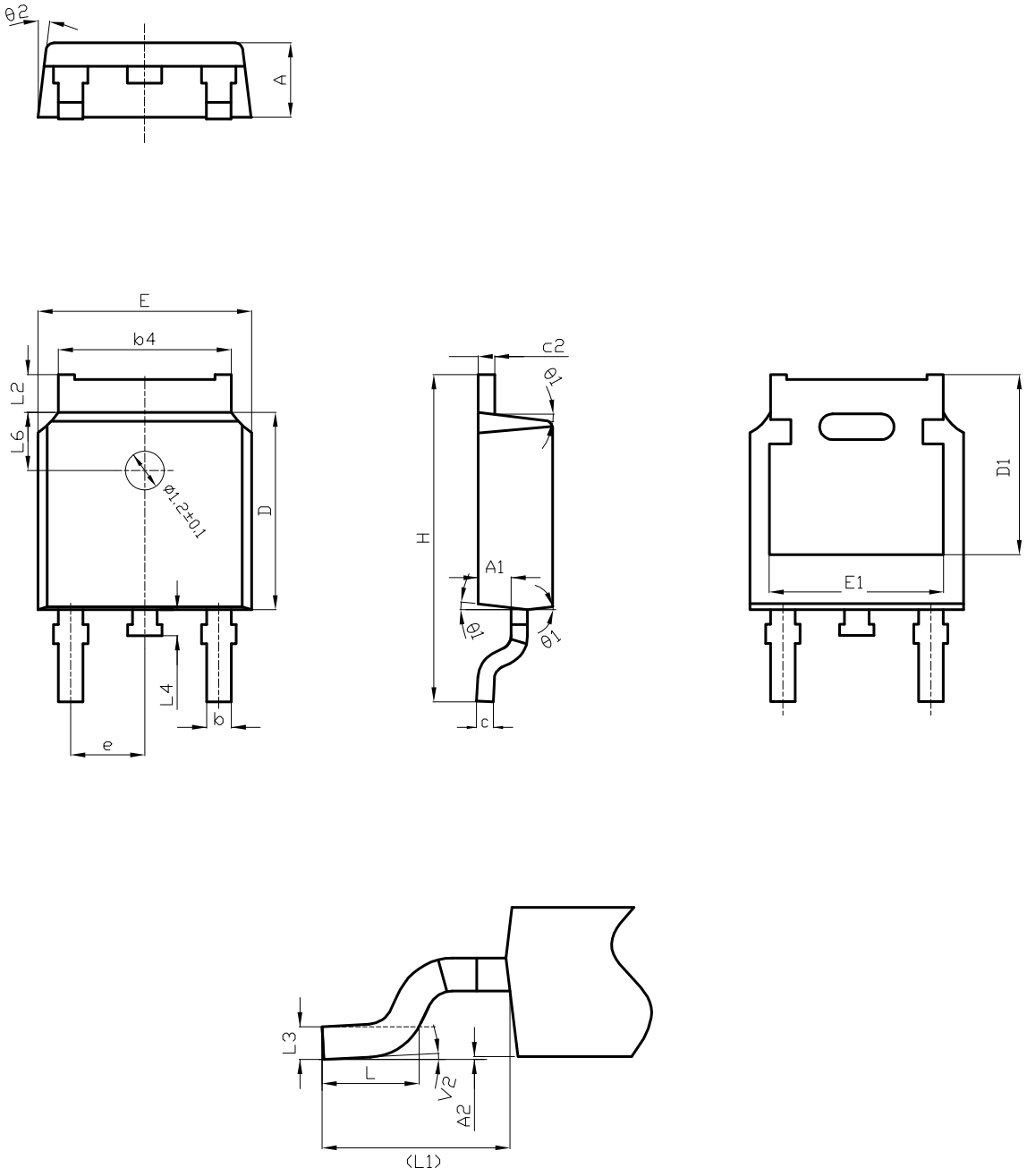
0068772_type-A2_rev30

Table 8. **DPAK (TO-252) type A2 mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	5.10	5.20	5.30
e	2.159	2.286	2.413
e1	4.445	4.572	4.699
H	9.35		10.10
L	1.00		1.50
L1	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

4.2 DPAK (TO-252) type C2 package information

Figure 23. **DPAK (TO-252) type C2 package outline**

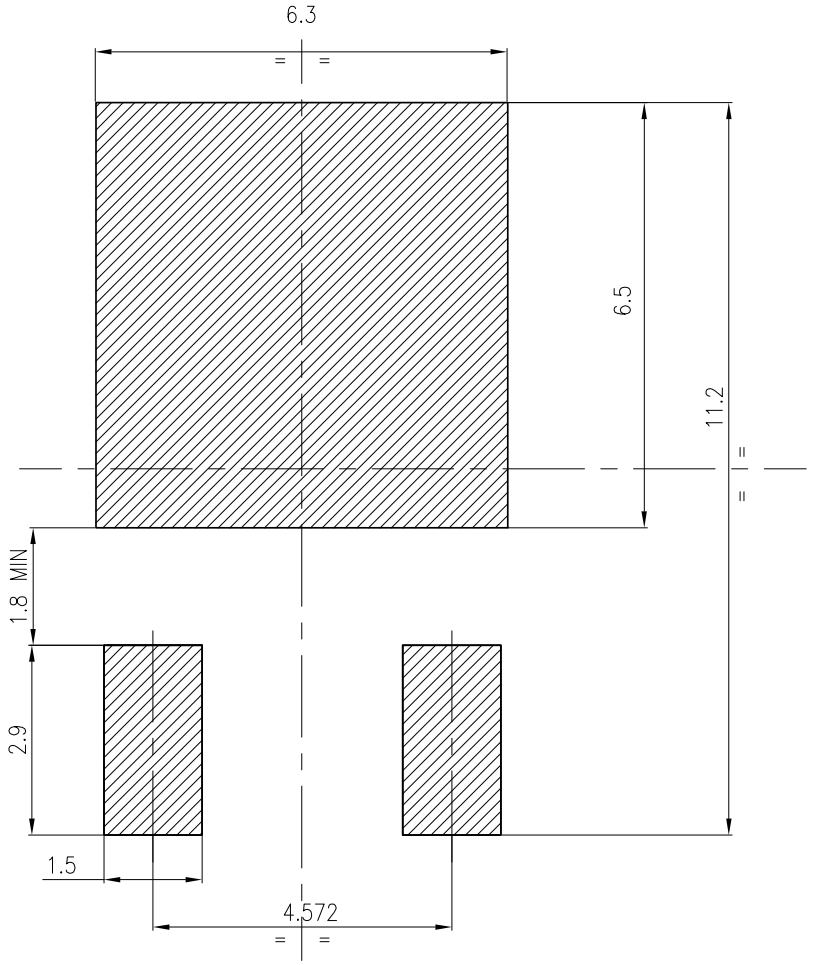


0068772_type-C2_rev30

Table 9. DPAK (TO-252) type C2 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.38
A1	0.90	1.01	1.10
A2	0.00		0.10
b	0.72		0.85
b4	5.13	5.33	5.46
c	0.47		0.60
c2	0.47		0.60
D	6.00	6.10	6.20
D1	5.10		5.60
E	6.50	6.60	6.70
E1	5.20		5.50
e	2.186	2.286	2.386
H	9.80	10.10	10.40
L	1.40	1.50	1.70
L1		2.90 REF	
L2	0.90		1.25
L3		0.51 BSC	
L4	0.60	0.80	1.00
L6		1.80 BSC	
θ1	5°	7°	9°
θ2	5°	7°	9°
V2	0°		8°

Figure 24. DPAK (TO-252) recommended footprint (dimensions are in mm)



4.3 DPAK (TO-252) packing information

Figure 25. **DPAK (TO-252) tape outline**

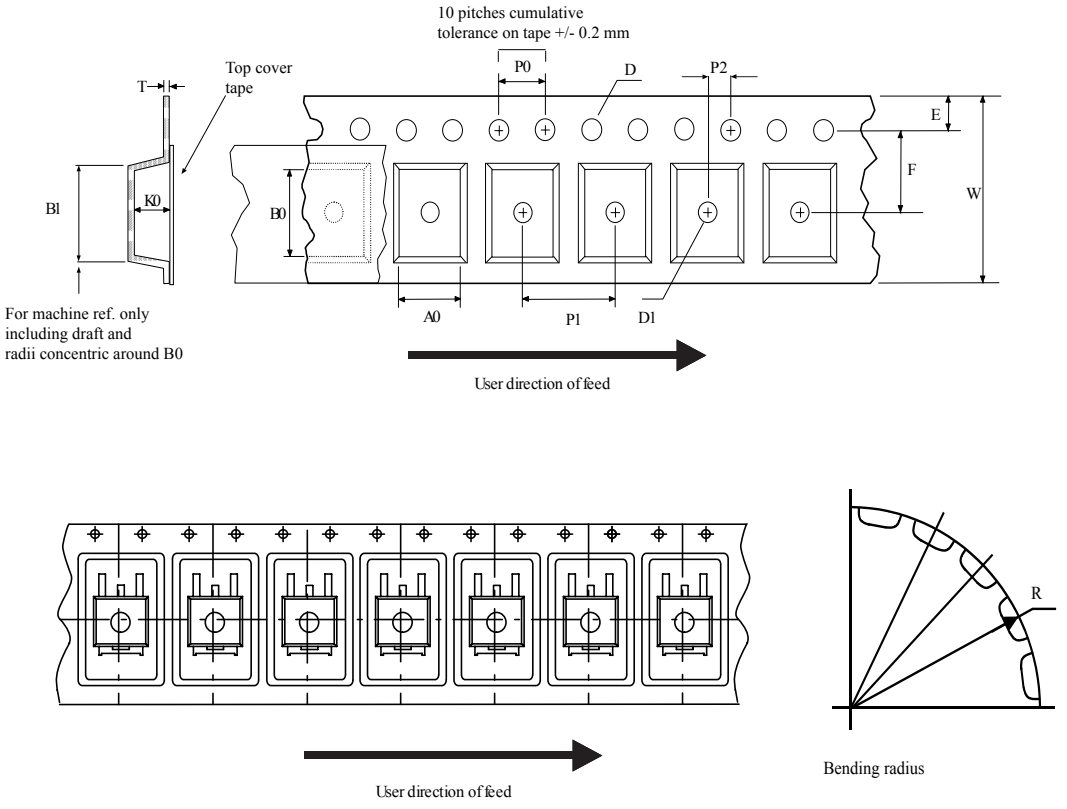


Figure 26. **DPAK (TO-252) reel outline**

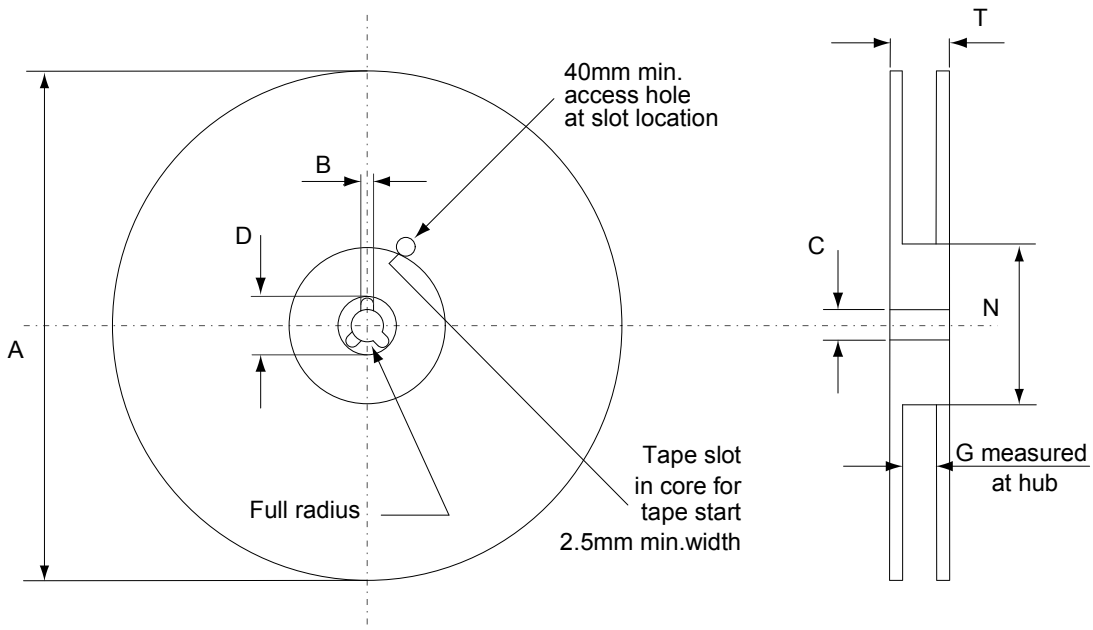


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Table 10. **DPAK (TO-252) tape and reel mechanical data**

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

4.4 TO-220 type A package information

Figure 27. **TO-220 type A package outline**

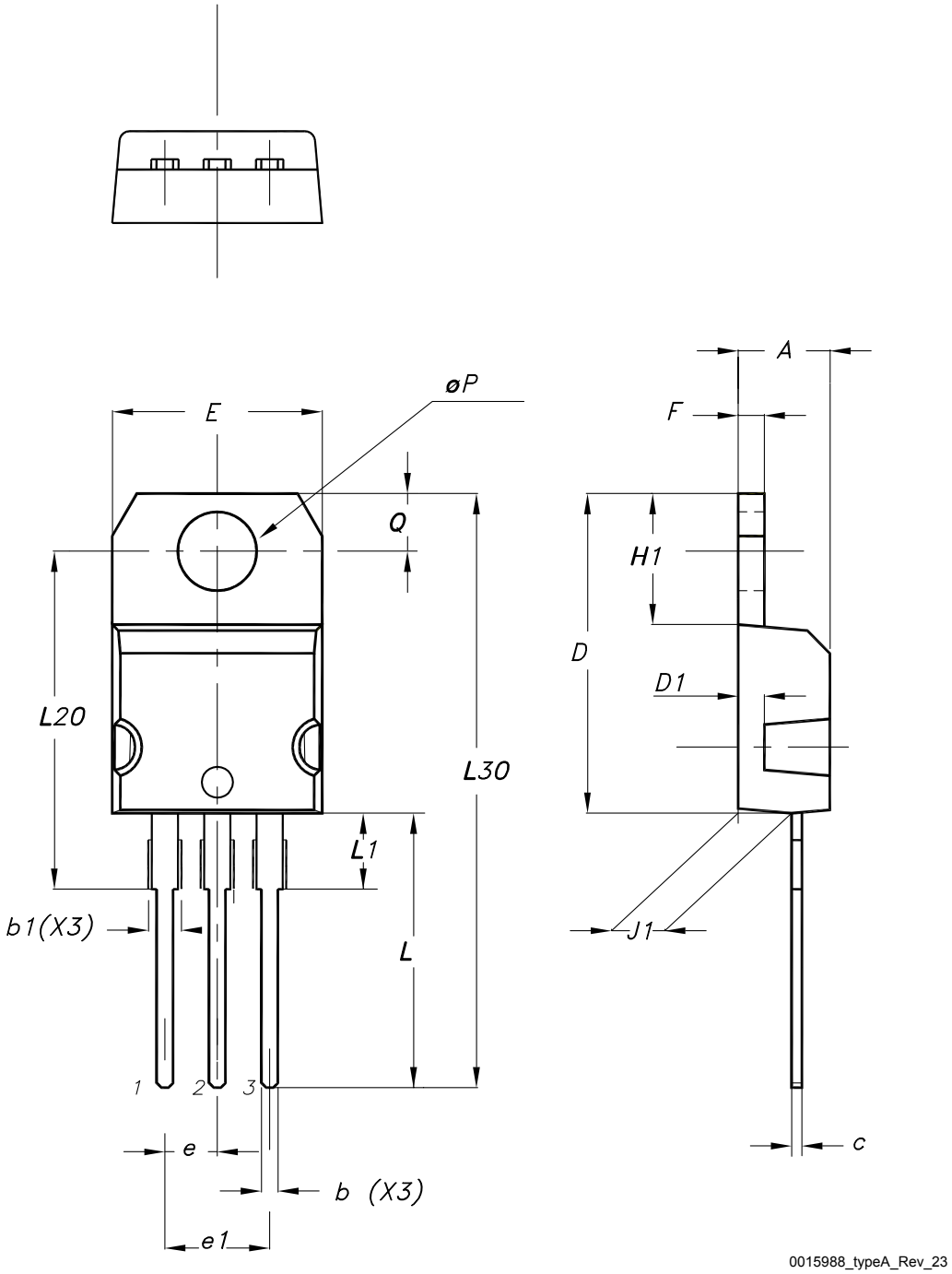

Table 11. **TO-220 type A package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.55
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10.00		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13.00		14.00
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95
Slug flatness		0.03	0.10

5 Ordering information

Table 12. **Order codes**

Order code	Marking	Package	Packing
STD18N55M5	18N55M5	DPAK	Tape and reel
STP18N55M5		TO-220	Tube

Revision history

Table 13. **Document revision history**

Date	Version	Changes
09-Feb-2010	1	First release.
04-Mar-2011	2	– Document status promoted from preliminary data to datasheet; – Added new package, mechanical data: D²PAK.
22-Nov-2013	3	– Updated: title on the cover page and RDS(on) values. – Modified: EAS value and note 3 in Table 2 – Modified: RDS(on) value in Table 4, typical values in Table 5 and 7 – Updated: the entire Table 5 – Added: Section 2.1: Electrical characteristics (curves) – Updated: Section 4: Package mechanical data and Section 5: Packaging mechanical data – Updated: Figure 11 and 18 – Minor text changes.
03-Aug-2018	4	The part numbers STB18N55M5 and STF18N55M5 have been moved to a separate datasheet. Removed maturity status indication from cover page. The document status is production data. Updated title in cover page, Section 1 Electrical ratings, Section 2 Electrical characteristics and Section 4 Package information. Minor text changes.
24-Mar-2020	5	Updated title on Figure 12. Normalized gate threshold voltage vs temperature and Figure 13. Normalized on-resistance vs temperature. Updated Section 4 Package information. Minor text changes.

Contents