



Product Change Notification / SYST-03DPVL777

Date:

04-Mar-2014

Product Category:

32-bit Microcontrollers

PCN Type:

Document Change

Notification Subject:

Data Sheet - PIC32MX1XX/2XX Family Data Sheet Data Sheet Document Revision

Affected CPNs:

[SYST-03DPVL777_Affected_CPN_03042014.pdf](#)

[SYST-03DPVL777_Affected_CPN_03042014.csv](#)

Notification Text:

SYST-03DPVL777

Microchip has released a new DeviceDoc for the PIC32MX1XX/2XX Family Data Sheet of devices. If you are using one of these devices please read the document located at [PIC32MX1XX/2XX Family Data Sheet](#).

Notification Status: Final

Description of Change:

- 1) 32-bit Microcontrollers (up to 256 KB Flash and 64 KB SRAM) with Audio and Graphics Interfaces, USB, and Advanced Analog
 - * Added new devices to the family features (see Table 1 and Table 2).
 - * Updated pin diagrams to include new devices (see "Pin Diagrams").
- 2) Section 1.0 "Device Overview"
 - * Added Note 3 reference to the following pin names: Vbus, Vusb3v3, Vbuson, D+, D-, and USBID.
- 3) Section 2.0 "Guidelines for Getting Started with 32-bit MCUs"
 - * Replaced Figure 2-1: Recommended Minimum Connection.
 - * Updated Figure 2-2: MCLR Pin Connections.
 - * Added 2.9 "SOSC Design Recommendation".
- 4) Section 4.0 "Memory Organization"
 - * Added memory tables for devices with 64 KB RAM (see Table 4-4 through Table 4-5).
 - * Changed the Virtual Addresses for all registers and updated the PWP bits in the DEVCFG: Device Configuration Word Summary (see Table 4-17).
 - * Updated the ODCA, ODCB, and ODCC port registers (see Table 4-19, Table 4-20, and Table 4-21).

- * The RTCTIME, RTCDATE, ALRMTIME, and ALRMDATE registers were updated (see Table 4-25).
 - * Added Data Ram Size value for 64 KB RAM devices (see Register 4-5).
 - * Added Program Flash Size value for 256 KB Flash devices (see Register 4-5).
- 5) Section 12.0 "Timer1"
- * The Timer1 block diagram was updated to include the 16-bit data bus (see Figure 12-1).
- 6) Section 13.0 "Timer2/3, Timer4/5"
- * The Timer2-Timer5 block diagram (16-bit) was updated to include the 16-bit data bus (see Figure 13-1).
 - * The Timer2/3, Timer4/5 block diagram (32-bit) was updated to include the 32-bit data bus (see Figure 13-1).
- 7) Section 19.0 "Parallel Master Port (PMP)"
- * The CSF<1:0> bit value definitions for '00' and '01' were updated (see Register 19-1).
 - * Bit 14 in the Parallel Port Address register (PMADDR) was updated (see Register 19-3).
- 8) Section 20.0 "Real-Time Clock and Calendar (RTCC)"
- * The following registers were updated: RTCTIME (see Register 20-3), RTCDATE (see Register 20-4), ALRMTIME (see Register 20-5), and ALRMDATE (see Register 20-6).
- 9) Section 26.0 "Special Features"
- * Updated the PWP bits (see Register 26-1).
- 10) Section 29.0 "Electrical Characteristics"
- * Added parameters DO50 and DO50a to the Capacitive Loading Requirements on Output Pins (see Table 29-14).
 - * Added Note 5 to the IDD DC Characteristics (see Table 29-5).
 - * Added Note 4 to the IDLE DC Characteristics (see Table 29-6).
 - * Added Note 5 to the IPD DC Characteristics (see Table 29-7).
 - * Updated the conditions for parameters USB321 (VOL) and USB322 (VOH) in the OTG Electrical Specifications (see Table 29-38).
- 11) Product Identification System
- * Added 40 MHz speed information.

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 04 Mar 2014

NOTE: Please be advised that this is a change to the document only the product has not been changed..

Markings to Distinguish Revised from Unrevised Devices: N/A

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