AN_1x22_020 June 2008

73M1x22 Worldwide Design Guide

Introduction

This application note provides guidelines and recommendations for the configuration and use of the 73M1822 and 73M1922 in preparing for worldwide homologation. These integrated circuits will be collectively referred to as the 73M1x22 in this document.

Designing for worldwide homologation is an extensive subject. This application note provides information for initial consideration. It is the intention of Teridian to expand and enhance this application note on a regular basis. For the latest version of this document, contact any sales office of Teridian Semiconductor Corporation.

The 73M1x22 MircoDAA provides the user with highly integrated, globally compliant, silicon DAA for ultra low-cost voice band data and fax applications. The global-compliance parameters, which provide the necessary functionality and the protection required for worldwide homologation, are programmable.

This application note describes the following built-in features for global configurations:

- AC Termination Impedance
- DC Mask Control
- Ring Detector Threshold

The final section gives an example of the 73M1x22 MicroDAA initialization sequence.

For additional information on the registers and bits, refer to the appropriate data sheet.

AC Termination Impedance

The AC termination impedance is set by selecting the ACZ bit settings in Register 0x17[4:3]. Table 1 provides AC termination impedance settings for a number of countries.

There are several different AC termination impedances that are used worldwide. Typical AC termination requirements are either 600 Ω resistive or a specific complex impedance (resistor/capacitor network) termination such as TBR-21 or Australian. See Table 2 for a complete list of terminations supported by the 73M1x22.

The match of a device's termination impedance to the line impedance determines the return loss figure. With the following settings, a single design can be used worldwide without the need for hardware changes for specific countries.

Table 1: Worldwide AC Impedance Setting

Country	AC term	ACZ(1:0)	Country	AC term	ACZ(1:0)	Country	AC term	ACZ(1:0)
Argentina	600	00	Hungary[1]	600	10	Pakistan	600	00
Australia	Complex	11	Iceland[2]	Complex	10	Peru	600	00
Austria[1]	Complex	10	India	Complex	00	Philippines	600	00
Bahrain	Complex	00	Indonesia	600	00	Poland[1]	600	10
Belgium[1]	Complex	10	Ireland[1]	Complex	10	Portugal[1]	Complex	10
Bolivia	600	00	Israel	Complex	00	Romania[1]	600	10
Brazil	600	00	Italy[1]	Complex	10	Russia	600	00
Bulgaria[1]	Complex	10	Japan	600	00	Saudi Arabia	600	00
Canada	600	00	Jordan	600	00	Singapore	600	00
Chile	600	00	Kazakhstan	600	00	Slovakia[1]	Complex	10
China[3]	Complex	10	Kuwait	600	00	Slovenia[1]	Complex	10
Columbia	600	00	Latvia[1]	Complex	10	S. Africa[3]	Complex	11
Croatia	Complex	10	Lebanon	Complex	00	S. Korea	600	00
Cyprus[1]	Complex	10	Leichtenstein[2]	Complex	10	Spain[1]	Complex	10
Czech Rep[1]	Complex	10	Lithuania[1]	Complex	10	Sweden[1]	Complex	10
Denmark[1]	Complex	10	Luxembourg[1]	Complex	10	Switzerland[2]	Complex	01
Ecuador	600	00	Macao	600	00	Syria	600	00
Egypt	600	00	Malaysia	600	00	Taiwan	600	00
El Salvador	600	00	Malta[1]	Complex	10	TBR 21	Complex	10
Estonia[1]	Complex	10	Mexico	600	00	Thailand	600	00
Finland[1]	Complex	10	Morocco	Complex	00	Turkey	600	00
France[1]	Complex	10	Netherlands[1]	Complex	10	UAE	600	00
Germany[1]	Complex	10	New Zealand[3]	Complex	00	UK[1]	Complex	10
Greece[1]	Complex	10	Nigeria	Complex	00	Ukraine	600	00
Guam	600	00	Norway[2]	Complex	10	USA	600	00
Hong Kong	600	00	Oman	600	00	Yemen	600	00

[1] These countries are members of the European Union, where there are no longer any regulatory requirements for AC impedance. The suggested setting complies with TBR 21, a regulatory requirement that applied in the European Union up until 2001. Other settings can be used if desired.

[2] These countries are members of the European Free Trade Association, and their regulations generally follow the European Union model. The suggested setting complies with TBR 21.

[3] These countries can use the suggested complex setting for voice or data products. Optionally, data products can use 600 ohms.

Table 2 lists the termination impedances supported by the 73M1x22.

Table 2: Termination Impedances Supported by the 73M1x22

ACZ(1:0)	Impedance	Example Countries
00	600 Ω	US, Japan
01	270 Ω + 750 Ω || 150 nF	TBK-21
10	200 Ω + 680 Ω || 100 nF	China
11	220 Ω + 820 Ω || 115 nF	Australia

Figure 1 shows typical return loss characteristics as measured on the Teridian 73M1x22 Reference Board.

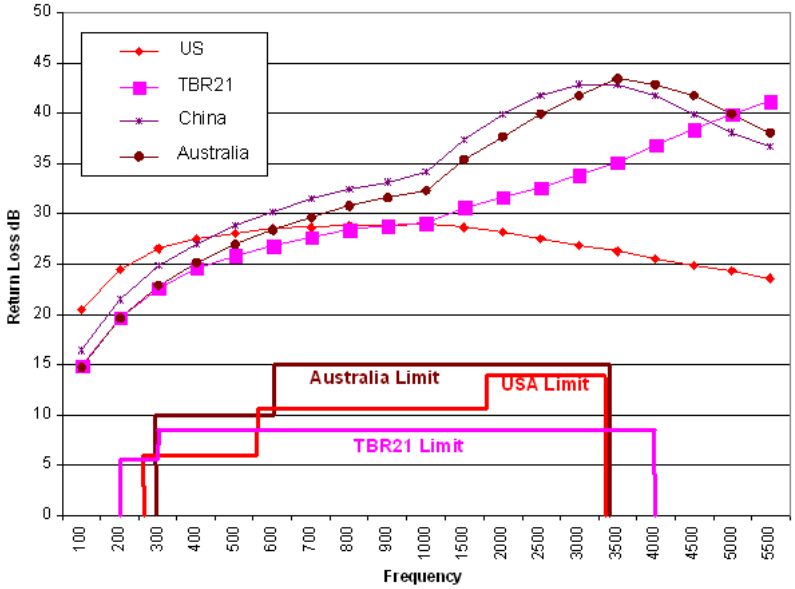

Figure 1: 73M1x22 Return Loss Characteristics

DC Mask Control

The DC mask control is set by selecting DCIV bit settings in Register 0x13[7:6]. Table 3 provides the DC mask settings for specific countries. The ILM bit in Register 0x13[5] controls the current limit mode. This was required for operation in France and former French colonies, but is no longer a requirement. Some applications may still require this feature for compatibility with legacy systems.

As each country regulates the AC termination, there are requirements for specific DC termination in some countries. The DC termination requirements can be measured by checking the DC mask compliances. Table 3 shows the recommended DC mask settings as set by the DCIV bits in Register 0x13[7:6]. See Figures 2 to 4 for measured results.

Table 1: Worldwide DC Mask Settings

Country	DCIV(1:0)	Country	DCIV(1:0)	Country	DCIV(1:0)
Argentina	10	Hungary	10	Pakistan	10
Australia	11	Iceland	10	Peru	10
Austria	10	India	10	Philippines	10
Bahrain	10	Indonesia	10	Poland	10
Belgium	10	Ireland	10	Portugal	10
Bolivia	10	Israel	10	Romania	10
Brazil	10	Italy	10	Russia	10
Bulgaria	10	Japan	00	Saudi Arabia	10
Canada	10	Jordan	10	Singapore	10
Chile	10	Kazakhstan	10	Slovakia	10
China	10	Kuwait	10	Slovenia	10
Columbia	10	Latvia	10	S. Africa	10
Croatia	10	Lebanon	10	S. Korea	10
Cyprus	10	Leichtenstein	10	Spain	10
Czech Rep	10	Lithuania	10	Sweden	10
Denmark	10	Luxembourg	10	Switzerland	10
Ecuador	10	Macao	10	Syria	10
Egypt	10	Malaysia	10	Taiwan	10
El Salvador	10	Malta	10	TBR 21	10
Estonia	10	Mexico	10	Thailand	10
Finland	10	Morocco	10	Turkey	10
France[1]	10[1]	Netherlands	10	UAE	10
Germany	10	New Zealand	10	UK	10
Greece	10	Nigeria	10	Ukraine	00
Guam	10	Norway	10	USA	10
Hong Kong	10	Oman	10	Yemen	10

[1] The setting for France can be used with current limiting mode enabled by setting the ILM bit in Register 0x13[5]. The use of current limiting is no longer a requirement for operation in France.

Figure 2 shows the DC line characteristics for the four DCVI1/DCVI0 settings.

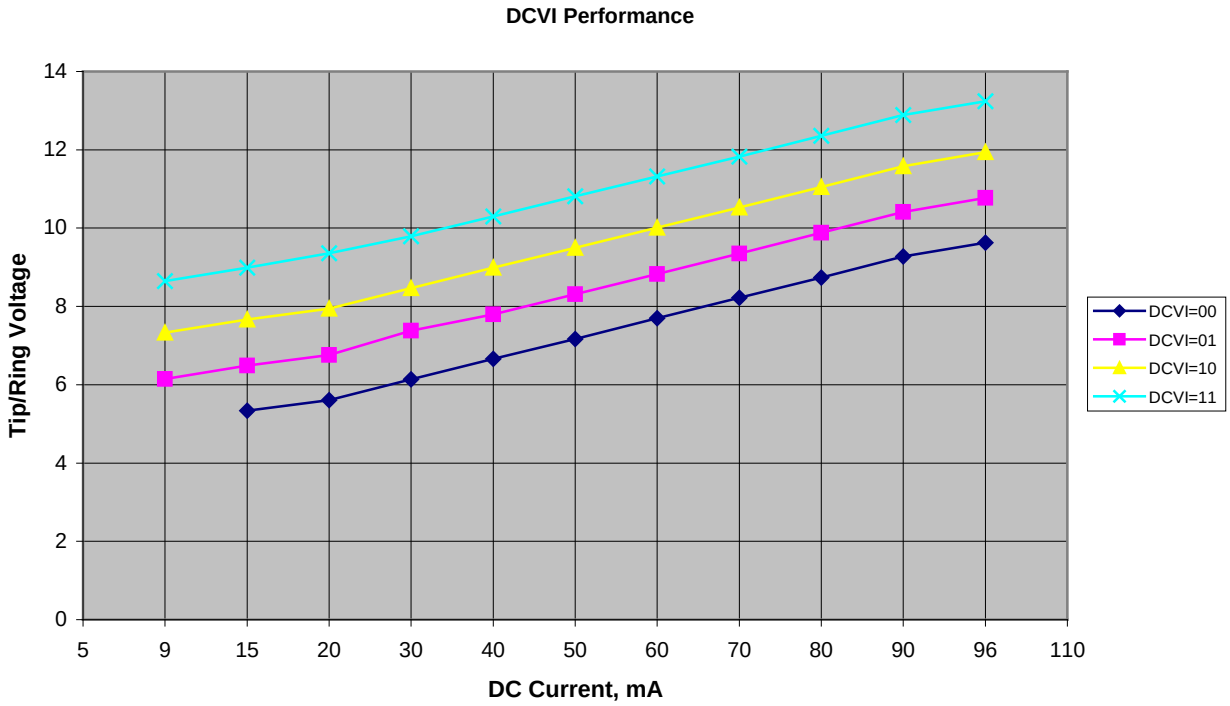

Figure 2: DC Line Characteristics with the 73M1x22 DCVI(1:0) Settings

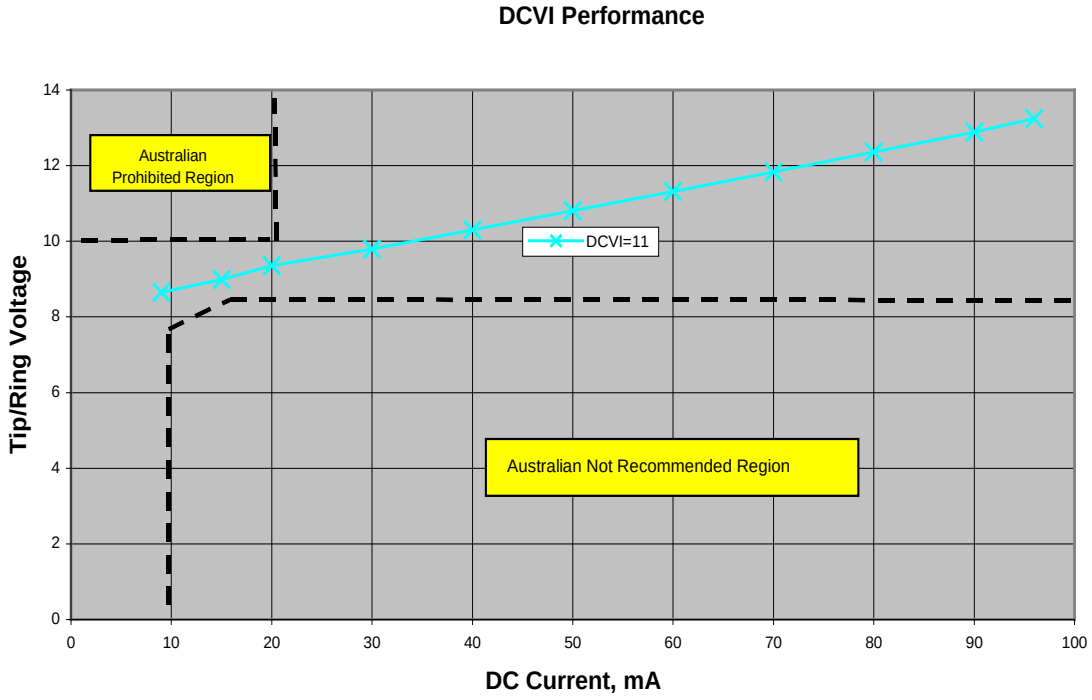

Figure 3: DCVI(1:0) = 11 Setting with the Australian Hold State Template

Figure 4 shows the Seize Mode DCVI characteristics with the Australian Seize Template.

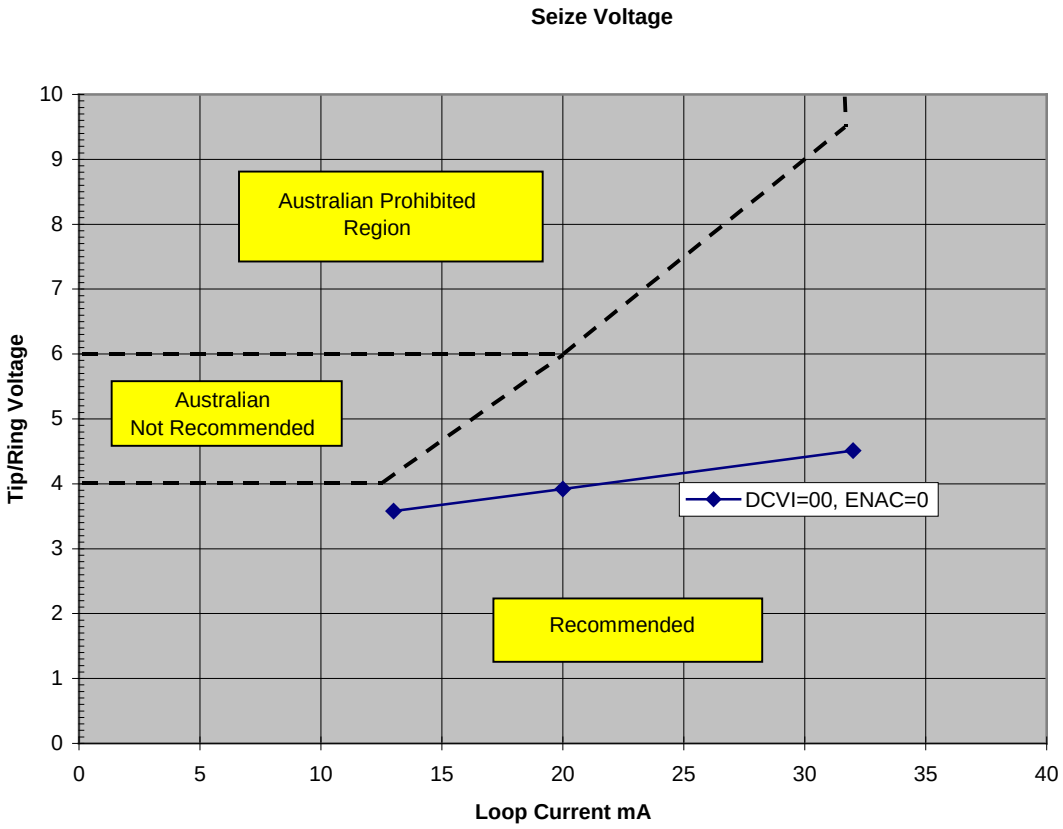

Figure 4: Seize Mode DCVI Characteristics with the Australian Seize Template

Ring Detector Threshold

Set by selecting the RGTH bits in Register 0x0E[1:0]. Table 4 shows the examples of ring threshold settings for specific countries.

Table 4 shows some preliminary max and minimum ring levels and ring threshold settings recommended for the 73M1x22 MicroDAA. Ring detection is only possible if bit ENDC=0 in Register 0x12[6].

Table 4: Worldwide Ring Threshold Settings

Country	Min(V_{RMS}) To Detect	Max(V_{RMS}) Not to Detect	RGTH(1:0) Setting (Volt)	Ring Min Threshold to Detect	Ring Max Threshold Not to Detect
Austria	25	10	01 (15 V)	14	0B
Belgium	25	10	01 (15 V)	14	0B
Bulgaria	30	9	01 (15 V)	14	0B
Cyprus	30	10	01 (15 V)	14	0B
Czech Republic	25	15		14	0B
Denmark	40	17	10(30 V)		
England	63	0			
Finland	35	10	10 (30 V)		
France	25	15			
Germany	32	0			
Greece	25	15			
Hungary	40	12	10 (30 V)		
Iceland	30	10	01 (15 V)		
Ireland	25	3	01 (15 V)		
Italy	26	15			
Japan					
Korea					
Luxembourg	45	10	01 (15 V)		
Norway	28	17			
Netherlands	35	10	10 (30 V)		
Poland	40	16	10 (30 V)		
Portugal	30	12	01 (15 V)		
Spain	35	0			
Sweden	30	10	01 (15 V)		
Switzerland	24	8	01 (15 V)		
USA	45	0	01 (15 V)		

Device Initialization Procedure

This section provides an example of the 73M1x22 MicroDAA initialization sequence including the global configuration parameter settings.

1. Reset pulse generation by the host

The 73M1x22 MicroDAA does not have a power on reset circuit. For proper operation, a reset signal shall be asserted from the host by pulling the reset pin of 73M1x22 Host Interface Circuitry (HIC) low approximately for a minimum of 100 ns after the power is stabilized. The 73M1x22 HIC will be ready to use within 100 µs after the removal of reset pulse from the reset pin.

2. 73M1x22 HIC Initialization

   1. Configure either hardware control frame or software control frame by selecting the HC bit in Register 0x01[3].
   2. Configure GPIOs by selecting GPIO Data (Register 0x02), GPIO Direction (Register 0x03), GPIO Interrupt Enable (Register 0x04) and Interrupt Polarity (Register 0x05).

      ✓ GPIO pins are not available on the 20-pin 73M1922.

   3. Timing Chain setup (Register 0x08 – Register 0x0D). It is recommended to write the Register 0x0D value last. Writing to Register 0x08 to Register 0x0C does not affect the PLL until Register 0x0D is written. It is also recommended to set the CHNGFS bit (Register 0x0D[3]) in case further sample rate changes are required (as in V.90 applications).
   4. Enable Analog Front End blocks by setting the ENFE bit (Register 0x0F[7]) and make the device active by clearing the Sleep bit (Register 0x0F[5]).
   5. Select system clock driven from the PLL by setting the FRCVCO bit (Register 0x0E[7]).
   6. Read Register 0x0E and modify the Ring Threshold by modifying the RGTH bits into the appropriate value and write back to Register 0x0E. This read-modify-write procedure is used so as not to affect other bits in the same register.

3. 73M1x22 LIC Power Up

The 73M1x22 Line Interface Circuitry (LIC) initialization begins after the 73M1x22 LIC part is fully powered up and initialized. Following the HIC Initialization and the setting of the ENFE bit, setting the FRVCO bits will start powering the 73M1x22 LIC. From this moment, the host shall wait for 100 to 200 ms for the 73M1x22 LIC to be ready.

4. 73M1x22 LIC Initialization

   1. Enable the Front End functional blocks by setting the ENFEL bit (Register 0x12[2]).
   2. Select the desired DCIV and ILM settings, and set the THDCEN bit (Register 0x13[4]). The DCVI characteristics should be chosen based on the country requirements shown in Table 2. ILM is not required for most applications. THDCEN enables the AC cancellation for the DC holding circuit.
   3. Select the proper AC impedance termination by setting the ACZ bits (Register 0x17[4:3]) based on the country requirements shown in Table 1. Set the ATEN bit (Register 0x16[4]) to activate AC termination.
   4. Enable the transmit and receive paths by setting the TXEN and RXEN bits (Register 0x16[7:6]). For most applications, the RXG bits (Register 0x14[1:0]) should be set to 10.
   5. To go off hook, set the OFH and ENDC bits in Register 0x12[7:6]. Optionally the ENAC bit (Register 0x12[5]) can be set at the same time, or it can be set separately to use the “seize” mode as required for Australia (Figure 3). This puts the network connection into a mode where the DC voltage is lower than what is set by the DCVI bits and is used for the first ~300 ms before the ENAC bit is set. After the ENAC bit is set, the line goes to the “hold” state and reverts to the normal DCVI mode selected by the DCVI bits (Figures 1 and 2). After entering the hold state, ENNOM bit (Register 0x12[0]) should be set to allow the operation of the line detectors (UVDT, OVDT, and OIDT) and shift the DC circuit to circuit to the low bandwidth state, At this point, the line voltage and current detectors can be enabled by setting the ENDT bit (Register 0x12[1]).

The 73M1x22 is ready for normal operation.

Revision History

Revision	Description
1.0	First publication.