CY7C421

# 512 × 9 Asynchronous FIFO

## Features

- Asynchronous First-In First-Out (FIFO) Buffer Memories
  - 512 × 9 (CY7C421)
- Dual-Ported RAM Cell
- High Speed 50 MHz Read and Write Independent of Depth and Width
- Low Operating Power: $I_{CC}$ = 35 mA
- Empty and Full Flags (Half Full Flag in Standalone)
- TTL Compatible
- Retransmit in Standalone
- Expandable in Width
- PLCC, 7 × 7 TQFP, 300-Mil Molded SOJ
- Pb-free Packages Available
- Pin Compatible and Functionally Equivalent to IDT7201, and AM7201

## Functional Description

The CY7C421 is a first-in first-out (FIFO) memory offered in 300-mil wide SOJ, TQFP & PLCC packages and it is 512 words by 9 bits wide. Each FIFO memory is organized such that the data is read in the same sequential order that it was written. Full and empty flags are provided to prevent overflow and underflow. Three additional pins are also provided to facilitate unlimited expansion in width, depth, or both. The depth expansion technique steers the control signals from one device to another in parallel. This eliminates the serial addition of propagation delays, so that throughput is not reduced. Data is steered in a similar manner.

The read and write operations may be asynchronous; each can occur at a rate of 50 MHz. The write operation occurs when the write ($\overline{W}$) signal is LOW. Read occurs when read ($\overline{R}$) goes LOW. The nine data outputs go to the high impedance state when $\overline{R}$ is HIGH.

A Half Full ($\overline{HF}$) output flag that is valid in the standalone and width expansion configurations is provided. In the depth expansion configuration, this pin provides the expansion out ($\overline{XO}$) information that is used to tell the next FIFO that it is activated.

In the standalone and width expansion configurations, a LOW on the retransmit ($\overline{RT}$) input causes the FIFO to retransmit the data. Read enable ($\overline{R}$) and write enable ($\overline{W}$) must both be HIGH during retransmit, and then $\overline{R}$ is used to access the data.

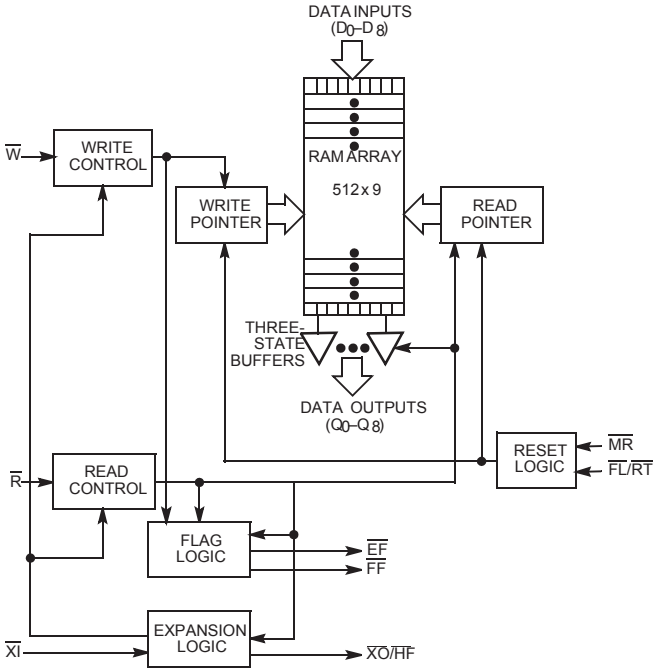
The CY7C421 is fabricated using an advanced 0.65-micron P-well CMOS technology. Input ESD protection is greater than 2000 V and latch up is prevented by careful layout and guard rings.

For a complete list of related documentation, click here.

## Selection Guide

| 512 × 9 | -15 | -20 |
|---|---|---|
| **Frequency (MHz)** | 40 | 33.3 |
| **Maximum Access Time (ns)** | 15 | 20 |
| **$I_{CC1}$ (mA)** | 35 | 35 |

## Logic Block Diagram



## Contents

## Pin Configurations

**Figure 1. 32-pin PLCC/LCC (Top View)**

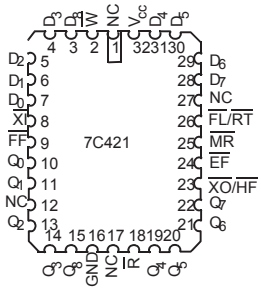



**Figure 2. 28-pin DIP (Top View)**

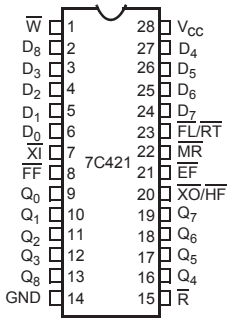
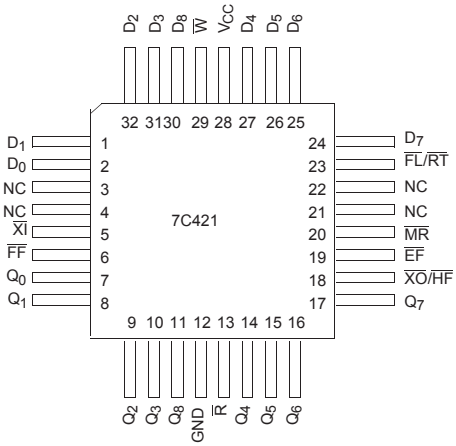



**Figure 3. 32-pIn TQFP (Top View)**



## Pin Definitions

| Signal Name | Description | I/O | Function |
|---|---|---|---|
| $\overline{W}$ | Write Signal | I | Write into the FIFO |
| $\overline{R}$ | Read Signal | I | Read from the FIFO |
| $D_0$–$D_8$ | Input Data | I | Data into the FIFO |
| $Q_0$–$Q_8$ | Output Data | O | Data Out from the FIFO |
| $\overline{XI}$ | Expansion In | I | Cascaded: Connected to $\overline{XO}$ of pervious device<br>Non-Cascaded: Connected to $V_{CC}$ |
| $\overline{XO}$ | Expansion Out | O | Cascaded: Connected to $\overline{XI}$ of next device<br>Non-Cascaded: Connected to $V_{CC}$ |
| $\overline{HF}$ | Half Full Flag | O | Half-full flag: When $\overline{HF}$ is LOW, half of the FIFO is full. |
| $\overline{FF}$ | Full Flag | O | When $\overline{FF}$ is LOW, the FIFO is full. |
| $\overline{EF}$ | Empty Flag | O | When $\overline{EF}$ is LOW, the FIFO is empty. |
| $\overline{MR}$ | Master Reset | I | FIFO Reset |
| $\overline{RT}$ | Retransmit | I | Causes FIFO to retransmit the data |
| $\overline{FL}$ | First Load | I | Width expansion: Connected to $V_{CC}$<br>Depth expansion: when Gnd indicates that part is first to be loaded all others connected to $V_{CC}$ |
| $V_{CC}$ | Power | I | Voltage Supply |
| GND | Ground | I | Ground |

## Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.[1]

Storage Temperature ..... –65 °C to +150 °C

Ambient Temperature with Power Applied ..... –55 °C to +125 °C

Supply Voltage to Ground Potential .....–0.5 V to +7.0 V

DC Voltage Applied to Outputs in High Z State .....–0.5 V to +7.0 V

DC Input Voltage .....–0.5 V to +7.0 V

Power Dissipation ..... 1.0 W

Output Current, into Outputs (LOW) ..... 20 mA

Static Discharge Voltage (per MIL–STD–883, Method 3015) ..... > 2000 V

Latch Up Current ..... > 200 mA

## Operating Range

| Range | Ambient Temperature[2] | $V_{CC}$ |
|---|---|---|
| Commercial | 0 °C to +70 °C | 5 V ± 10% |
| Industrial | –40 °C to +85 °C | 5 V ± 10% |

## Electrical Characteristics

Over the Operating Range

| Parameter | Description | Test Conditions | | All Speed Grades | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min | Max | |
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = Min, $I_{OH}$ = –2.0 mA | | 2.4 | – | V |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = Min, $I_{OL}$ = 8.0 mA | | – | 0.4 | V |
| $V_{IH}$ | Input HIGH Voltage | | Commercial | 2.0 | $V_{CC}$ | V |
| | | | Industrial | 2.2 | $V_{CC}$ | |
| $V_{IL}$ | Input LOW Voltage | | | [3] | 0.8 | V |
| $I_{IX}$ | Input Leakage Current | GND ≤ $V_I$ ≤ $V_{CC}$ | | –10 | +10 | µA |
| $I_{OZ}$ | Output Leakage Current | $\overline{R}$ ≥ $V_{IH}$, GND ≤ $V_O$ ≤ $V_{CC}$ | | –10 | +10 | µA |
| $I_{OS}$ | Output Short Circuit Current [4] | $V_{CC}$ = Max, $V_{OUT}$ = GND | | – | –90 | mA |

## Electrical Characteristics

Over the Operating Range

| Parameter | Description | Test Conditions | | -15 | | -20 | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | |
| $I_{CC}$ | Operating Current | $V_{CC}$ = Max, $I_{OUT}$ = 0 mA, f = $f_{MAX}$ | Commercial | – | 65 | – | 55 | mA |
| | | | Industrial | – | 100 | – | 90 | |
| $I_{CC1}$ | Operating Current | $V_{CC}$ = Max, $I_{OUT}$ = 0 mA, f = 20 MHz | Commercial | – | 35 | – | 35 | mA |
| $I_{SB1}$ | Standby Current | All Inputs = $V_{IH}$ Min | Commercial | – | 10 | – | 10 | mA |
| | | | Industrial | – | 15 | – | 15 | |
| $I_{SB2}$ | Power Down Current | All Inputs ≥ $V_{CC}$ – 0.2 V | Commercial | – | 5 | – | 5 | mA |
| | | | Industrial | – | 8 | – | 8 | |

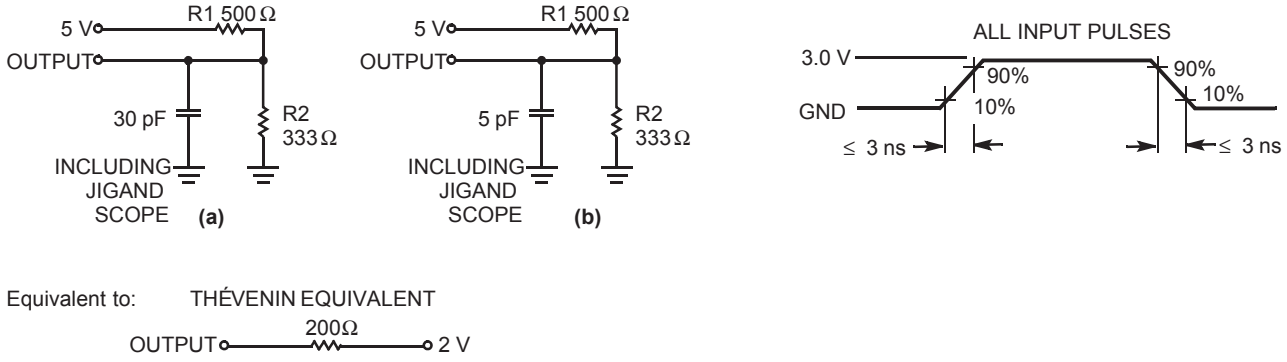
**Notes**
1. Single Power Supply: The voltage on any input or I/O pin cannot exceed the power pin during power up.
2. $T_A$ is the "instant on" case temperature.
3. $V_{IL(Min)}$ = –2.0 V for pulse durations of less than 20 ns.
4. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.

## Capacitance

| Parameter [5] | Description | Test Conditions | Max | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $T_A$ = 25 °C, f = 1 MHz, $V_{CC}$ = 4.5 V | 6 | pF |
| $C_{OUT}$ | Output Capacitance | | 6 | pF |

## AC Test Loads and Waveforms

**Figure 4. AC Test Loads and Waveforms**




Equivalent to: THÉVENIN EQUIVALENT




**Note**
5. Tested initially and after any design or process changes that may affect these parameters.

## Switching Characteristics

Over the Operating Range

| Parameter [6] | Description | -15 | | -20 | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| $t_{RC}$ | Read Cycle Time | 25 | – | 30 | – | ns |
| $t_{A}$ | Access Time | – | 15 | – | 20 | ns |
| $t_{RR}$ | Read Recovery Time | 10 | – | 10 | – | ns |
| $t_{PR}$ | Read Pulse Width | 15 | – | 20 | – | ns |
| $t_{LZR}$[7] | Read LOW to Low Z | 3 | – | 3 | – | ns |
| $t_{DVR}$[7, 8] | Data Valid after Read HIGH | 5 | – | 5 | – | ns |
| $t_{HZR}$[7, 8] | Read HIGH to High Z | – | 15 | – | 15 | ns |
| $t_{WC}$ | Write Cycle Time | 25 | – | 30 | – | ns |
| $t_{PW}$ | Write Pulse Width | 15 | – | 20 | – | ns |
| $t_{HWZ}$[7] | Write HIGH to Low Z | 5 | – | 5 | – | ns |
| $t_{WR}$ | Write Recovery Time | 10 | – | 10 | – | ns |
| $t_{SD}$ | Data Setup Time | 8 | – | 12 | – | ns |
| $t_{HD}$ | Data Hold Time | 0 | – | 0 | – | ns |
| $t_{MRSC}$ | $\overline{MR}$ Cycle Time | 25 | – | 30 | – | ns |
| $t_{PMR}$ | $\overline{MR}$ Pulse Width | 15 | – | 20 | – | ns |
| $t_{RMR}$ | $\overline{MR}$ Recovery Time | 10 | – | 10 | – | ns |
| $t_{RPW}$ | Read HIGH to $\overline{MR}$ HIGH | 15 | – | 20 | – | ns |
| $t_{WPW}$ | Write HIGH to $\overline{MR}$ HIGH | 15 | – | 20 | – | ns |
| $t_{RTC}$ | Retransmit Cycle Time | 25 | – | 30 | – | ns |
| $t_{PRT}$ | Retransmit Pulse Width | 15 | – | 20 | – | ns |
| $t_{RTR}$ | Retransmit Recovery Time | 10 | – | 10 | – | ns |
| $t_{EFL}$ | $\overline{MR}$ to $\overline{EF}$ LOW | – | 25 | – | 30 | ns |
| $t_{HFH}$ | $\overline{MR}$ to $\overline{HF}$ HIGH | – | 25 | – | 30 | ns |
| $t_{FFH}$ | $\overline{MR}$ to $\overline{FF}$ HIGH | – | 25 | – | 30 | ns |
| $t_{REF}$ | Read LOW to $\overline{EF}$ LOW | – | 15 | – | 20 | ns |
| $t_{RFF}$ | Read HIGH to $\overline{FF}$ HIGH | – | 15 | – | 20 | ns |
| $t_{WEF}$ | Write HIGH to $\overline{EF}$ HIGH | – | 15 | – | 20 | ns |
| $t_{WFF}$ | Write LOW to $\overline{FF}$ LOW | – | 15 | – | 20 | ns |
| $t_{WHF}$ | Write LOW to $\overline{HF}$ LOW | – | 15 | – | 20 | ns |
| $t_{RHF}$ | Read HIGH to $\overline{HF}$ HIGH | – | 15 | – | 20 | ns |
| $t_{RAE}$ | Effective Read from Write HIGH | – | 15 | – | 20 | ns |
| $t_{RPE}$ | Effective Read Pulse Width after $\overline{EF}$ HIGH | 15 | – | 20 | – | ns |
| $t_{WAF}$ | Effective Write from Read HIGH | – | 15 | – | 20 | ns |
| $t_{WPF}$ | Effective Write Pulse Width after $\overline{FF}$ HIGH | 15 | – | 20 | – | ns |
| $t_{XOL}$ | Expansion Out LOW Delay from Clock | – | 15 | – | 20 | ns |
| $t_{XOH}$ | Expansion Out HIGH Delay from Clock | – | 15 | – | 20 | ns |

**Notes**

6. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V and output loading of the specified $I_{OL}/I_{OH}$ and 30 pF load capacitance, as in part (a) of Figure 4 on page 7, unless otherwise specified.
7. $t_{HZR}$ transition is measured at +200 mV from $V_{OL}$ and –200 mV from $V_{OH}$. $t_{DVR}$ transition is measured at the 1.5V level. $t_{HWZ}$ and $t_{LZR}$ transition is measured at ±100 mV from the steady state.
8. $t_{HZR}$ and $t_{DVR}$ use capacitance loading as in part (b) of Figure 4 on page 7.

## Switching Waveforms

**Figure 5. Asynchronous Read and Write**

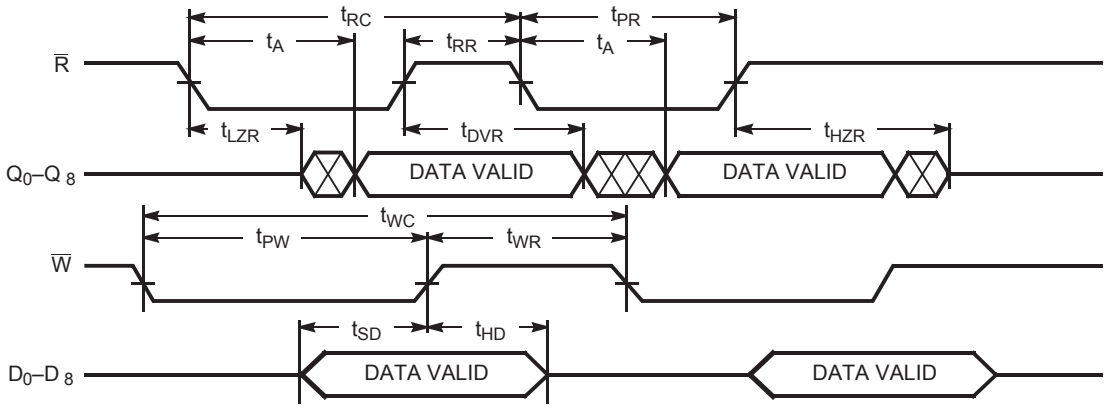



**Figure 6. Master Reset**

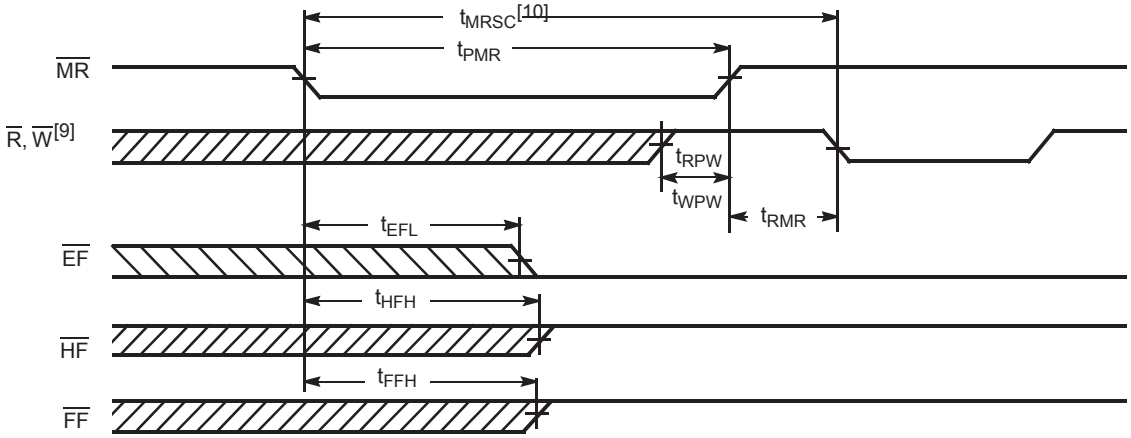
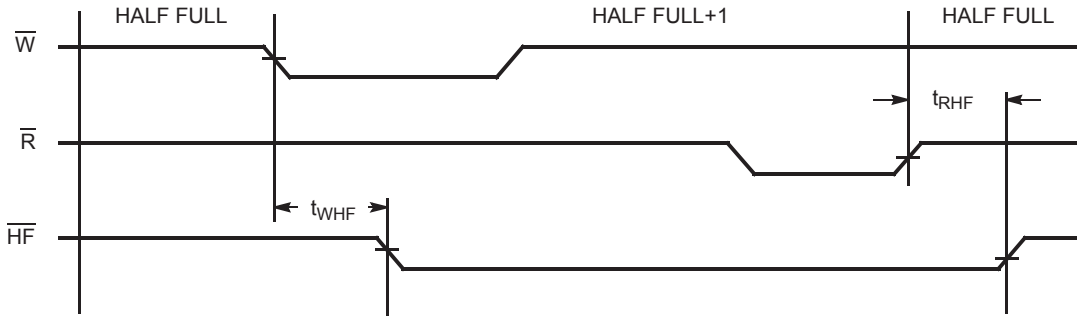



**Figure 7. Half-full Flag**




**Notes**
9. $\overline{W}$ and $\overline{R} \geq V_{IH}$ around the rising edge of $\overline{MR}$.
10. $t_{MRSC} = t_{PMR} + t_{RMR}$.

## Switching Waveforms (continued)

**Figure 8. Last Write to First Read Full Flag**

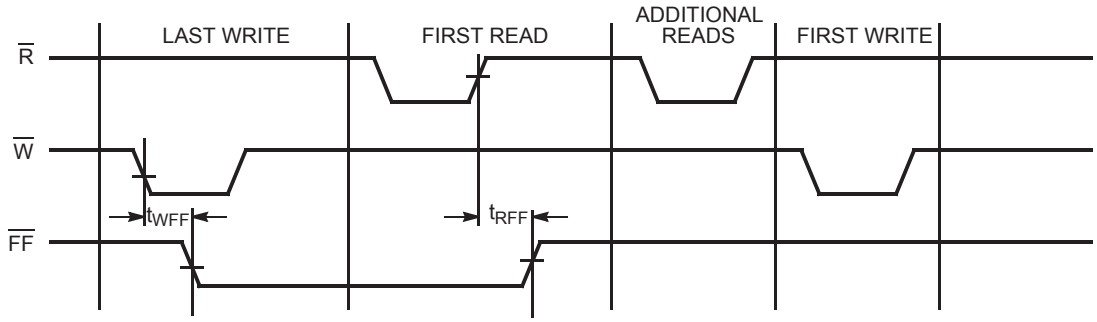



**Figure 9. Last Read to First Write Empty Flag**

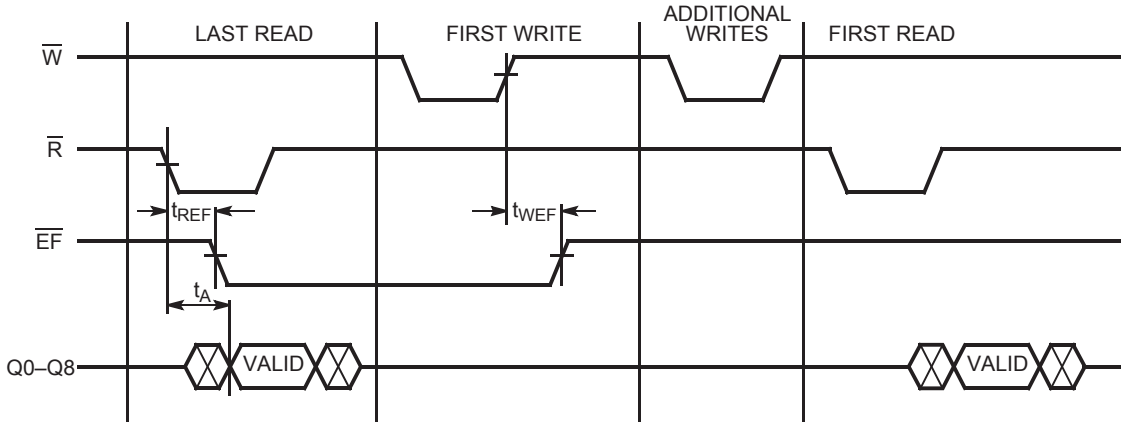
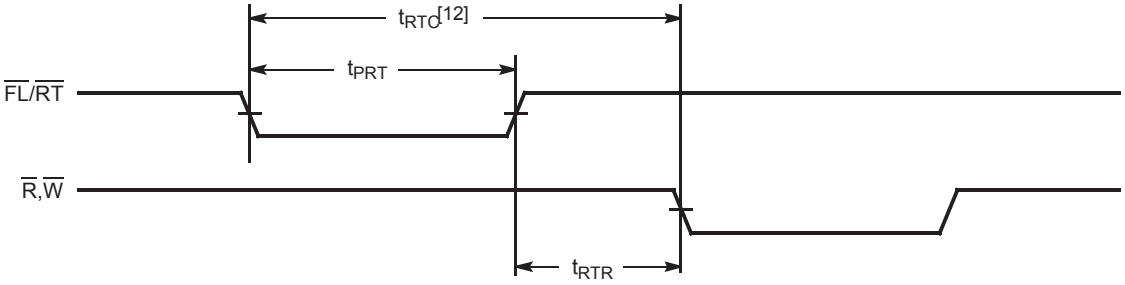



**Figure 10. Retransmit [11]**




**Notes**
11. $\overline{EF}$, $\overline{HF}$ and $\overline{FF}$ may change state during retransmit as a result of the offset of the read and write pointers, but flags are valid at $t_{RTC}$.
12. $t_{RTC} = t_{PRT} + t_{RTR}$.

## Switching Waveforms (continued)

**Figure 11. Empty Flag and Read Data Flow-through Mode**

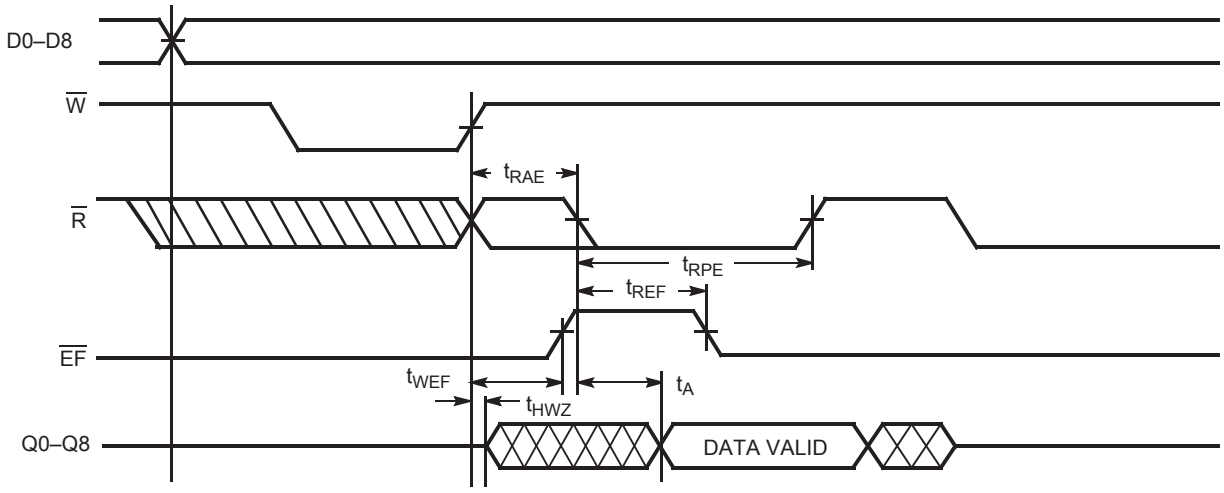
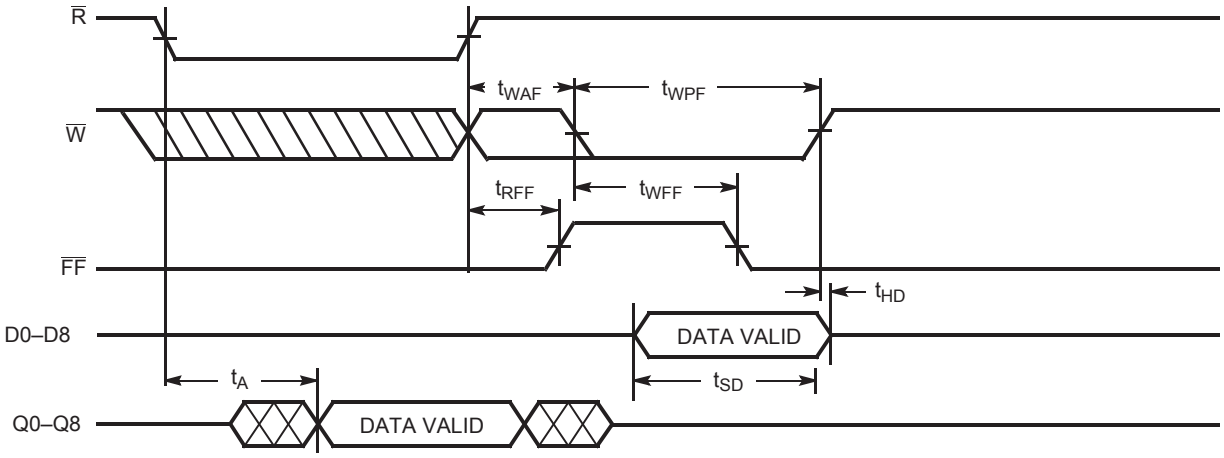
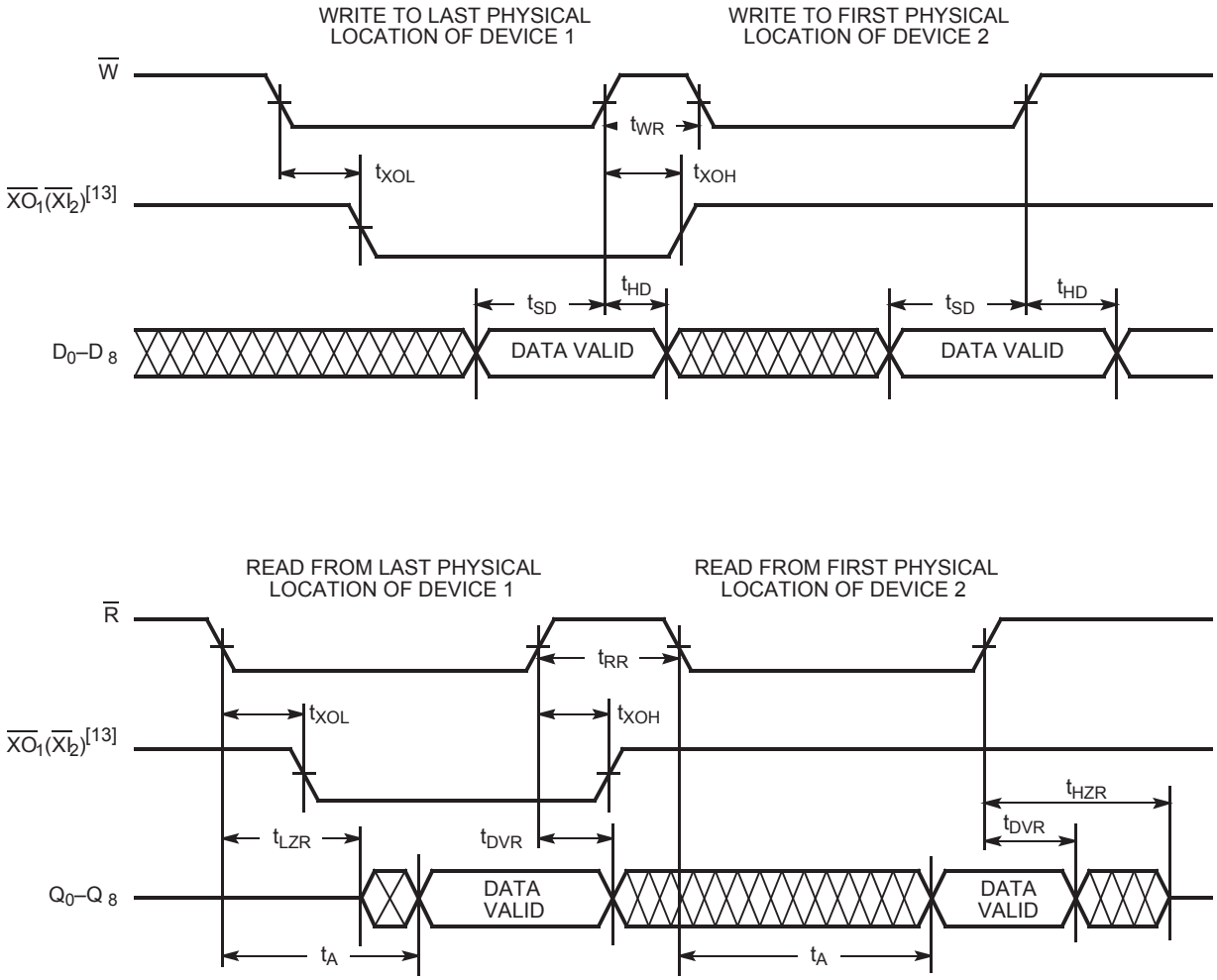



**Figure 12. Full Flag and Write Data Flow-through Mode**



## Switching Waveforms (continued)

**Figure 13. Expansion Timing Diagrams**




**Note**
13. Expansion Out of device 1 ($\overline{XO}_1$) is connected to Expansion In of device 2 ($\overline{XI}_2$).

## Architecture

The CY7C421 FIFO consist of an array of 512 words of 9 bits each (implemented by an array of dual-port RAM cells), a read pointer, a write pointer, control signals (W, R, XI, XO, FL, RT, MR), and Full, Half Full, and Empty flags.

### Dual-Port RAM

The dual-port RAM architecture refers to the basic memory cell used in the RAM. The cell itself enables the read and write operations to be independent of each other, which is necessary to achieve truly asynchronous operation of the inputs and outputs. A second benefit is that the time required to increment the read and write pointers is much less than the time required for data propagation through the memory, which is the case if memory is implemented using the conventional register array architecture.

### Resetting the FIFO

Upon power up, the FIFO must be reset with a Master Reset ($\overline{MR}$) cycle. This causes the FIFO to enter the empty condition signified by the Empty flag ($\overline{EF}$) being LOW, and both the Half Full ($\overline{HF}$) and Full flags ($\overline{FF}$) being HIGH. Read ($\overline{R}$) and write ($\overline{W}$) must be HIGH $t_{RPW}/t_{WPW}$ before and $t_{RMR}$ after the rising edge of $\overline{MR}$ for a valid reset cycle. If reading from the FIFO after a reset cycle is attempted, the outputs are in the high impedance state.

### Writing Data to the FIFO

The availability of at least one empty location is indicated by a HIGH $\overline{FF}$. The falling edge of $\overline{W}$ initiates a write cycle. Data appearing at the inputs ($D_0$–$D_8$) $t_{SD}$ before and $t_{HD}$ after the rising edge of $\overline{W}$ are stored sequentially in the FIFO.

The $\overline{EF}$ LOW-to-HIGH transition occurs $t_{WEF}$ after the first LOW-to-HIGH transition of $\overline{W}$ for an empty FIFO. $\overline{HF}$ goes LOW $t_{WHF}$ after the falling edge of $\overline{W}$ following the FIFO actually being Half Full. Therefore, the $\overline{HF}$ is active after the FIFO is filled to half its capacity plus one word. $\overline{HF}$ remains LOW while less than one half of total memory is available for writing. The LOW-to-HIGH transition of $\overline{HF}$ occurs $t_{RHF}$ after the rising edge of $\overline{R}$ when the FIFO goes from half full +1 to half full. $\overline{HF}$ is available in standalone and width expansion modes. $\overline{FF}$ goes LOW $t_{WFF}$ after the falling edge of $\overline{W}$, during the cycle in which the last available location is filled. Internal logic prevents FIFO overflow. Writes to a full FIFO are ignored and the write pointer is not incremented. $\overline{FF}$ goes HIGH $t_{RFF}$ after a read from a full FIFO.

### Reading Data from the FIFO

The falling edge of $\overline{R}$ initiates a read cycle provided $\overline{EF}$ is not LOW. Data outputs ($Q_0$–$Q_8$) are in a high impedance condition between read operations ($\overline{R}$ HIGH), when the FIFO is empty, or when the FIFO is not the active device in the depth expansion mode.

When one word is in the FIFO, the falling edge of $\overline{R}$ initiates a HIGH-to-LOW transition of $\overline{EF}$. The rising edge of $\overline{R}$ causes the data outputs to go to the high impedance state and remain such until a write is performed. Reads to an empty FIFO are ignored and do not increment the read pointer. From the empty condition, the FIFO can be read $t_{WEF}$ after a valid write.

The retransmit feature is beneficial when transferring packets of data. It enables the receiver to acknowledge receipt of data and retransmit, if necessary.

The Retransmit ($\overline{RT}$) input is active in the standalone and width expansion modes. The retransmit feature is intended for use when a number of writes equal to or less than the depth of the FIFO have occurred since the last $\overline{MR}$ cycle. A LOW pulse on $\overline{RT}$ resets the internal read pointer to the first physical location of the FIFO. $\overline{R}$ and $\overline{W}$ must both be HIGH for $t_{PRT}$ and $t_{RTR}$ after retransmit is asserted. With every read cycle after retransmit, the data from the first physical location of FIFO is read until the read pointer equals write pointer. Full, Half Full, and Empty flags are governed by the relative locations of the read and write pointers and are updated during a retransmit cycle. Data written to the FIFO after activation of $\overline{RT}$ are also transmitted. Full depth of FIFO data can be repeatedly retransmitted.

### Standalone/Width Expansion Modes

Standalone and width expansion modes are set by grounding Expansion In ($\overline{XI}$) and tying First Load ($\overline{FL}$) to $V_{CC}$. FIFOs can be expanded in width to provide word widths greater than nine in increments of nine. During width expansion mode, all control line inputs are common to all devices, and flag outputs from any device can be monitored.

### Depth Expansion Mode

Depth expansion mode (see Figure 14 on page 14) is entered when, during a $\overline{MR}$ cycle, Expansion Out ($\overline{XO}$) of one device is connected to Expansion In ($\overline{XI}$) of the next device, with $\overline{XO}$ of the last device connected to $\overline{XI}$ of the first device. In the depth expansion mode the First Load ($\overline{FL}$) input, when grounded, indicates that this part is the first to be loaded. All other devices must have this pin HIGH. To enable the correct FIFO, $\overline{XO}$ is pulsed LOW when the last physical location of the previous FIFO is written to and pulsed LOW again when the last physical location is read. Only one FIFO is enabled for read and one for write at any particular time. All other devices are in standby.

FIFOs can also be expanded simultaneously in depth and width. Consequently, any depth or width FIFO can be created of word widths in increments of 9. When expanding in depth, a composite $\overline{FF}$ must be created by ORing the $\overline{FF}$s together. Likewise, a composite $\overline{EF}$ is created by ORing the $\overline{EF}$s together. $\overline{HF}$ and $\overline{RT}$ functions are not available in depth expansion mode.

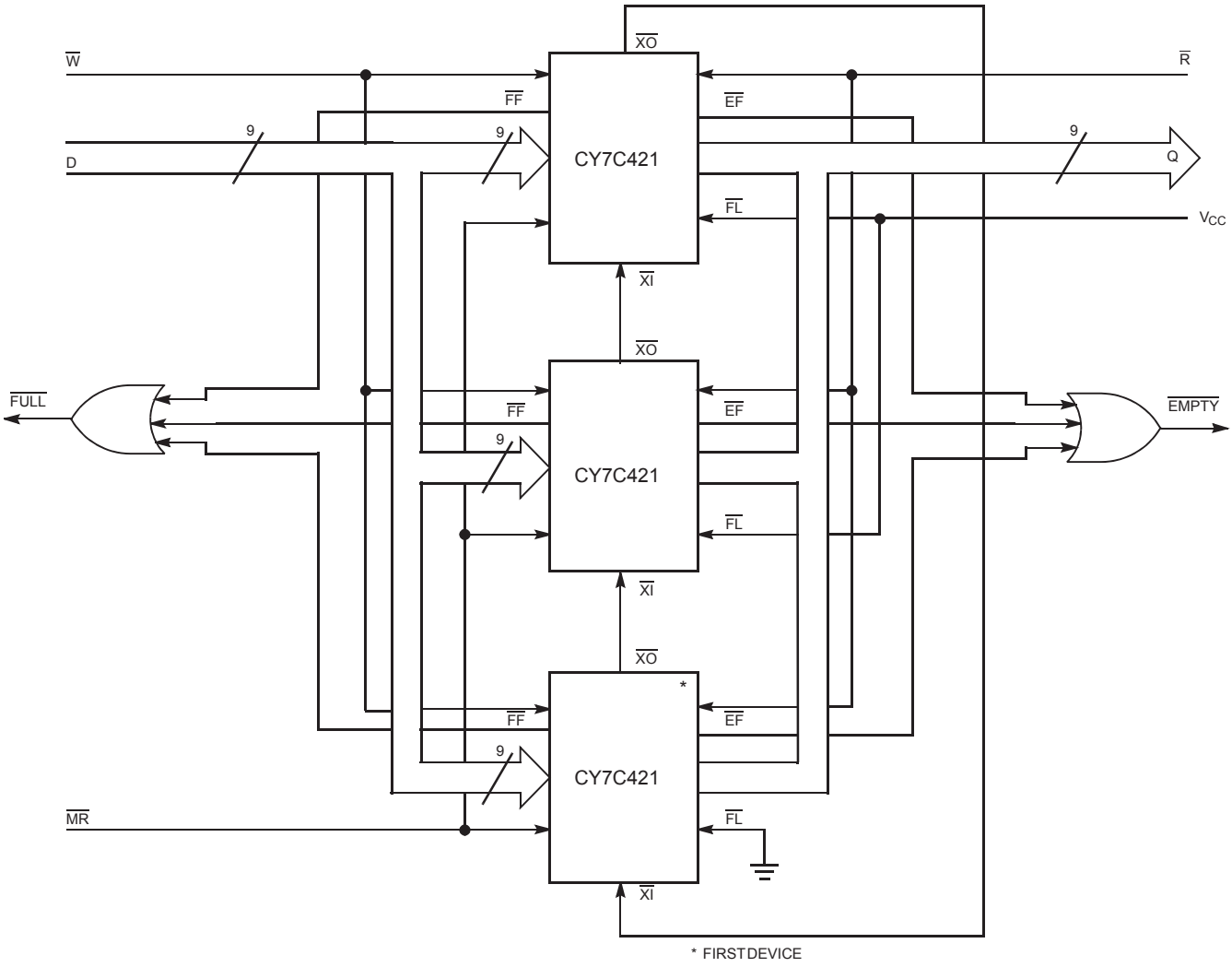
## Use of the Empty and Full Flags

To achieve maximum frequency, the flags must be valid at the beginning of the next cycle. However, because they can be updated by either edge of the read or write signal, they must be valid by one-half of a cycle. Cypress FIFOs meet this requirement.

The reason for why the flags should be valid by the next cycle is complex. The “effective pulse width violation” phenomenon can occur at the full and empty boundary conditions, if the flags are not properly used. The empty flag must be used to prevent reading from an empty FIFO and the full flag must be used to prevent writing into a full FIFO.

For example, consider an empty FIFO that is receiving read pulses. Because the FIFO is empty, the read pulses are ignored by the FIFO, and nothing happens. Next, a single word is written into the FIFO, with a signal that is asynchronous to the read signal. The (internal) state machine in the FIFO goes from empty to empty+1. However, it does this asynchronously with respect to the read signal, so that the effective pulse width of the read signal cannot be determined, because the state machine does not look at the read signal until it goes to the empty+1 state. Similarly, the minimum write pulse width may be violated by trying to write into a full FIFO, and asynchronously performing a read. The empty and full flags are used to avoid these effective pulse width violations, but to do this and operate at the maximum frequency, the flag must be valid at the beginning of the next cycle.

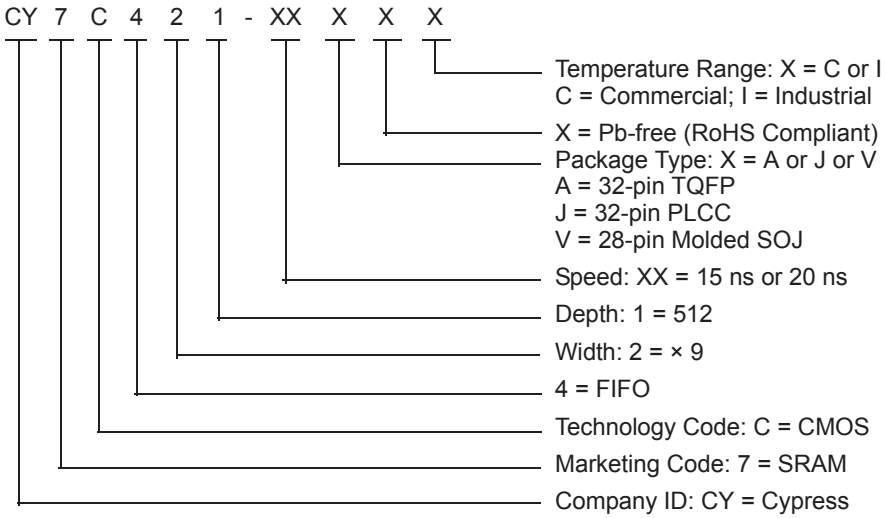
**Figure 14. Depth Expansion**



## Ordering Information

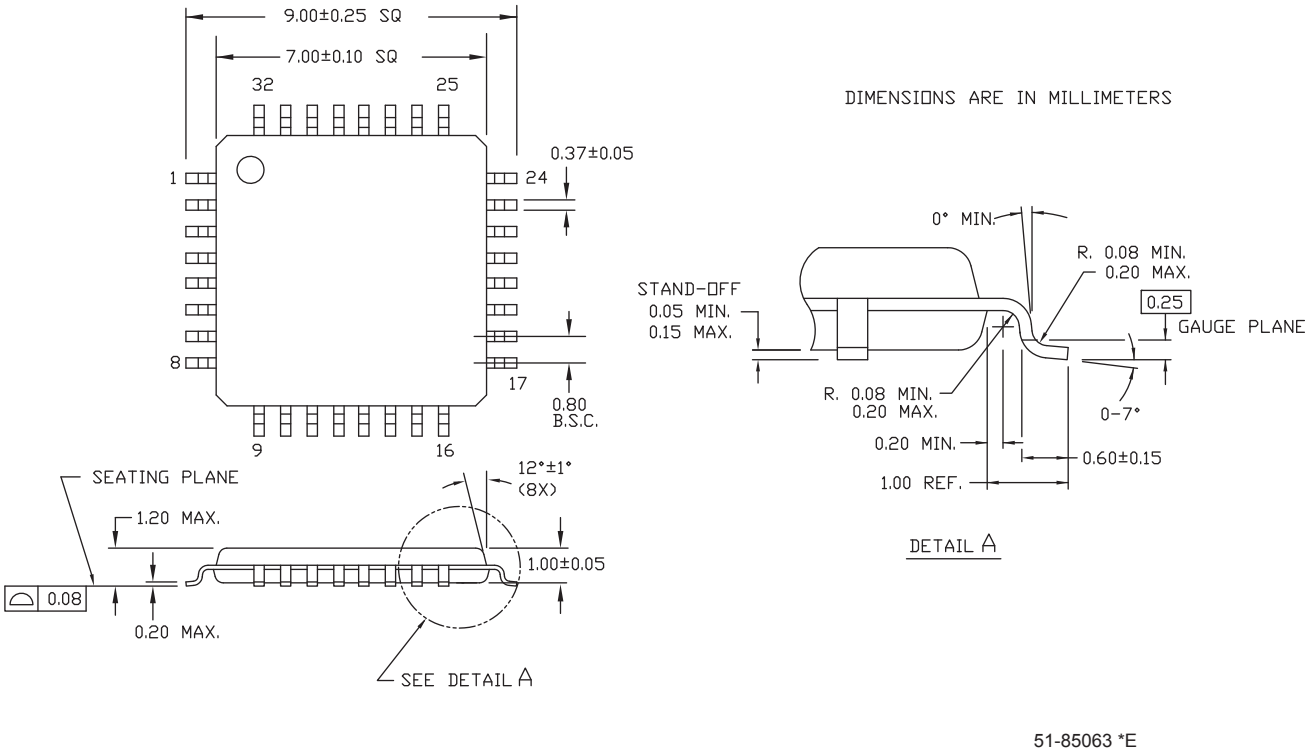
| Speed (ns) | Ordering Code | Package Diagram | Package Type | Operating Range |
|---|---|---|---|---|
| 15 | CY7C421-15AXC | 51-85063 | 32-pin TQFP (Pb-free) | Commercial |
| 20 | CY7C421-20JXC | 51-85002 | 32-pin PLCC (Pb-free) | Commercial |
| | CY7C421-20VXC | 51-85031 | 28-pin (300 Mils) Molded SOJ (Pb-free) | |

### Ordering Code Definitions



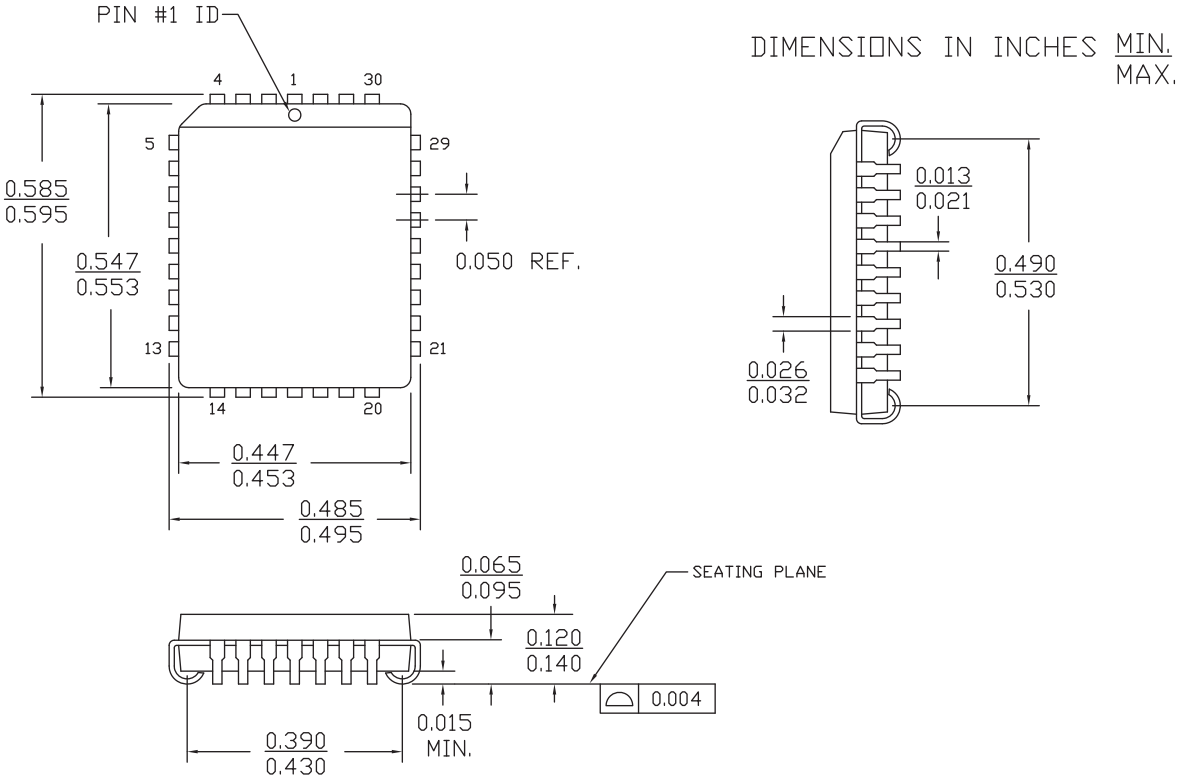
## Package Diagrams

**Figure 15. 32-pin TQFP (7 × 7 × 1.0 mm) A3210 Package Outline, 51-85063**



## Package Diagrams (continued)

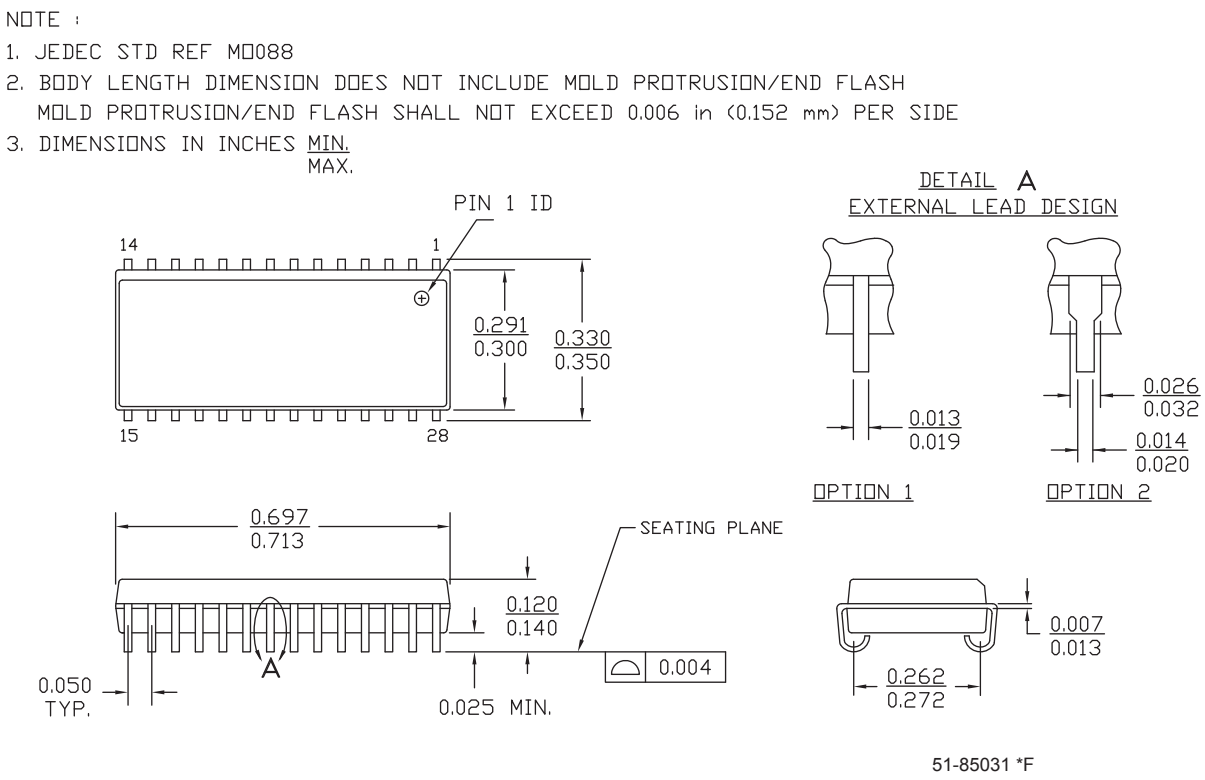
**Figure 16. 32-pin PLCC (0.453 × 0.553 Inches) J32 Package Outline, 51-85002**




51-85002 *E

## Package Diagrams (continued)

**Figure 17. 28-pin SOJ (300 Mils) V28.3 (Molded SOJ V21) Package Outline, 51-85031**



## Acronyms

| Acronym | Description |
|---|---|
| DIP | Dual In-line Package |
| FIFO | First-In First-Out |
| I/O | Input/Output |
| LCC | Leadless Chip Carrier |
| PLCC | Plastic Leaded Chip Carrier |
| RAM | Random Access Memory |
| SOJ | Small Outline J-lead |
| TQFP | Thin Quad Flat Pack |
| TTL | Transistor-Transistor Logic |

## Document Conventions

### Units of Measure

| Symbol | Unit of Measure |
|---|---|
| °C | degree Celsius |
| MHz | megahertz |
| µA | microampere |
| mA | milliampere |
| mm | millimeter |
| mV | millivolt |
| ns | nanosecond |
| % | percent |
| pF | picofarad |
| V | volt |
| W | watt |

## Document History Page

| Document Title: CY7C421, 512 × 9 Asynchronous FIFO<br>Document Number: 38-06001 | | | | |
|---|---|---|---|---|
| **Rev.** | **ECN No.** | **Orig. of Change** | **Submission Date** | **Description of Change** |
| ** | 106462 | SZV | 07/11/01 | Change from Spec Number: 38-00079 to 38-06001 |
| *A | 122332 | RBI | 12/30/02 | Updated Maximum Ratings:<br>Added Note 1 and referred the same note in “maximum ratings”. |
| *B | 383597 | PCX | See ECN | Added Pb-Free Logo.<br>Updated Ordering Information (Added the following MPNs: CY7C419-10JXC, CY7C419-15JXC, CY7C419-15VXC, CY7C421-10JXC, CY7C421-15AXC, CY7C421-20JXC, CY7C421-20VXC, CY7C425-10AXC, CY7C425-10JXC, CY7C425-15JXC, CY7C425-20JXC, CY7C425-20VXC, CY7C429-10AXC, CY7C429-15JXC, CY7C429-20JXC, CY7C433-10AXC, CY7C433-10JXC, CY7C433-15JXC, CY7C433-20AXC, CY7C433-20JXC). |
| *C | 2623658 | VKN / PYRS | 12/17/08 | Removed 26-pin CerDIP, 32-pin RLCC, 28-pin molded DIP packages related information in all instances across the document.<br>Removed Military Temperature Range related Information in all instances across the document.<br>Updated Ordering Information (Added MPN CY7C421-20JXI, removed MPNs CY7C419/25/29/33). |
| *D | 2714768 | VKN / AESA | 06/04/2009 | Updated Logic Block Diagram.<br>Updated Pin Configurations.<br>Updated Package Diagrams. |
| *E | 2896039 | RAME | 03/19/2010 | Added Contents.<br>Updated Ordering Information (Removed inactive parts from the data sheet).<br>Updated Package Diagrams.<br>Updated Sales, Solutions, and Legal Information (Updated links). |
| *F | 3110157 | ADMU | 12/14/2010 | Added Ordering Code Definitions under Ordering Information. |
| *G | 3324980 | ADMU | 07/26/2011 | Updated title to read as “CY7C421, 512 × 9 Asynchronous FIFO”.<br>Updated Features.<br>Updated Functional Description (Removed CY7C420/424/425/428/429/432/433 related information).<br>Updated Selection Guide (Removed -10, -25, -30, -40 and -65 speed bins related information).<br>Updated Electrical Characteristics (Removed -10, -25, -30, -40 and -65 speed bins related information).<br>Updated Switching Characteristics (Removed -10, -25, -30, -40 and -65 speed bins related information).<br>Updated Architecture (Removed CY7C420/424/425/428/429/432/433 related information).<br>Updated Package Diagrams.<br>Added Acronyms and Units of Measure.<br>Updated to new template. |
| *H | 3697624 | SMCH | 08/07/2012 | Added Pin Definitions.<br>Updated Architecture (Updated Reading Data from the FIFO (Updated description)). |
| *I | 4082890 | SMCH | 07/31/2013 | Updated Ordering Information (Updated part numbers).<br>Updated to new template.<br>Completing Sunset Review. |
| *J | 4581652 | SMCH | 11/26/2014 | Updated Functional Description:<br>Added “For a complete list of related documentation, click here.” at the end. |

## Document History Page (continued)

| Document Title: CY7C421, 512 × 9 Asynchronous FIFO<br>Document Number: 38-06001 | | | | |
|---|---|---|---|---|
| **Rev.** | **ECN No.** | **Orig. of Change** | **Submission Date** | **Description of Change** |
| *K | 5436569 | NILE | 09/14/2016 | Updated Package Diagrams:<br>spec 51-85063 – Changed revision from *D to *E.<br>spec 51-85002 – Changed revision from *D to *E.<br>spec 51-85031 – Changed revision from *E to *F.<br>Updated to new template.<br>Completing Sunset Review. |

## Sales, Solutions, and Legal Information

### Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

### Products

| | |
|---|---|
| ARM® Cortex® Microcontrollers | cypress.com/arm |
| Automotive | cypress.com/automotive |
| Clocks & Buffers | cypress.com/clocks |
| Interface | cypress.com/interface |
| Internet of Things | cypress.com/iot |
| Lighting & Power Control | cypress.com/powerpsoc |
| Memory | cypress.com/memory |
| PSoC | cypress.com/psoc |
| Touch Sensing | cypress.com/touch |
| USB Controllers | cypress.com/usb |
| Wireless/RF | cypress.com/wireless |

### PSoC®Solutions

PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP

### Cypress Developer Community

Forums | Projects | Video | Blogs | Training | Components

### Technical Support

cypress.com/support