

## DUAL-BIT DUAL-SUPPLY BUS TRANSCEIVER WITH CONFIGURABLE VOLTAGE TRANSLATION AND 3-STATE OUTPUTS

Check for Samples: [SN74LVC2T45-EP](#)

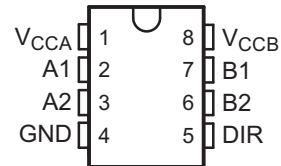
### FEATURES

- Available in the Texas Instruments NanoFree™ Package
- Fully Configurable Dual-Rail Design Allows Each Port to Operate Over the Full 1.65-V to 5.5-V Power-Supply Range
- $V_{CC}$  Isolation Feature – If Either  $V_{CC}$  Input Is at GND, Both Ports Are in the High-Impedance State
- DIR Input Circuit Referenced to  $V_{CCA}$
- Low Power Consumption, 10- $\mu$ A Max  $I_{CC}$
- $\pm 24$ -mA Output Drive at 3.3 V
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Max Data Rates
  - 420 Mbps (3.3-V to 5-V Translation)
  - 210 Mbps (Translate to 3.3 V)
  - 140 Mbps (Translate to 2.5 V)
  - 75 Mbps (Translate to 1.8 V)
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 4000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

### SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- Controlled Baseline
- One Assembly/Test Site
- One Fabrication Site
- Available Temperature Ranges:
  - $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$
  - $-55^{\circ}\text{C}$  to  $150^{\circ}\text{C}$
- Extended Product Life Cycle
- Extended Product-Change Notification
- Product Traceability

DCT OR DCU PACKAGE  
(TOP VIEW)



### DESCRIPTION/ORDERING INFORMATION

This dual-bit noninverting bus transceiver uses two separate configurable power-supply rails. The A port is designed to track  $V_{CCA}$ .  $V_{CCA}$  accepts any supply voltage from 1.65 V to 5.5 V. The B port is designed to track  $V_{CCB}$ .  $V_{CCB}$  accepts any supply voltage from 1.65 V to 5.5 V. This allows for universal low-voltage bidirectional translation between any of the 1.8-V, 2.5-V, 3.3-V, and 5-V voltage nodes.

Table 1. ORDERING INFORMATION<sup>(1)</sup>

$T_A$	PACKAGE <sup>(2)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
$-55^{\circ}\text{C}$ to $125^{\circ}\text{C}$	SSOP – DCT	Reel of 250	SN74LVC2T45MDCTTEP	NXR
$-55^{\circ}\text{C}$ to $150^{\circ}\text{C}$	SSOP – DCU	Reel of 250	SN74LVC2T45SDCUT	CCVR

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).

(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

## DESCRIPTION/ORDERING INFORMATION (CONTINUED)

The SN74LVC2T45 is designed for asynchronous communication between two data buses. The logic levels of the direction-control (DIR) input activate either the B-port outputs or the A-port outputs. The device transmits data from the A bus to the B bus when the B-port outputs are activated, and from the B bus to the A bus when the A-port outputs are activated. The input circuitry on both A and B ports always is active and must have a logic HIGH or LOW level applied to prevent excess  $I_{CC}$  and  $I_{CCZ}$ .

The SN74LVC2T45 is designed so that the DIR input circuit is supplied by  $V_{CCA}$ .

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The  $V_{CC}$  isolation feature ensures that if either  $V_{CC}$  input is at GND, both ports are in the high-impedance state.

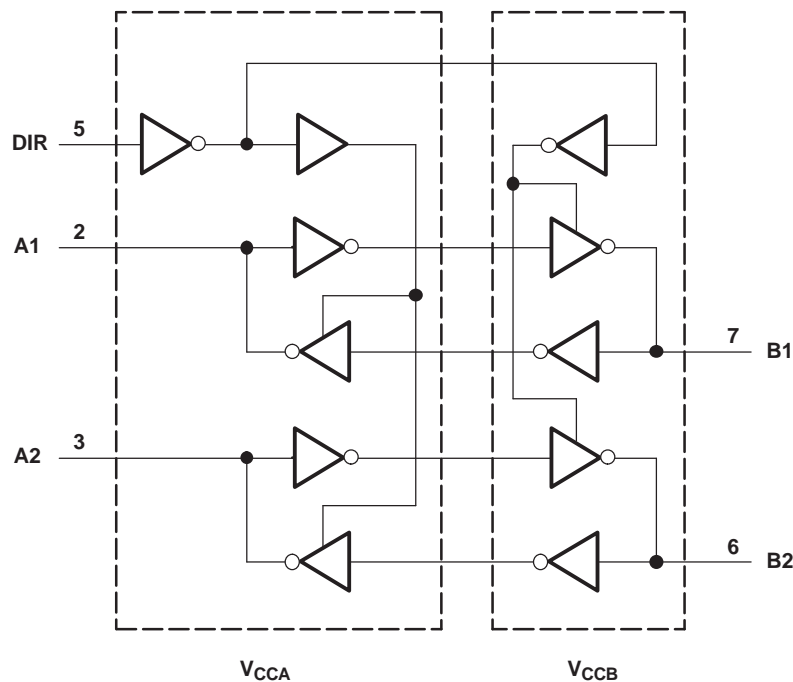
NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

**Table 2. FUNCTION TABLE<sup>(1)</sup>  
(EACH TRANSCEIVER)**

INPUT DIR	OPERATION
L	B data to A bus
H	A data to B bus

(1) Input circuits of the data I/Os always are active.

### LOGIC DIAGRAM (POSITIVE LOGIC)



## Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT	
$V_{CCA}$ $V_{CCB}$	Supply voltage range	-0.5	6.5	V	
$V_I$	Input voltage range <sup>(2)</sup>	-0.5	6.5	V	
$V_O$	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>	-0.5	6.5	V	
$V_O$	Voltage range applied to any output in the high or low state <sup>(2) (3)</sup>	A port	-0.5	$V_{CCA} + 0.5$	V
		B port	-0.5	$V_{CCB} + 0.5$	
$I_{IK}$	Input clamp current		-50	mA	
$I_{OK}$	Output clamp current		-50	mA	
$I_O$	Continuous output current		±50	mA	
	Continuous current through $V_{CC}$ or GND		±100	mA	
$\theta_{JA}$	Package thermal impedance <sup>(4)</sup>	DCT		220	°C/W
		DCU		329.4	
$T_{stg}$	Storage temperature range	-65	150	°C	

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (3) The value of  $V_{CC}$  is provided in the recommended operating conditions table.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

**Recommended Operating Conditions**<sup>(1) (2) (3)</sup>

		$V_{CCI}$	$V_{CCO}$	MIN	MAX	UNIT
$V_{CCA}$	Supply voltage			1.65	5.5	V
$V_{CCB}$				1.65	5.5	
$V_{IH}$	High-level input voltage	Data inputs <sup>(4)</sup>	1.65 V to 1.95 V	$V_{CCI} \times 0.65$	V	
			2.3 V to 2.7 V	1.7		
			3 V to 3.6 V	2		
			4.5 V to 5.5 V	$V_{CCI} \times 0.7$		
$V_{IL}$	Low-level input voltage	Data inputs <sup>(4)</sup>	1.65 V to 1.95 V	$V_{CCI} \times 0.35$	V	
			2.3 V to 2.7 V	0.7		
			3 V to 3.6 V	0.8		
			4.5 V to 5.5 V	$V_{CCI} \times 0.3$		
$V_{IH}$	High-level input voltage	DIR (referenced to $V_{CCA}$ ) <sup>(5)</sup>	1.65 V to 1.95 V	$V_{CCA} \times 0.65$	V	
			2.3 V to 2.7 V	1.7		
			3 V to 3.6 V	2		
			4.5 V to 5.5 V	$V_{CCA} \times 0.7$		
$V_{IL}$	Low-level input voltage	DIR (referenced to $V_{CCA}$ ) <sup>(5)</sup>	1.65 V to 1.95 V	$V_{CCA} \times 0.35$	V	
			2.3 V to 2.7 V	0.7		
			3 V to 3.6 V	0.8		
			4.5 V to 5.5 V	$V_{CCA} \times 0.3$		
$V_I$	Input voltage			0	5.5	V
$V_O$	Output voltage			0	$V_{CCO}$	V
$I_{OH}$	High-level output current		1.65 V to 1.95 V	-4	mA	
			2.3 V to 2.7 V	-8		
			3 V to 3.6 V	-24		
			4.5 V to 5.5 V	-32		
$I_{OL}$	Low-level output current		1.65 V to 1.95 V	4	mA	
			2.3 V to 2.7 V	8		
			3 V to 3.6 V	24		
			4.5 V to 5.5 V	32		
$\Delta t/\Delta v$	Input transition rise or fall rate	Data inputs	1.65 V to 1.95 V	20	ns/V	
			2.3 V to 2.7 V	20		
			3 V to 3.6 V	10		
			4.5 V to 5.5 V	5		
		Control input	1.65 V to 5.5 V	5		
$T_A$	Operating free-air temperature	DCT		-55	125	°C
		DCU		-55	150	

(1)  $V_{CCI}$  is the  $V_{CC}$  associated with the input port.

(2)  $V_{CCO}$  is the  $V_{CC}$  associated with the output port.

(3) All unused data inputs of the device must be held at  $V_{CCI}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

(4) For  $V_{CCI}$  values not specified in the data sheet,  $V_{IH}$  min =  $V_{CCI} \times 0.7$  V,  $V_{IL}$  max =  $V_{CCI} \times 0.3$  V.

(5) For  $V_{CCI}$  values not specified in the data sheet,  $V_{IH}$  min =  $V_{CCA} \times 0.7$  V,  $V_{IL}$  max =  $V_{CCA} \times 0.3$  V.

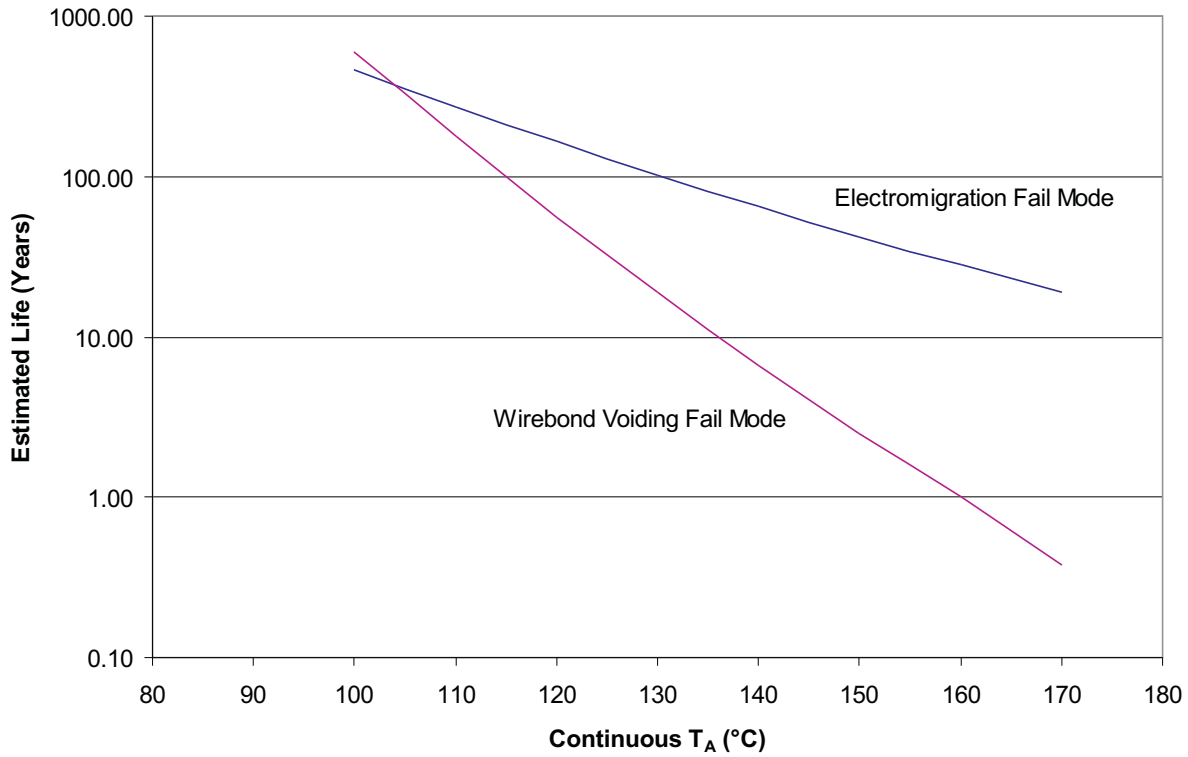
**Electrical Characteristics<sup>(1) (2)</sup>**

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V <sub>CCA</sub>	V <sub>CCB</sub>	T <sub>A</sub> = 25°C		–55°C to 125°C		–55°C to 150°C		UNIT
					TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>		V <sub>I</sub> = V <sub>IH</sub>	1.65 V to 4.5 V	1.65 V to 4.5 V			V <sub>CCO</sub> – 0.1		V <sub>CCO</sub> – 0.1		V
			1.65 V	1.65 V			1.2		1.2		
			2.3 V	2.3 V			1.9		1.9		
			3 V	3 V			2.4		2.4		
			4.5 V	4.5 V			3.8		3.8		
V <sub>OL</sub>		V <sub>I</sub> = V <sub>IL</sub>	1.65 V to 4.5 V	1.65 V to 4.5 V				0.1		0.1	V
			1.65 V	1.65 V				0.45		0.45	
			2.3 V	2.3 V				0.3		0.3	
			3 V	3 V				0.55		0.55	
			4.5 V	4.5 V				0.55		0.55	
I <sub>I</sub>	DIR	V <sub>I</sub> = V <sub>CCA</sub> or GND	1.65 V to 5.5 V	1.65 V to 5.5 V		±1		±2		±2	μA
I <sub>off</sub>	A port	V <sub>I</sub> or V <sub>O</sub> = 0 to 5.5 V	0 V	0 to 5.5 V		±1		±9		±9	μA
	B port		0 to 5.5 V	0 V		±1		±9		±9	
I <sub>OZ</sub>	A or B port	V <sub>O</sub> = V <sub>CCO</sub> or GND	1.65 V to 5.5 V	1.65 V to 5.5 V		±1		±9		±9	μA
I <sub>CCA</sub>		V <sub>I</sub> = V <sub>CCI</sub> or GND, I <sub>O</sub> = 0	1.65 V to 5.5 V	1.65 V to 5.5 V				4		4	μA
			5 V	0 V				2		2	
			0 V	5 V				–12		–12	
I <sub>CCB</sub>		V <sub>I</sub> = V <sub>CCI</sub> or GND, I <sub>O</sub> = 0	1.65 V to 5.5 V	1.65 V to 5.5 V				4		4	μA
			5 V	0 V				–12		–12	
			0 V	5 V				2		2	
I <sub>CCA</sub> + I <sub>CCB</sub> (see Table 3)		V <sub>I</sub> = V <sub>CCI</sub> or GND, I <sub>O</sub> = 0	1.65 V to 5.5 V	1.65 V to 5.5 V				4		4	μA
ΔI <sub>CCA</sub>	A port	One A port at V <sub>CCA</sub> – 0.6 V, DIR at V <sub>CCA</sub> , B port = open	3 V to 5.5 V	3 V to 5.5 V				50		50	μA
	DIR				DIR at V <sub>CCA</sub> – 0.6 V, B port = open, A port at V <sub>CCA</sub> or GND				50		
ΔI <sub>CCB</sub>	B port	One B port at V <sub>CCB</sub> – 0.6 V, DIR at GND, A port = open	3 V to 5.5 V	3 V to 5.5 V				50		50	μA
C <sub>I</sub>	DIR	V <sub>I</sub> = V <sub>CCA</sub> or GND	3.3 V	3.3 V		2.5					pF
C <sub>io</sub>	A or B port	V <sub>O</sub> = V <sub>CCA/B</sub> or GND	3.3 V	3.3 V		6					pF

 (1) V<sub>CCO</sub> is the V<sub>CC</sub> associated with the output port.

 (2) V<sub>CCI</sub> is the V<sub>CC</sub> associated with the input port.



**Notes:**

1. See datasheet for absolute maximum and minimum recommended operating conditions.
2. Silicon operating life design goal is 10 years at 105°C junction temperature (does not include package interconnect life).
3. Product disclaimer applies to DCU package 150°C.

**Figure 1. LVC2T45SDCU Operating Life Derating Chart**

## Switching Characteristics

over recommended operating free-air temperature range,  $V_{CCA} = 1.8\text{ V} \pm 0.15\text{ V}$  (unless otherwise noted) (see [Figure 2](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$		$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	A	B	3	21.7	2.2	14.3	1.7	12.3	1.4	11.2	ns
$t_{PHL}$			2.8	28.3	2.2	12.5	1.8	11.1	1.7	11	
$t_{PLH}$	B	A	3	21.7	2.3	20	2.1	19.5	1.9	19.1	ns
$t_{PHL}$			2.8	18.3	2.1	16.9	2	16.6	1.8	16.2	
$t_{PHZ}$	DIR	A	10.6	34.9	10.3	34.5	10.5	34.5	10.7	33.3	ns
$t_{PLZ}$			7.3	23.7	7.5	23.6	7.5	23.5	7	23.4	
$t_{PHZ}$	DIR	B	10	31.9	8.4	18.9	6.5	15.3	4.1	12.6	ns
$t_{PLZ}$			6.5	23.5	7.2	16.6	4.3	13.7	2.1	11.1	
$t_{PZH}^{(1)}$	DIR	A		45.2		36.6		33.2		30.2	ns
$t_{PZL}^{(1)}$				50.2		35.8		31.9		28.8	
$t_{PZH}^{(1)}$	DIR	B		45.4		37.9		35.8		34.6	ns
$t_{PZL}^{(1)}$				53.2		47		45.6		44.3	

(1) The enable time is a calculated value, derived using the formula shown in the *enable times* section.

## Switching Characteristics

over recommended operating free-air temperature range,  $V_{CCA} = 2.5\text{ V} \pm 0.2\text{ V}$  (unless otherwise noted) (see [Figure 2](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$		$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$		$V_{CCB} = 5\text{ V} \pm 0.5\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	A	B	2.3	20	1.5	12.5	1.3	10.4	1.1	9.1	ns
$t_{PHL}$			2.1	16.9	1.4	11.5	1.3	9.4	0.9	8.6	
$t_{PLH}$	B	A	2.2	14.3	1.5	12.5	1.4	12	1	11.5	ns
$t_{PHL}$			2.2	12.5	1.4	11.5	1.3	11	0.9	10.2	
$t_{PHZ}$	DIR	A	6.6	21.1	7.1	20.8	6.8	20.8	5.2	20.5	ns
$t_{PLZ}$			5.3	16.6	5.2	16.5	4.9	16.3	4.8	16.3	
$t_{PHZ}$	DIR	B	10.7	31.9	8.1	17.9	5.8	14.5	3.5	11.6	ns
$t_{PLZ}$			7.8	22.9	6.2	15.2	3.6	12.9	1.4	11.2	
$t_{PZH}^{(1)}$	DIR	A		37.2		27.7		24.9		21.7	ns
$t_{PZL}^{(1)}$				44.4		29.4		25.5		21.8	
$t_{PZH}^{(1)}$	DIR	B		26.6		29		26.7		25.4	ns
$t_{PZL}^{(1)}$				38		32.3		30.2		29.1	

(1) The enable time is a calculated value, derived using the formula shown in the *enable times* section.

## Switching Characteristics

over recommended operating free-air temperature range,  $V_{CCA} = 3.3 \text{ V} \pm 0.3 \text{ V}$  (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.8 \text{ V}$ $\pm 0.15 \text{ V}$		$V_{CCB} = 2.5 \text{ V}$ $\pm 0.2 \text{ V}$		$V_{CCB} = 3.3 \text{ V}$ $\pm 0.3 \text{ V}$		$V_{CCB} = 5 \text{ V}$ $\pm 0.5 \text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	A	B	2.1	19.5	1.4	12	0.7	9.6	0.7	8.4	ns
$t_{PHL}$			2	16.6	1.3	11	0.8	9	0.7	8	
$t_{PLH}$	B	A	1.7	12.3	1.3	10.4	0.7	9.8	0.6	9.4	ns
$t_{PHL}$			1.8	11.1	1.3	9.4	0.8	9	0.7	8.5	
$t_{PHZ}$	DIR	A	5	14.9	5.1	14.8	5	14.8	5	14.4	ns
$t_{PLZ}$			3.4	12.4	3.7	12.4	3.9	12.1	3.3	11.8	
$t_{PHZ}$	DIR	B	11.2	31.3	8	17.7	5.8	14.4	2.9	11.4	ns
$t_{PLZ}$			9.4	21.7	5.6	15.3	4.3	12.3	1	9.6	
$t_{PZH}^{(1)}$	DIR	A	34		25.7		22.1		19		ns
$t_{PZL}^{(1)}$			42.4		27.1		23.4		19.9		
$t_{PZH}^{(1)}$	DIR	B	31.9		24.4		21.9		20.2		ns
$t_{PZL}^{(1)}$			31.5		25.8		23.8		22.4		

(1) The enable time is a calculated value, derived using the formula shown in the *enable times* section.

## Switching Characteristics

over recommended operating free-air temperature range,  $V_{CCA} = 5 \text{ V} \pm 0.5 \text{ V}$  (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.8 \text{ V}$ $\pm 0.15 \text{ V}$		$V_{CCB} = 2.5 \text{ V}$ $\pm 0.2 \text{ V}$		$V_{CCB} = 3.3 \text{ V}$ $\pm 0.3 \text{ V}$		$V_{CCB} = 5 \text{ V}$ $\pm 0.5 \text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	A	B	1.9	19.1	1	11.5	0.6	9.4	0.5	7.9	ns
$t_{PHL}$			1.8	16.2	0.9	10.2	0.7	8.5	0.5	7.5	
$t_{PLH}$	B	A	1.4	11.2	1	9.1	0.7	8.4	0.5	7.9	ns
$t_{PHL}$			1.7	11	0.9	8.6	0.7	8	0.5	7.5	
$t_{PHZ}$	DIR	A	2.9	12.2	2.9	11.9	2.8	11.9	2.2	11.8	ns
$t_{PLZ}$			1.4	10.9	1.3	10.7	0.7	10.7	0.7	10.6	
$t_{PHZ}$	DIR	B	11.2	30.1	7.2	17.9	5.8	14.1	1.3	11.3	ns
$t_{PLZ}$			8.4	20.9	5	15	4	11.7	1	9.6	
$t_{PZH}^{(1)}$	DIR	A	32.1		24.1		20.1		18.5		ns
$t_{PZL}^{(1)}$			41.1		26.5		22.1		18.8		
$t_{PZH}^{(1)}$	DIR	B	30		22.2		20.1		18.5		ns
$t_{PZL}^{(1)}$			28.4		22.1		22.4		19.3		

(1) The enable time is a calculated value, derived using the formula shown in the *enable times* section.



## Operating Characteristics

 $T_A = 25^\circ\text{C}$ 

PARAMETER		TEST CONDITIONS	$V_{CCA} =$ $V_{CCB} = 1.8\text{ V}$	$V_{CCA} =$ $V_{CCB} = 2.5\text{ V}$	$V_{CCA} =$ $V_{CCB} = 3.3\text{ V}$	$V_{CCA} =$ $V_{CCB} = 5\text{ V}$	UNIT
			TYP	TYP	TYP	TYP	
$C_{pdA}$ (1)	A-port input, B-port output	$C_L = 0\text{ pF},$ $f = 10\text{ MHz},$ $t_r = t_f = 1\text{ ns}$	3	4	4	4	pF
	B-port input, A-port output		18	19	20	21	
$C_{pdB}$ (1)	A-port input, B-port output	$C_L = 0\text{ pF},$ $f = 10\text{ MHz},$ $t_r = t_f = 1\text{ ns}$	18	19	20	21	pF
	B-port input, A-port output		3	4	4	4	

(1) Power dissipation capacitance per transceiver

## Power-Up Considerations

A proper power-up sequence always should be followed to avoid excessive supply current, bus contention, oscillations, or other anomalies. To guard against such power-up problems, take the following precautions:

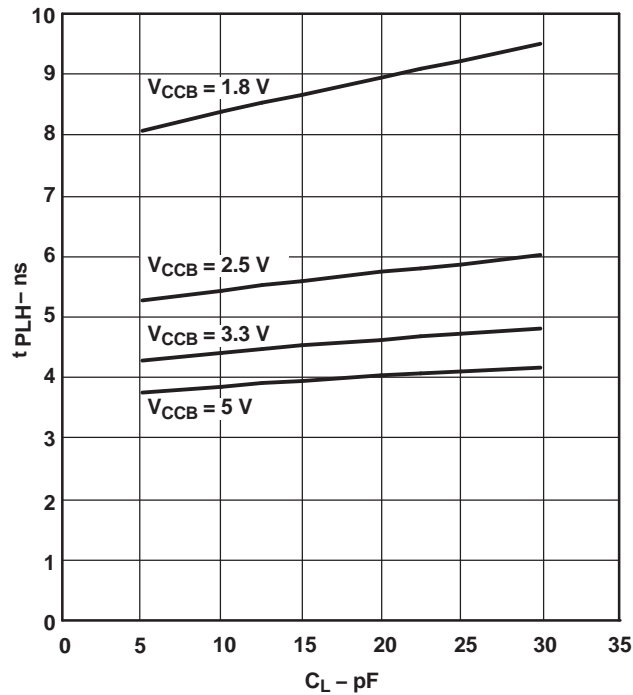
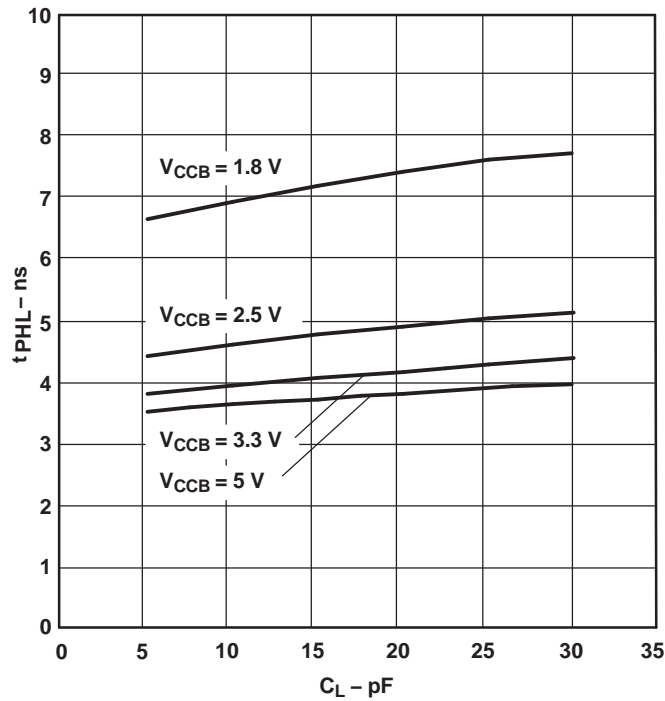
1. Connect ground before any supply voltage is applied.
2. Power up  $V_{CCA}$ .
3.  $V_{CCB}$  can be ramped up along with or after  $V_{CCA}$ .

**Table 3. Typical Total Static Power Consumption ( $I_{CCA} + I_{CCB}$ )**

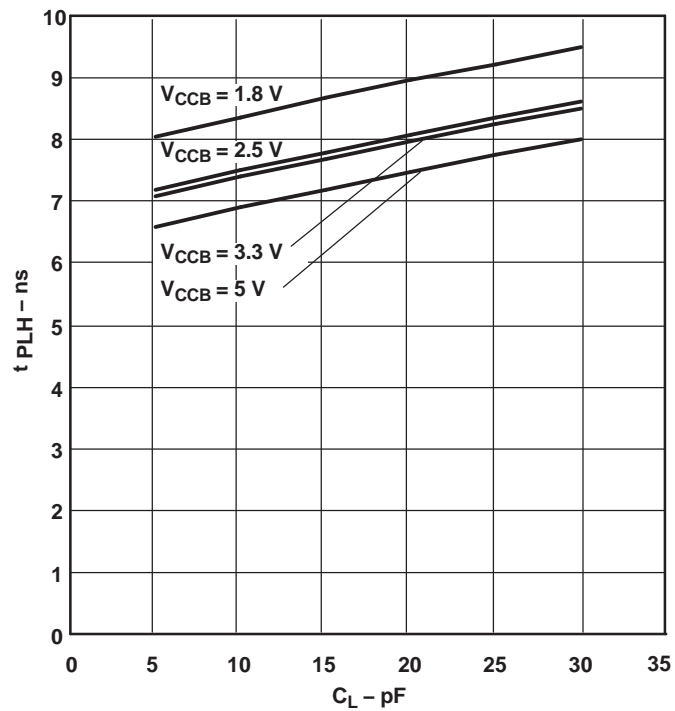
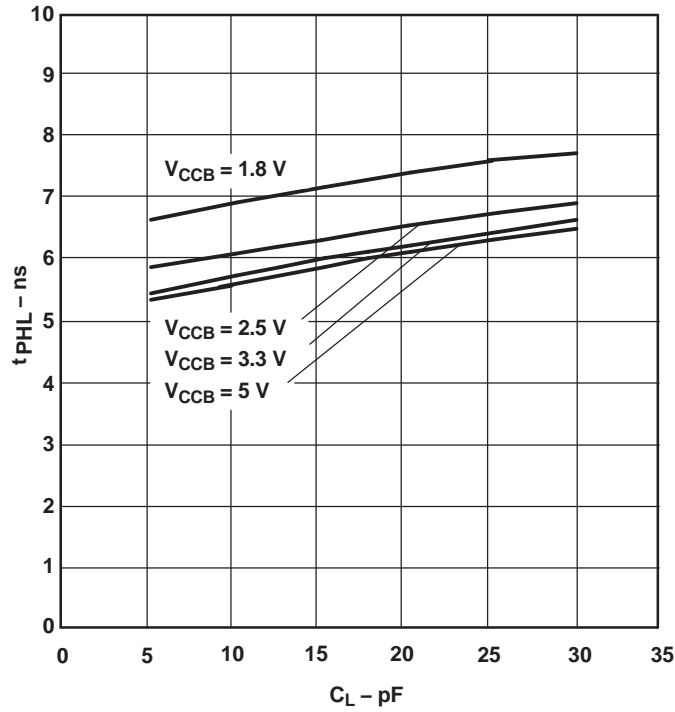
$V_{CCB}$	$V_{CCA}$					UNIT
	0 V	1.8 V	2.5 V	3.3 V	5 V	
0 V	0	<1	<1	<1	<1	μA
1.8 V	<1	<2	<2	<2	2	
2.5 V	<1	<2	<2	<2	<2	
3.3 V	<1	<2	<2	<2	<2	
5 V	<1	2	<2	<2	<2	

TYPICAL CHARACTERISTICS

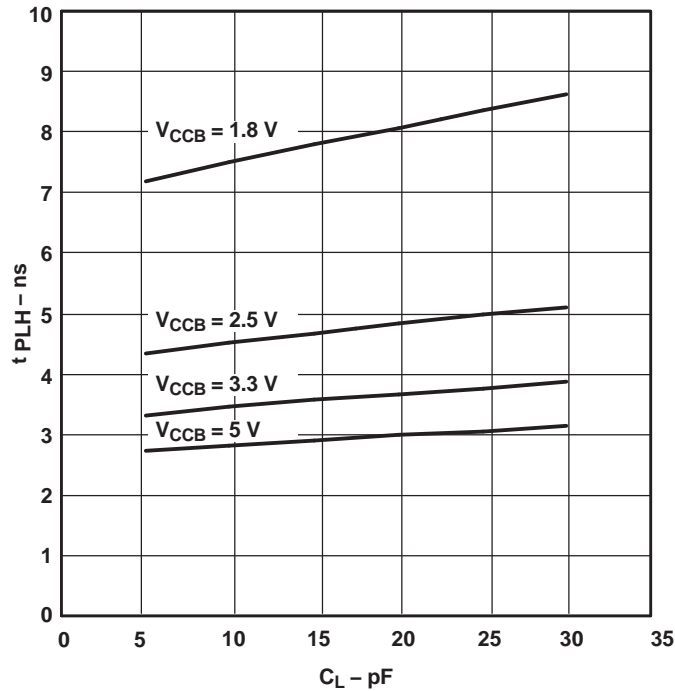
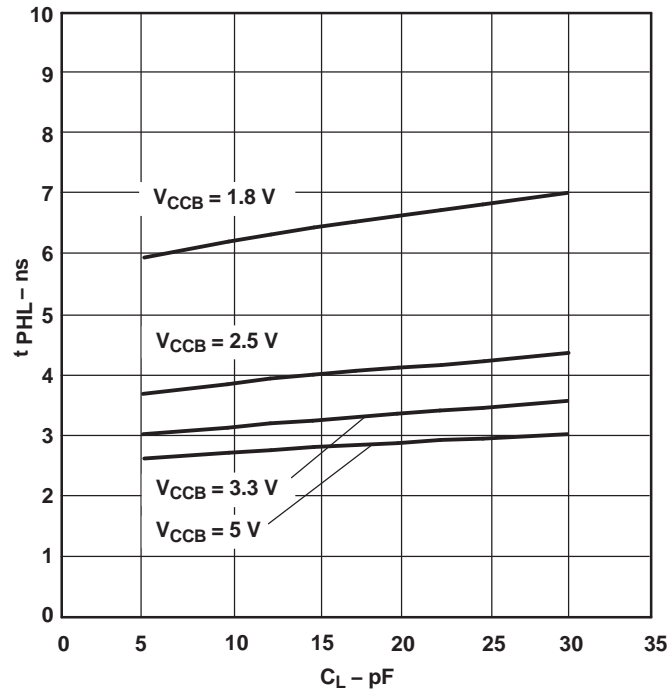
TYPICAL PROPAGATION DELAY (A to B) vs LOAD CAPACITANCE  
 $T_A = 25^\circ\text{C}$ ,  $V_{CCA} = 1.8\text{ V}$



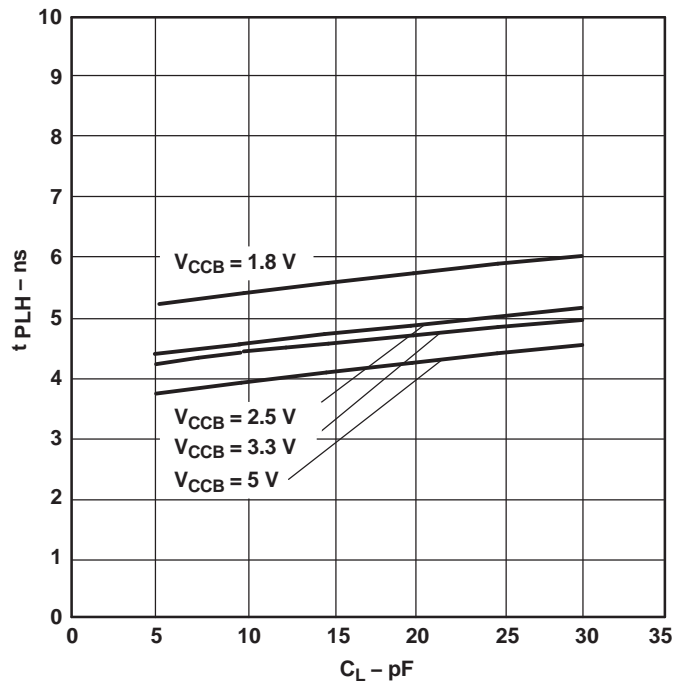
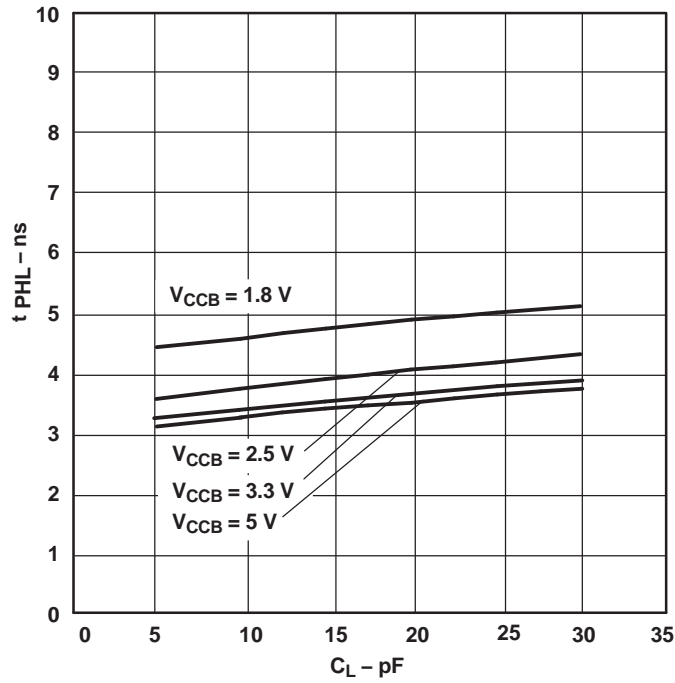
**TYPICAL PROPAGATION DELAY (B to A) vs LOAD CAPACITANCE**  
 $T_A = 25^\circ\text{C}, V_{CCA} = 1.8\text{ V}$



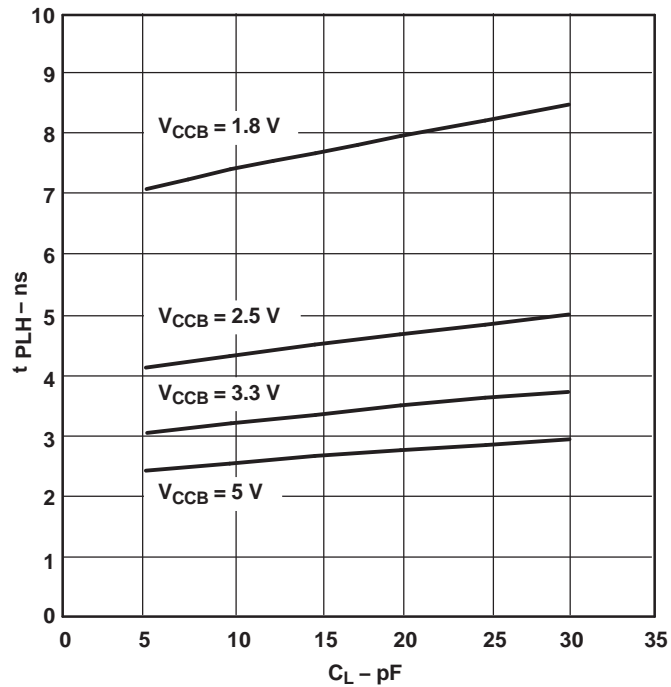
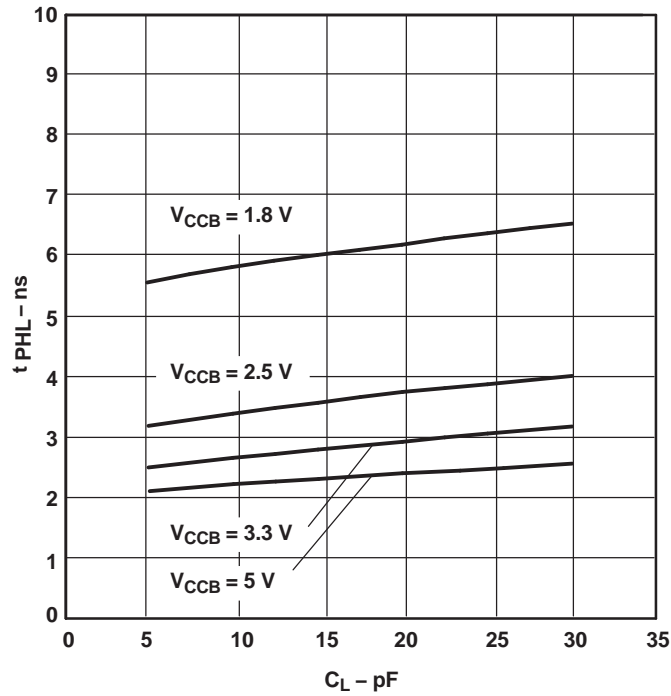
**TYPICAL PROPAGATION DELAY (A to B) vs LOAD CAPACITANCE**  
 $T_A = 25^\circ\text{C}$ ,  $V_{CCA} = 2.5\text{ V}$



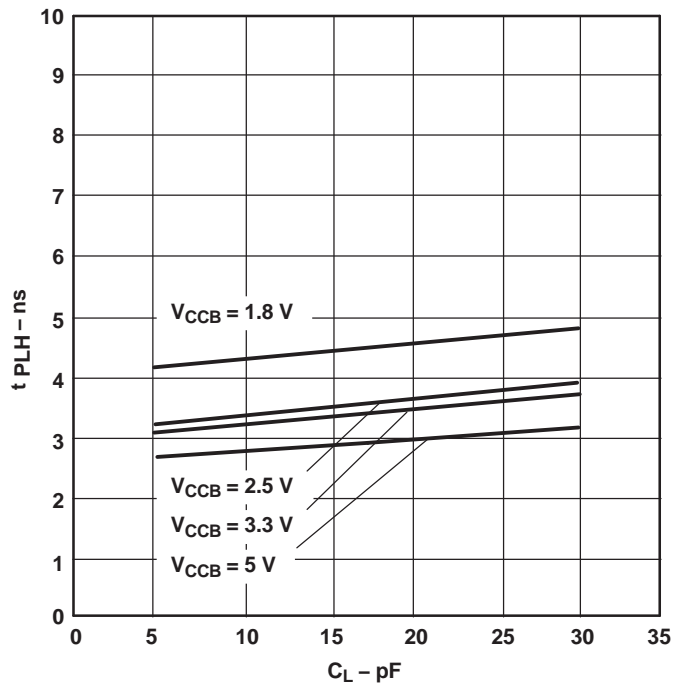
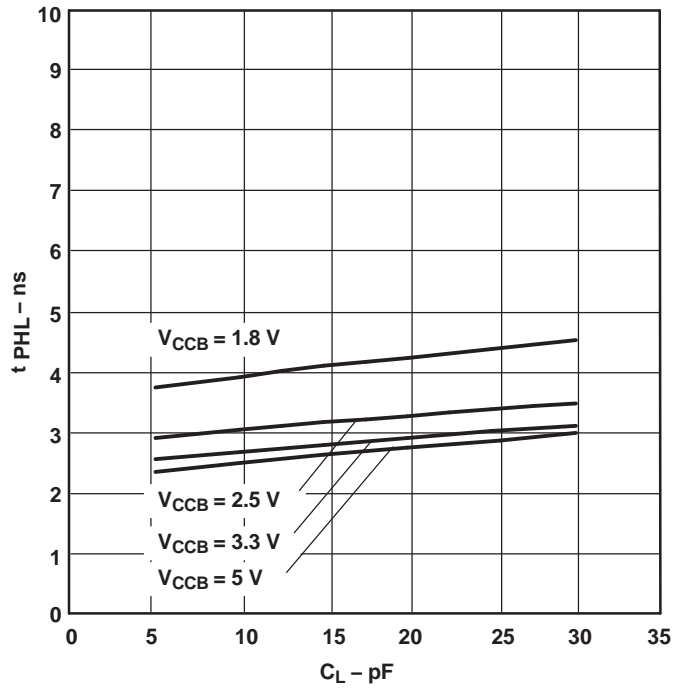
**TYPICAL PROPAGATION DELAY (B to A) vs LOAD CAPACITANCE**  
 $T_A = 25^\circ\text{C}, V_{CCA} = 2.5\text{ V}$



**TYPICAL PROPAGATION DELAY (A to B) vs LOAD CAPACITANCE**  
 $T_A = 25^\circ\text{C}$ ,  $V_{CCA} = 3.3\text{ V}$

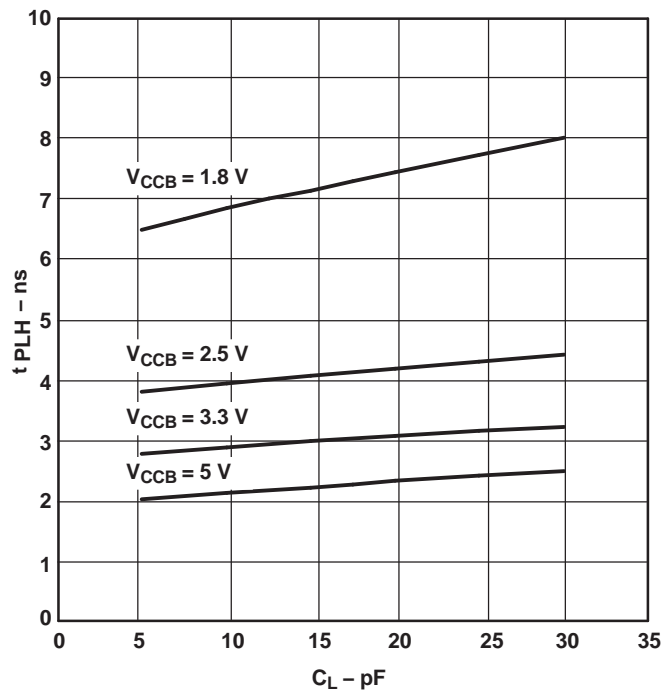
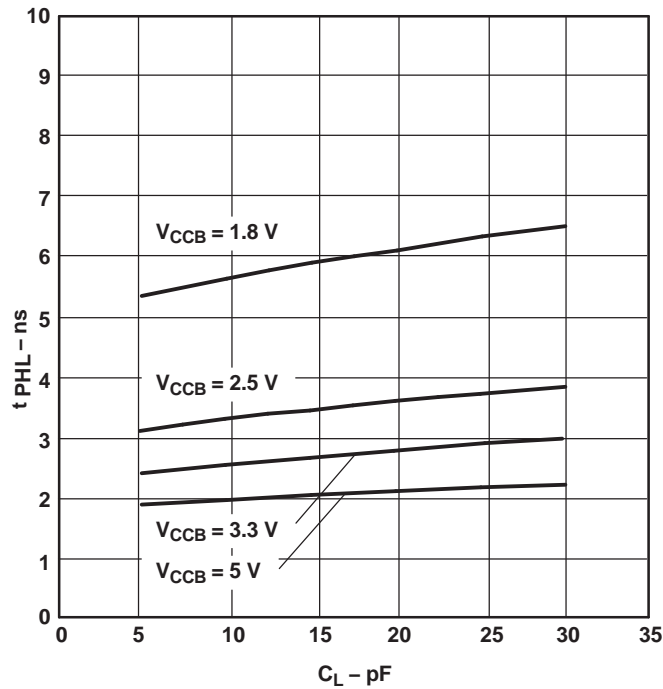


**TYPICAL PROPAGATION DELAY (B to A) vs LOAD CAPACITANCE**  
 $T_A = 25^\circ\text{C}, V_{CCA} = 3.3\text{ V}$

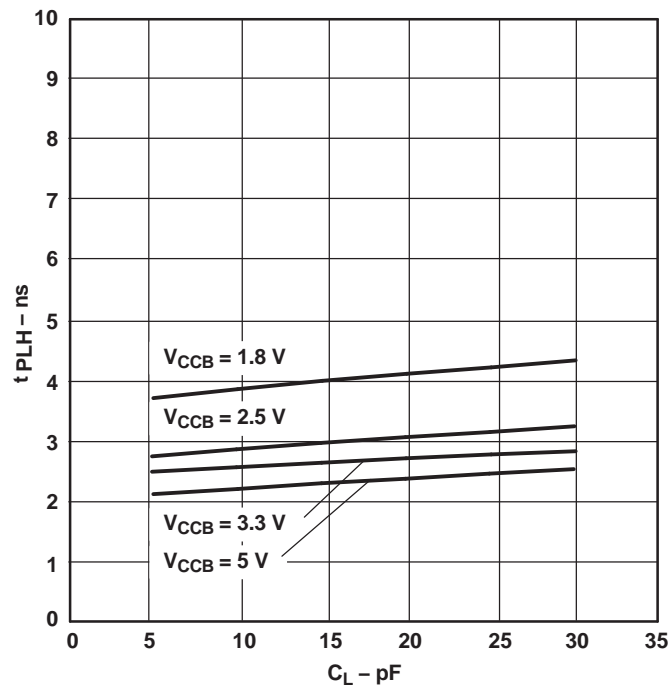
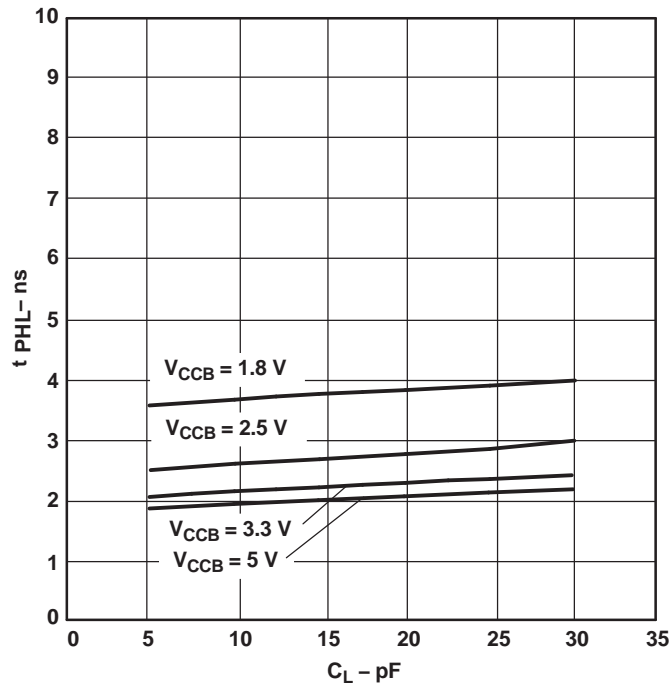




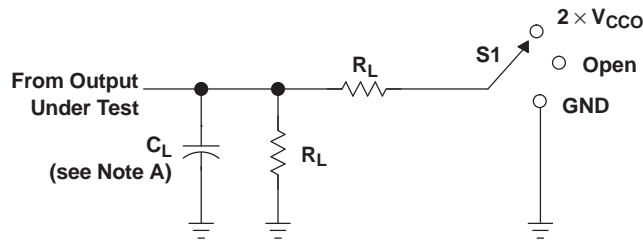
**TYPICAL PROPAGATION DELAY (A to B) vs LOAD CAPACITANCE**  
 $T_A = 25^\circ\text{C}$ ,  $V_{CCA} = 5\text{ V}$



**TYPICAL PROPAGATION DELAY (B to A) vs LOAD CAPACITANCE**  
 $T_A = 25^\circ\text{C}, V_{CCA} = 5\text{ V}$



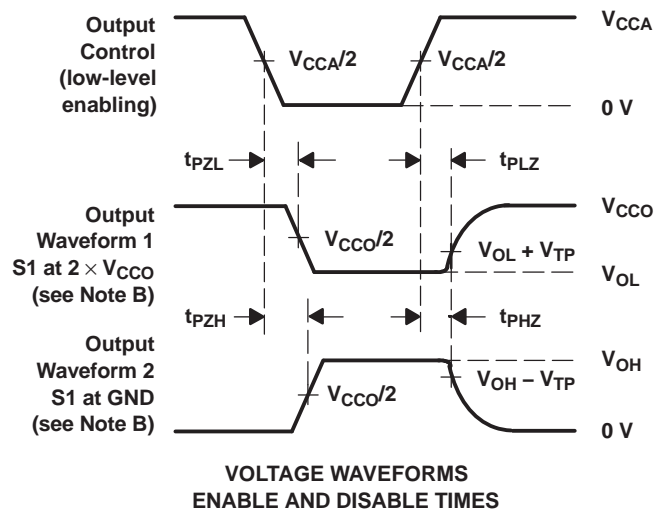
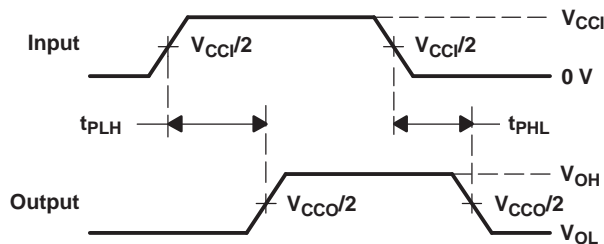
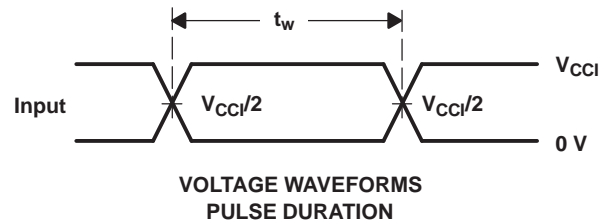
PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

TEST	S1
$t_{pd}$	Open
$t_{PLZ}/t_{PZL}$	$2 \times V_{CCO}$
$t_{PHZ}/t_{PZH}$	GND

$V_{CCO}$	$C_L$	$R_L$	$V_{TP}$
$1.8\text{ V} \pm 0.15\text{ V}$	15 pF	2 k $\Omega$	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	15 pF	2 k $\Omega$	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	15 pF	2 k $\Omega$	0.3 V
$5\text{ V} \pm 0.5\text{ V}$	15 pF	2 k $\Omega$	0.3 V

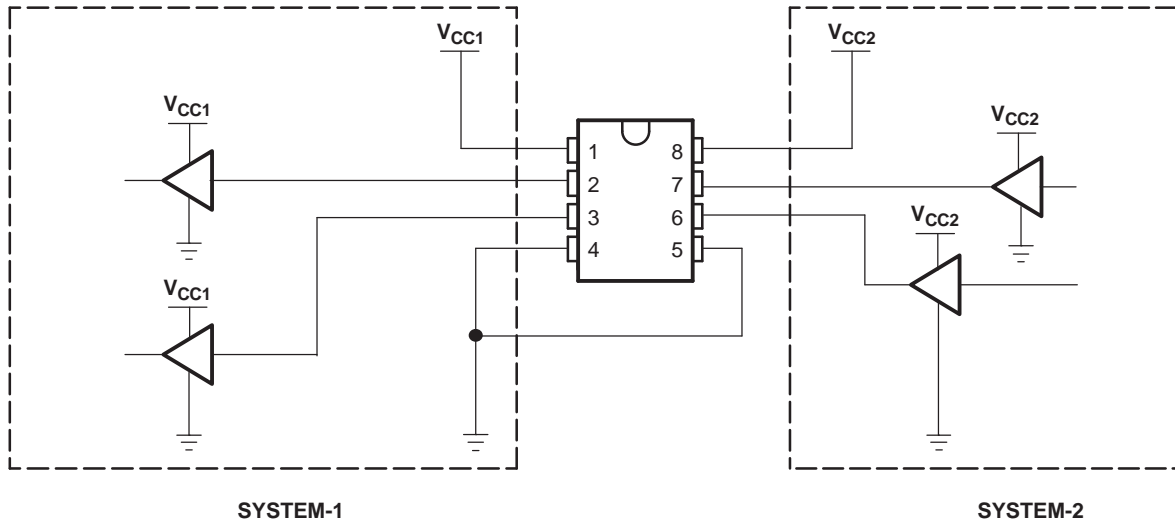


- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50\ \Omega$ ,  $dv/dt \geq 1\text{ V/ns}$ .
  - D. The outputs are measured one at a time, with one transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - H.  $V_{CCI}$  is the  $V_{CC}$  associated with the input port.
  - I.  $V_{CCO}$  is the  $V_{CC}$  associated with the output port.
  - J. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

## APPLICATION INFORMATION

The following shows an example of the SN74LVC2T45 being used in a unidirectional logic level-shifting application.

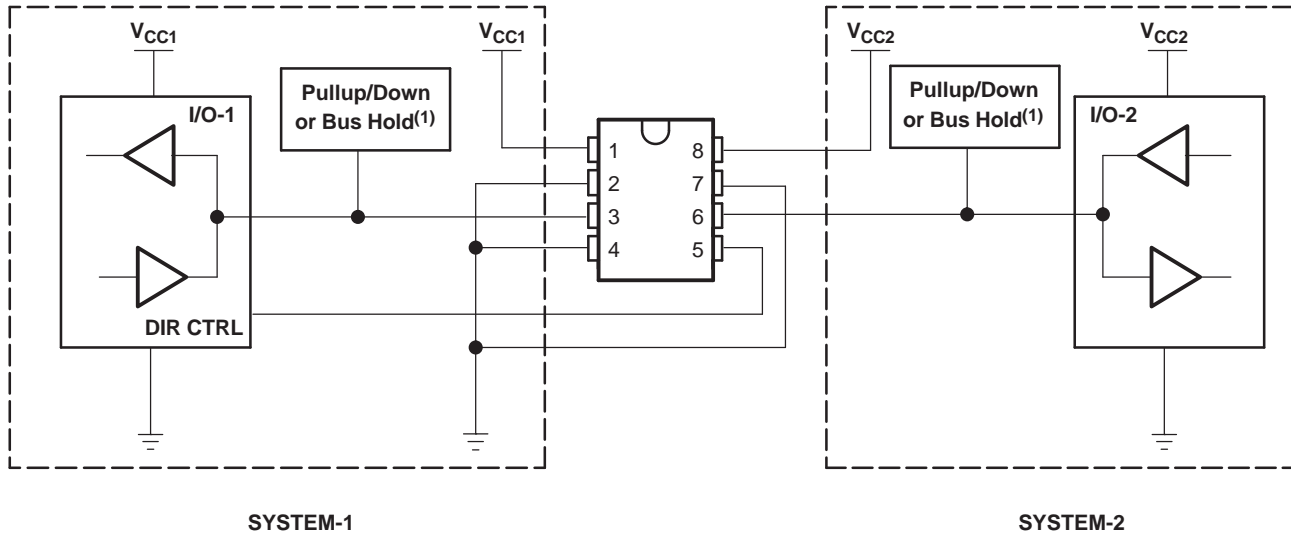


PIN	NAME	FUNCTION	DESCRIPTION
1	$V_{CCA}$	$V_{CC1}$	SYSTEM-1 supply voltage (1.65 V to 5.5 V)
2	A1	OUT1	Output level depends on $V_{CC1}$ voltage.
3	A2	OUT2	Output level depends on $V_{CC1}$ voltage.
4	GND	GND	Device GND
5	DIR	DIR	GND (low level) determines B-port to A-port direction.
6	B2	IN2	Input threshold value depends on $V_{CC2}$ voltage.
7	B1	IN1	Input threshold value depends on $V_{CC2}$ voltage.
8	$V_{CCB}$	$V_{CC2}$	SYSTEM-2 supply voltage (1.65 V to 5.5 V)

**Figure 3. Unidirectional Logic Level-Shifting Application**

## APPLICATION INFORMATION

Figure 4 shows the SN74LVC2T45 being used in a bidirectional logic level-shifting application. Since the SN74LVC2T45 does not have an output-enable (OE) pin, the system designer should take precautions to avoid bus contention between SYSTEM-1 and SYSTEM-2 when changing directions.



The following table shows data transmission from SYSTEM-1 to SYSTEM-2 and then from SYSTEM-2 to SYSTEM-1.

STATE	DIR CTRL	I/O-1	I/O-2	DESCRIPTION
1	H	Out	In	SYSTEM-1 data to SYSTEM-2
2	H	Hi-Z	Hi-Z	SYSTEM-2 is getting ready to send data to SYSTEM-1. I/O-1 and I/O-2 are disabled. The bus-line state depends on pullup or pulldown. <sup>(1)</sup>
3	L	Hi-Z	Hi-Z	DIR bit is flipped. I/O-1 and I/O-2 still are disabled. The bus-line state depends on pullup or pulldown. <sup>(1)</sup>
4	L	In	Out	SYSTEM-2 data to SYSTEM-1

(1) SYSTEM-1 and SYSTEM-2 must use the same conditions, i.e., both pullup or both pulldown.

**Figure 4. Bidirectional Logic Level-Shifting Application**



### Enable Times

Calculate the enable times for the SN74LVC2T45 using the following formulas:

- $t_{PZH} \text{ (DIR to A)} = t_{PLZ} \text{ (DIR to B)} + t_{PLH} \text{ (B to A)}$
- $t_{PZL} \text{ (DIR to A)} = t_{PHZ} \text{ (DIR to B)} + t_{PHL} \text{ (B to A)}$
- $t_{PZH} \text{ (DIR to B)} = t_{PLZ} \text{ (DIR to A)} + t_{PLH} \text{ (A to B)}$
- $t_{PZL} \text{ (DIR to B)} = t_{PHZ} \text{ (DIR to A)} + t_{PHL} \text{ (A to B)}$

In a bidirectional application, these enable times provide the maximum delay from the time the DIR bit is switched until an output is expected. For example, if the SN74LVC2T45 initially is transmitting from A to B, then the DIR bit is switched; the B port of the device must be disabled before presenting it with an input. After the B port has been disabled, an input signal applied to it appears on the corresponding A port after the specified propagation delay.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVC2T45MDCTTEP	ACTIVE	SM8	DCT	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	NXR Z	
V62/09604-01XE	ACTIVE	SM8	DCT	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	NXR Z	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN74LVC2T45-EP :**

- Catalog: [SN74LVC2T45](#)
- Automotive: [SN74LVC2T45-Q1](#)

## NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects



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NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.



# EXAMPLE BOARD LAYOUT

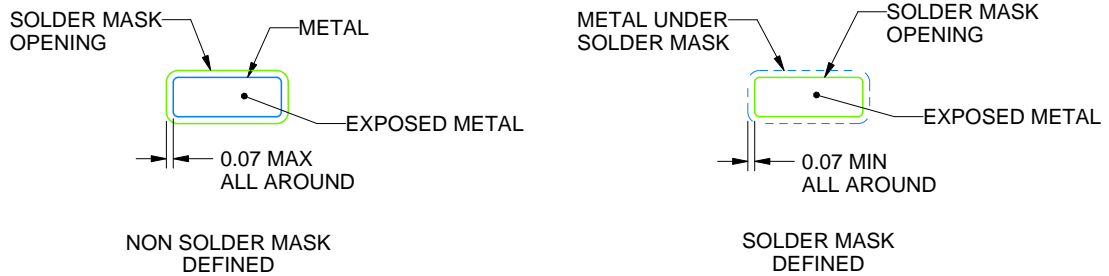
DCT0008A

SSOP - 1.3 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DCT0008A

SSOP - 1.3 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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