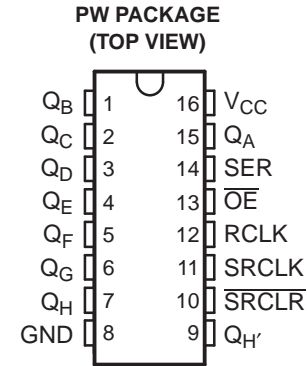


## FEATURES

- Qualified for Automotive Applications
- Operating Range 2-V to 5.5-V  $V_{CC}$
- 8-Bit Serial-In, Parallel-Out Shift
- Shift Register Has Direct Clear



## DESCRIPTION/ORDERING INFORMATION

The SN74AHC595 contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has parallel 3-state outputs. Separate clocks are provided for both the shift and storage registers. The shift register has a direct overriding clear ( $\overline{SRCLR}$ ) input, serial (SER) input, and a serial output for cascading. When the output-enable ( $\overline{OE}$ ) input is high, all outputs, except  $Q_{H'}$ , are in the high-impedance state.

Both the shift-register clock (SRCLK) and storage-register clock (RCLK) are positive-edge triggered. If both clocks are connected together, the shift register always is one clock pulse ahead of the storage register.

### ORDERING INFORMATION<sup>(1)</sup>

$T_A$	PACKAGE <sup>(2)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	TSSOP – PW	Reel of 2000	SN74AHC595QPWRQ1	HA595Q

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).  
 (2) Package drawings, thermal data, and symbolization are available at [www.ti.com/packaging](http://www.ti.com/packaging).

### FUNCTION TABLE

INPUTS					FUNCTION
SER	SRCLK	$\overline{SRCLR}$	RCLK	$\overline{OE}$	
X	X	X	X	H	Outputs $Q_A$ – $Q_H$ are disabled.
X	X	X	X	L	Outputs $Q_A$ – $Q_H$ are enabled.
X	X	L	X	X	Shift register is cleared.
L	↑	H	X	X	First stage of the shift register goes low. Other stages store the data of previous stage, respectively.
H	↑	H	X	X	First stage of the shift register goes high. Other stages store the data of previous stage, respectively.
X	X	X	↑	X	Shift-register data is stored into the storage register.

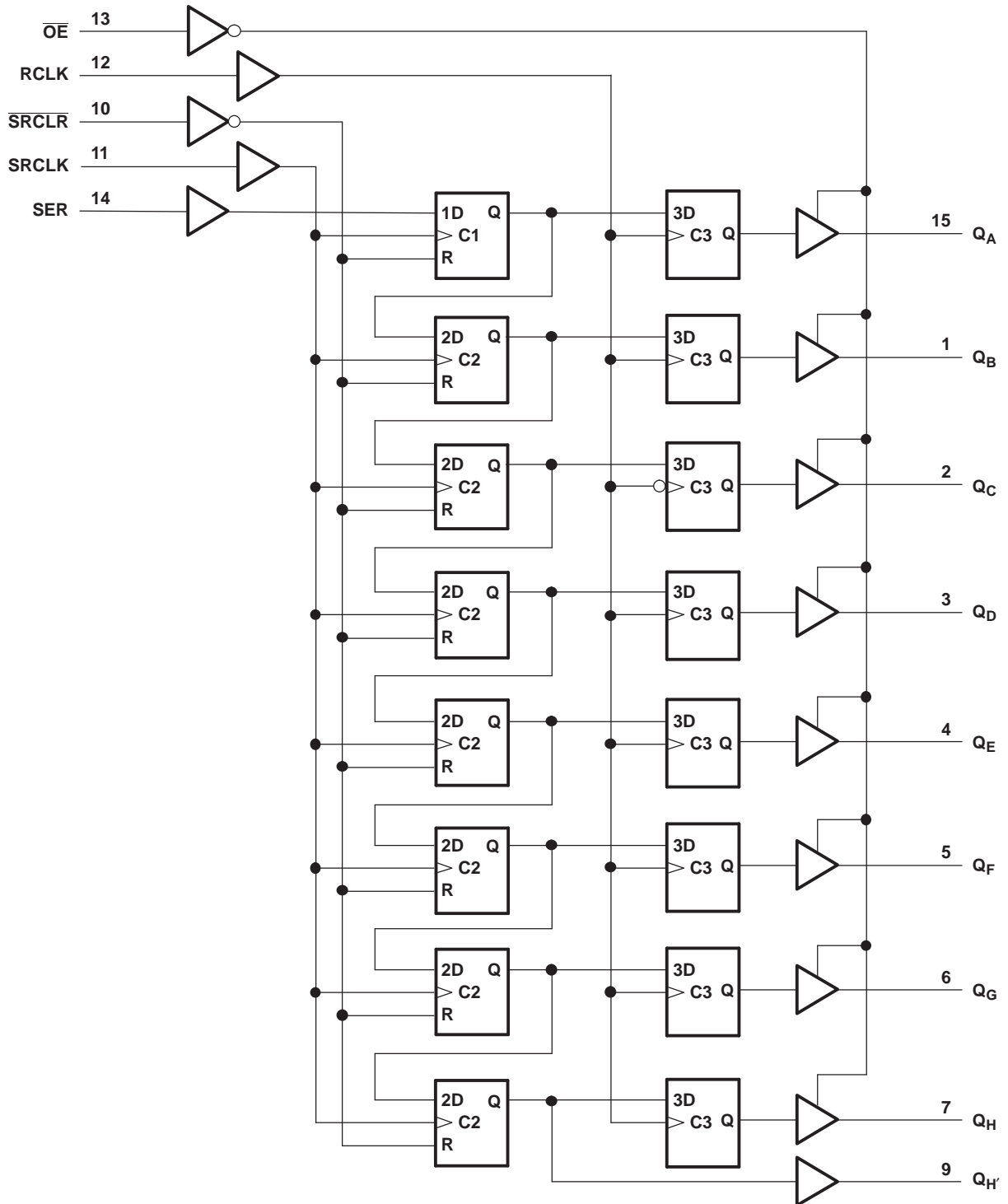


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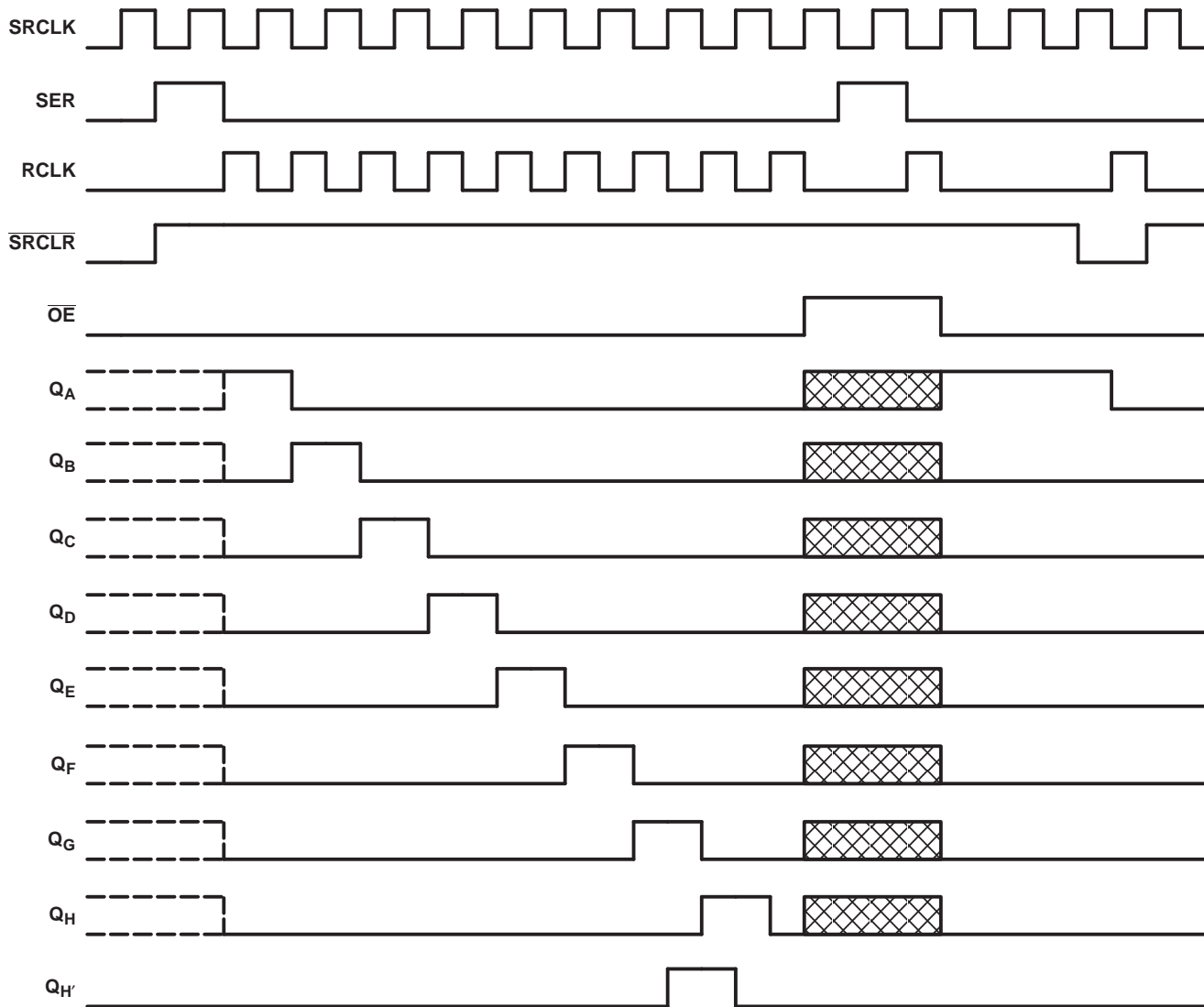
# SN74AHC595-Q1 8-BIT SHIFT REGISTER WITH 3-STATE OUTPUT REGISTERS

SCLS537B—AUGUST 2003—REVISED JANUARY 2008

## LOGIC DIAGRAM (POSITIVE LOGIC)



**TIMING DIAGRAM**



# SN74AHC595-Q1

## 8-BIT SHIFT REGISTER

### WITH 3-STATE OUTPUT REGISTERS

SCLS537B–AUGUST 2003–REVISED JANUARY 2008

#### ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

$V_{CC}$	Supply voltage range		–0.5 V to 7 V
$V_I$	Input voltage range <sup>(2)</sup>		–0.5 V to 7 V
$V_O$	Output voltage range <sup>(2)</sup>		–0.5 V to $V_{CC} + 0.5$ V
$I_{IK}$	Input clamp current	$V_I < 0$	–20 mA
$I_{OK}$	Output clamp current	$V_O < 0$ or $V_O > V_{CC}$	±20 mA
$I_O$	Continuous output current	$V_O = 0$ to $V_{CC}$	±25 mA
	Continuous current through $V_{CC}$ or GND		±75 mA
$\theta_{JA}$	Package thermal impedance, junction to free air <sup>(3)</sup>		108°C/W
$T_{stg}$	Storage temperature range		–65°C to 150°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.

#### RECOMMENDED OPERATING CONDITIONS<sup>(1)</sup>

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	2	5.5	V
$V_{IH}$	High-level input voltage	$V_{CC} = 2$ V	1.5	V
		$V_{CC} = 3$ V	2.1	
		$V_{CC} = 5.5$ V	3.85	
$V_{IL}$	Low-level input voltage	$V_{CC} = 2$ V	0.5	V
		$V_{CC} = 3$ V	0.9	
		$V_{CC} = 5.5$ V	1.65	
$V_I$	Input voltage	0	5.5	V
$V_O$	Output voltage	0	$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 2$ V	–50	μA
		$V_{CC} = 3.3$ V ± 0.3 V	–4	
		$V_{CC} = 5$ V ± 0.5 V	–8	
$I_{OL}$	Low-level output current	$V_{CC} = 2$ V	50	μA
		$V_{CC} = 3.3$ V ± 0.3 V	4	
		$V_{CC} = 5$ V ± 0.5 V	8	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 3.3$ V ± 0.3 V	100	ns/V
		$V_{CC} = 5$ V ± 0.5 V	20	
$T_A$	Operating free-air temperature	I-suffix devices	–40	°C
		Q-suffix devices	–40	

- (1) All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

## ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V <sub>OH</sub>	I <sub>OH</sub> = -50 μA	2 V	1.9	2		1.9	V	
		3 V	2.9	3		2.9		
		4.5 V	4.4	4.5		4.4		
	I <sub>OH</sub> = -4 mA	3 V	2.58			2.48		
	I <sub>OH</sub> = -8 mA	4.5 V	3.94			3.8		
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	2 V			0.1	0.1	V	
		3 V			0.1	0.1		
		4.5 V			0.1	0.1		
	I <sub>OL</sub> = 4 mA	3 V			0.36	0.44		
	I <sub>OL</sub> = 8 mA	4.5 V			0.36	0.44		
I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	0 V to 5.5 V			±0.1	±1	μA	
I <sub>oz</sub>	Q <sub>A</sub> -Q <sub>H</sub> , V <sub>I</sub> = V <sub>CC</sub> or GND, V <sub>O</sub> = V <sub>CC</sub> or GND, $\overline{OE}$ = V <sub>IH</sub> or V <sub>IL</sub>	5.5 V			±0.25	±10	μA	
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V			4	40	μA	
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		3	10	10	pF	
C <sub>o</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5 V		5.5			pF	

## TIMING REQUIREMENTS

V<sub>CC</sub> = 3.3 V ± 0.3 V, over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		T <sub>A</sub> = 25°C		MIN	MAX	UNIT
		MIN	MAX			
t <sub>w</sub>	Pulse duration	SRCLK high or low	5.5		6.5	ns
		RCLK high or low	5.5		6.5	
		$\overline{SRCLR}$ low	5		6	
t <sub>su</sub>	Setup time	SER before SRCLK↑	3.5		4.5	ns
		SRCLK↑ before RCLK↑ <sup>(1)</sup>	8		9.5	
		$\overline{SRCLR}$ low before RCLK↑	8		10	
		$\overline{SRCLR}$ high (inactive) before SRCLK↑	3		4	
t <sub>h</sub>	Hold time	SER after SRCLK↑	1.5		2.5	ns

(1) This setup time allows the storage register to receive stable data from the shift register. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.

## TIMING REQUIREMENTS

V<sub>CC</sub> = 5 V ± 0.5 V, over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

		T <sub>A</sub> = 25°C		MIN	MAX	UNIT
		MIN	MAX			
t <sub>w</sub>	Pulse duration	SRCLK high or low	5		6	ns
		RCLK high or low	5		6	
		$\overline{SRCLR}$ low	5.2		6.2	
t <sub>su</sub>	Setup time	SER before SRCLK↑	3		4	ns
		SRCLK↑ before RCLK↑ <sup>(1)</sup>	5		6	
		$\overline{SRCLR}$ low before RCLK↑	5		6	
		$\overline{SRCLR}$ high (inactive) before SRCLK↑	2.5		3.5	
t <sub>h</sub>	Hold time	SER after SRCLK↑	2		3	ns

(1) This setup time allows the storage register to receive stable data from the shift register. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.

# SN74AHC595-Q1

## 8-BIT SHIFT REGISTER

### WITH 3-STATE OUTPUT REGISTERS

SCLS537B–AUGUST 2003–REVISED JANUARY 2008

#### SWITCHING CHARACTERISTICS

$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ , over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
				MIN	TYP	MAX			
$f_{\max}$			$C_L = 50\text{ pF}$	55	105		40		MHz
$t_{\text{PLH}}$	RCLK	$Q_A-Q_H$	$C_L = 50\text{ pF}$	7.9	15.4		1	20	ns
$t_{\text{PHL}}$				7.9	15.4		1	20	
$t_{\text{PLH}}$	SRCLK	$Q_{H'}$	$C_L = 50\text{ pF}$	9.2	16.5		1	21.5	ns
$t_{\text{PHL}}$				9.2	16.5		1	21.5	
$t_{\text{PHL}}$	$\overline{\text{SRCLR}}$	$Q_{H'}$	$C_L = 50\text{ pF}$	9	16.3		1	20.2	ns
$t_{\text{PZH}}$	$\overline{\text{OE}}$	$Q_A-Q_H$	$C_L = 50\text{ pF}$	7.8	15		1	20	ns
$t_{\text{PZL}}$				9.6	15		1	20	
$t_{\text{PHZ}}$	$\overline{\text{OE}}$	$Q_A-Q_H$	$C_L = 50\text{ pF}$	8.1	15.7		1	19.2	ns
$t_{\text{PLZ}}$				9.3	15.7		1	19.2	

#### SWITCHING CHARACTERISTICS

$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ , over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 1](#))

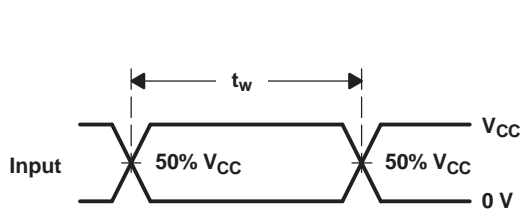
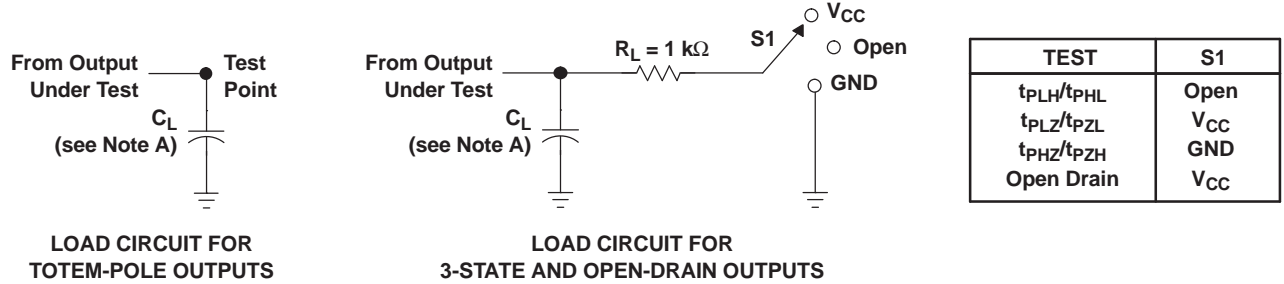
PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
				MIN	TYP	MAX			
$f_{\max}$			$C_L = 50\text{ pF}$	95	140		75		MHz
$t_{\text{PLH}}$	RCLK	$Q_A-Q_H$	$C_L = 50\text{ pF}$	5.6	9.4		1	13.5	ns
$t_{\text{PHL}}$				5.6	9.4		1	13.5	
$t_{\text{PLH}}$	SRCLK	$Q_{H'}$	$C_L = 50\text{ pF}$	6.4	10.2		1	14.4	ns
$t_{\text{PHL}}$				6.4	10.2		1	14.4	
$t_{\text{PHL}}$	$\overline{\text{SRCLR}}$	$Q_{H'}$	$C_L = 50\text{ pF}$	6.4	10		1	14.1	ns
$t_{\text{PZH}}$	$\overline{\text{OE}}$	$Q_A-Q_H$	$C_L = 50\text{ pF}$	5.7	10.6		1	15	ns
$t_{\text{PZL}}$				6.8	10.6		1	15	
$t_{\text{PHZ}}$	$\overline{\text{OE}}$	$Q_A-Q_H$	$C_L = 50\text{ pF}$	3.5	10.3		1	14	ns
$t_{\text{PLZ}}$				3.4	10.3		1	14	

#### OPERATING CHARACTERISTICS

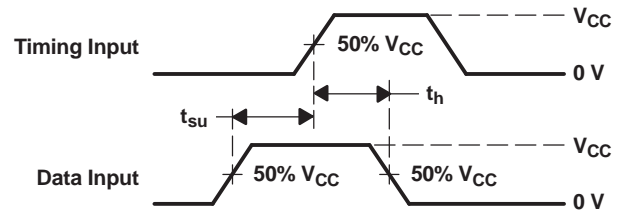
$V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{\text{pd}}$ Power dissipation capacitance	No load, $f = 10\text{ MHz}$	114	pF

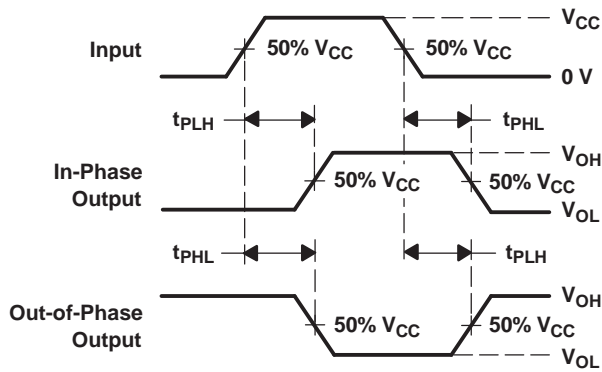
PARAMETER MEASUREMENT INFORMATION



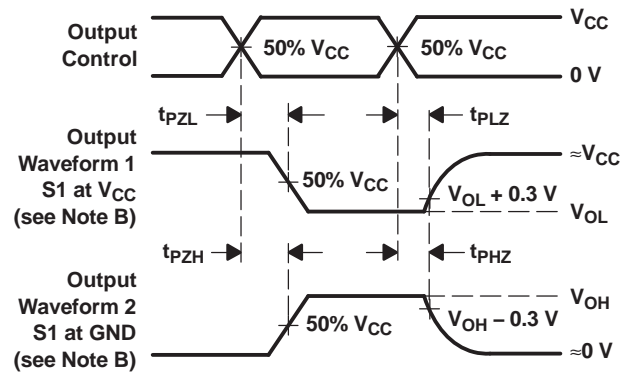
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 3\text{ ns}$ ,  $t_f \leq 3\text{ ns}$ .  
 D. The outputs are measured one at a time, with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AHC595QPWRQ1	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HA595Q	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN74AHC595-Q1 :**



- Catalog: [SN74AHC595](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC595QPWRQ1	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC595QPWRQ1	TSSOP	PW	16	2000	853.0	449.0	35.0



4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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