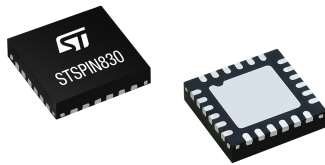


## Compact and versatile three-phase and three-sense motor driver



### Features

- Operating voltage from 7 to 45 V
- Maximum output current 1.5 A<sub>rms</sub>
- R<sub>DSon</sub> HS + LS = 1 Ω typ.
- Supporting both single and three shunts architectures
- Current control with adjustable OFF time
- Current sensing based on external shunt resistors
- Flexible driving methodology user settable between 6 inputs (high side & low side driving) and 3 inputs (direct PWM driving)
- FOC compatible thanks to three shunts sensing topology support
- Full protections set:
  - Non-dissipative overcurrent protection
  - Short-circuit protection
  - Undervoltage Lockout
  - Thermal shutdown
  - Interlocking function
- Low standby current consumption

### Application


- Industrial robotics
- Medical and health care
- Factory automation end-points
- Home appliances
- Small pumps
- Server, computing and general purpose FANs
- Office and home automation

### Description

**STSPIN830** is a compact and versatile field oriented control FOC ready three-phase motor driver. It integrates in a very small 4 x 4 mm QFN package, both the control logic and a fully protected low R<sub>DSon</sub> triple half-bridge power stage. Thanks to a dedicated MODE input pin the device offers the freedom to decide whether to drive it through 6 inputs (one for each power switch) or a more common 3 PWM direct driving inputs.

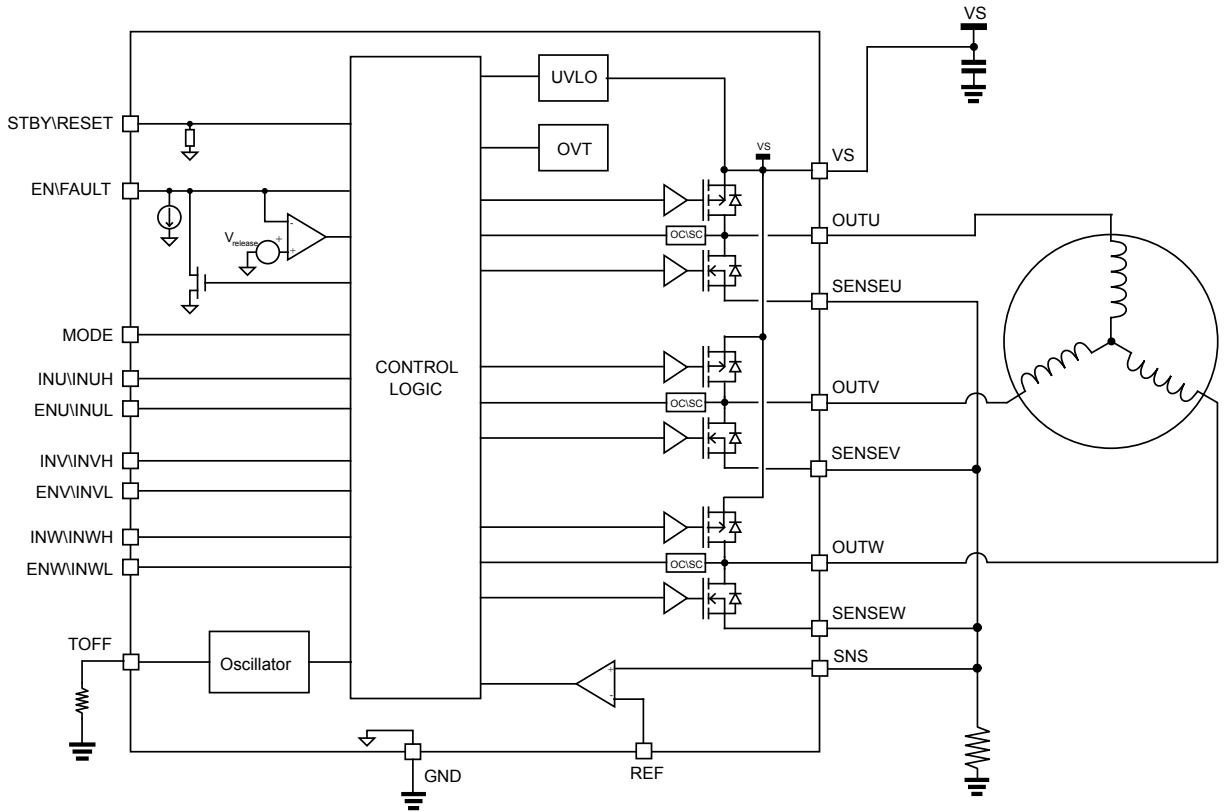
The **STSPIN830** supports both single and three shunts architectures and embeds a PWM current limiter based on user settable values of reference voltage and OFF time. The devices can be forced in a low consumption state reducing the total current consumption down to less than 45 μA.

As with all other devices from the STSPIN family, the **STSPIN830** integrates a complete set of protections for the power stages (non-dissipative overcurrent, thermal shutdown, short-circuit, undervoltage lockout and interlocking) making it a bulletproof solution for the new wave of demanding industrial applications.

Product status link	
<a href="#">STSPIN830</a>	
Product summary	
Order code	<a href="#">STSPIN830</a>
Package	TFQFPN 4 x 4 x 1.05 - 24L
Packing	Tape and reel
Product label	
	

# 1 Block diagram

Figure 1. STSPIN830 block diagram



## 2 Electrical data

### 2.1 Absolute maximum ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
V <sub>S</sub>	Supply voltage	-0.3 to 48	V
V <sub>IN</sub>	Logic input voltage	-0.3 to 5.5	V
V <sub>OUT,diff</sub>	Differential voltage between VSx, OUTU, OUTV, OUTW and SENSEx pins	up to 48	V
V <sub>SENSE</sub>	Sense pins voltage <sup>(1)</sup>	-2 to 2	V
V <sub>REF</sub>	Reference voltage input	-0.3 to 2	V
I <sub>OUT,RMS</sub>	Continuous power stage output current (each bridge)	1.5	A <sub>rms</sub>
T <sub>j</sub>	Junction temperature	-40 to 150	°C
T <sub>STG</sub>	Storage temperature	-55 to 150	°C

1. SENSEU, SENSEV, SENSEW, SNS.

### 2.2 Recommended operating conditions

**Table 2. Recommended operating conditions**

Symbol	Parameter	Min	Typ	Max	Unit
V <sub>S</sub>	Supply voltage	7	-	45	V
V <sub>IN</sub>	Logic input voltage		-	5	V
V <sub>SENSE</sub>	Sense pins voltage	-1	-	+1	V
V <sub>REF</sub>	Reference voltage input	0.1	-	1	V
f <sub>SW</sub>	Switching frequency			400	kHz

### 2.3 Thermal data

**Table 3. Thermal data**

Symbol	Parameter	Conditions	Value	Unit
R <sub>thJA</sub>	Junction-to-ambient thermal resistance	Natural convection, according to JESD51-2a 1	36.5	°C/W
R <sub>thJctop</sub>	Junction-to-case thermal resistance (top side)	Cold plate on top package, according to JESD51-121	27.6	°C/W
R <sub>thJcbot</sub>	Junction-to-case thermal resistance (bottom side)	Cold plate on exposed pad, according to JESD51-121	5.9	°C/W
R <sub>thJB</sub>	Junction-to-board thermal resistance	according to JESD51-81	13.6	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization	According to JESD51-2a1	1	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization	According to JESD51-2a1	13.7	°C/W

1. Simulated on a 76.2 x 114.3 x 1.6 mm, with vias underneath the component, 2s2p board as per standard Jedec (JESD51-7) in natural convection.

## 2.4 ESD protection ratings

**Table 4. ESD protection ratings**

Symbol	Parameter	Conditions	Class	Value	Unit
HBM	Human body model	Conforming to ANSI/ESDA/JEDEC JS001	H2	2	kV
CDM	Charge device model	Conforming to ANSI/ESDA/JEDEC JS002 All pins	C2a	500	V
		Conforming to ANSI/ESDA/JEDEC JS002 Corner pins only (1, 6, 7, 12, 13, 18, 19, 24)	-	750	V
MM	Machine model	Conforming to EIA/JESD22-A115-C	NC	200	V

### 3 Electrical characteristics

Testing conditions:  $V_S = 36\text{ V}$ ,  $T_j = 25\text{ °C}$  unless otherwise specified.

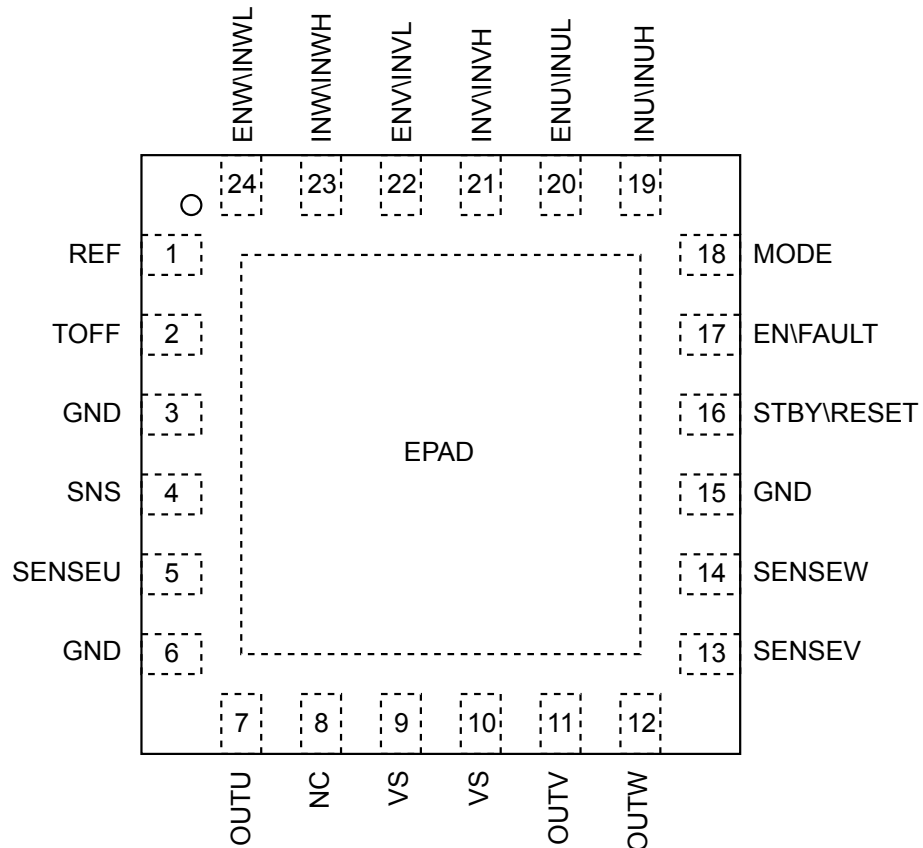
**Table 5. Electrical characteristics**

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
<b>General</b>						
$V_{Sth(ON)}$	$V_S$ turn-on threshold	$V_S$ rising from 0 V		6.0	6.5	V
$V_{Sth(HYST)}$	$V_S$ turn-off threshold hysteresis	$V_S$ falling from 7 V		0.4		V
$I_S$	$V_S$ supply current	No commutations EN = '0' $R_{TOFF} = 10\text{ k}\Omega$		2.3	2.7	mA
		No commutations EN = '1' $R_{TOFF} = 10\text{ k}\Omega$		2.7	3	mA
$V_{STBYL}$	Standby low voltage				0.8	V
$V_{STBYH}$	Standby high voltage		2			V
$I_{S, STBY}$	$V_S$ supply standby current	STBY = 0 V			45	$\mu\text{A}$
<b>Power stage</b>						
$R_{DSon HS+LS}$	Total on resistance HS + LS	$V_S = 21\text{ V}$ $I_{OUT} = 1\text{ A}$		1	1.3	$\Omega$
		$V_S = 21\text{ V}$ $I_{OUT} = 1\text{ A}$ $T_j = 150\text{ °C}^{(1)}$		1.4	1.6	
$I_{DSS}$	Output leakage current	OUTx = $V_S = 48\text{ V}$			20	$\mu\text{A}$
		OUTx = -0.3 V	-1			
$V_{DF}$	Freewheeling diode forward voltage	$I_D = \text{TBD A}$		1		V
$t_{rise}$	Rise time	$V_S = 21\text{ V}$		120		ns
$t_{fall}$	Fall time	$V_S = 21\text{ V}$		60		ns
<b>Logic IO</b>						
$V_{IH}$	High logic level input voltage		2			V
$V_{IL}$	Low logic level input voltage				0.8	V
$V_{OL}$	Low logic level output voltage	$I_{OL} = 4\text{ mA}$			0.3	V
$V_{RELEASE}$	FAULT open-drain release voltage				0.6	V
$R_{STBY}$	STBY pull-down resistance			60		k $\Omega$
$I_{PDEN}$	Enable pull-down current			5		$\mu\text{A}$
$t_{END}$	EN input propagation delay	From EN falling edge to OUT high impedance		400		ns
$t_{IND(ON)}$	Turn-on propagation delay	From INxH rising edge to 10% of OUTx		450		ns

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
$t_{IND(OFF)}$	Turn-off propagation delay	From INxL rising edge to 90% of OUTx		250		ns
<b>PWM current control</b>						
$V_{SNS,OFFSET}$	Current control offset		-15		15	mV
$t_{OFF}$	Total OFF time	$R_{OFF} = 10\text{ k}\Omega$		13		$\mu\text{s}$
		$R_{OFF} = 160\text{ k}\Omega$		146		$\mu\text{s}$
$\Delta t_{OFF}$	OFF time precision	Full temperature range <sup>(1)</sup>	20%		+20%	%
$t_{OFF,jitter}$	Total OFF time jittering			$\pm 2\%$		
<b>Protections</b>						
$T_{jSD}$	Thermal shutdown threshold			160		$^{\circ}\text{C}$
$T_{jSD,Hyst}$	Thermal shutdown hysteresis			40		$^{\circ}\text{C}$
$I_{OC}$	Overcurrent threshold			3	3.5	A

1. Based on characterization data on a limited number of samples, not tested during production.

## 4 Pin description

**Figure 2. Pin connection (top view)**


*Note:* the exposed pad must be connected to ground.

**Table 6. Pin description**

N.	Name	Type	Function
1	REF	Analog input	Reference voltage for the PWM current control circuitry
2	TOFF	Analog input	Internal oscillator frequency adjustment
3, 6, 15	GND	Ground	Device ground
4	SNS	Analog input	Current limiter sense input
5	SENSEU	Power output	Sense output of the bridge U
7	OUTU	Power output	Power bridge output U
9	VS	Supply	Device supply voltage
10	VS	Supply	Device supply voltage
11	OUTV	Power output	Power bridge output V
12	OUTW	Power output	Power bridge output W
13	SENSEV	Power output	Sense output of the bridge V
14	SENSEW	Power output	Sense output of the bridge W

N.	Name	Type	Function
16	STBY\RESET	Logic input	Standby\Reset input When forced low the device enters in low consumption mode
17	EN\FAULT	Logic input\ Open drain output	Logic input 5 V compliant with open drain output. This is the power stage input enable (when low, the power stage is turned off) and is forced low through the integrated open-drain MOSFET when a failure occurs
18	MODE	Logic input	Inputs driving method selection. When low the ENx\INx option is selected, when high the INxH\INxL option is enabled
19	INU\INUH	Logic input	Output U high-side driving input <sup>(1)</sup>
20	ENU\INUL	Logic input	Output U low-side driving input <sup>(1)</sup>
21	INV\INVH	Logic input	Output V high-side driving input <sup>(1)</sup>
22	ENV\INVL	Logic input	Output V low-side driving input <sup>(1)</sup>
23	INW\INWH	Logic input	Output W high-side driving input <sup>(1)</sup>
24	ENW\INWL	Logic input	Output W low-side driving input <sup>(1)</sup>
8	NC	NC	Not connected.

1. Refer to :[Section 5.2 Logic inputs](#) for more details



## 5 Functional description

The STSPIN830 is a 3-phase motor driver integrating a PWM current limiter and a power stage composed by three fully-protected half-bridges.

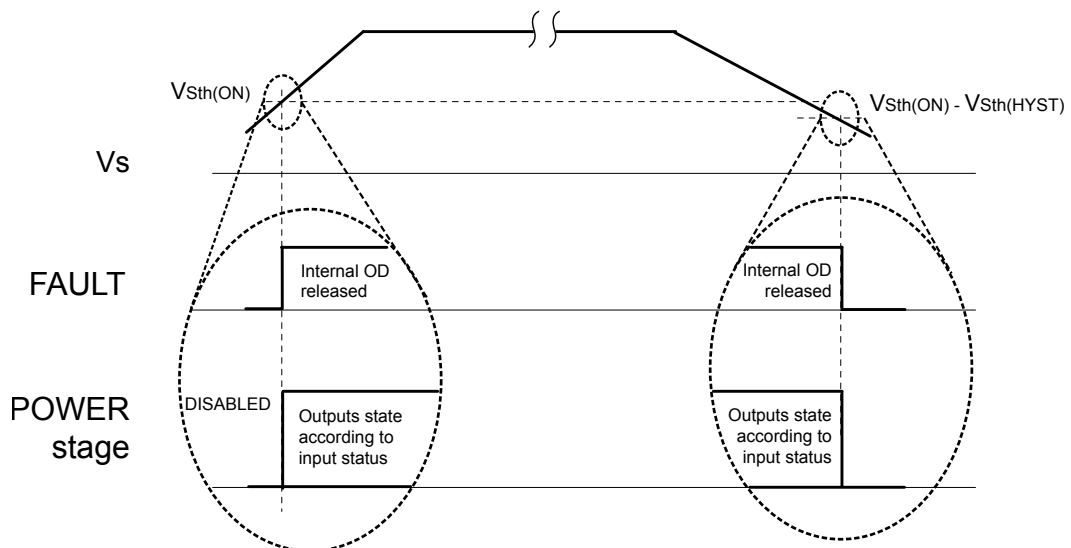
### 5.1 Power supply and standby

The device is supplied through the VS pins, the two pins **must** be at the same voltage.

At power-up the power stage is disabled and the FAULT pin is forced low until the VS voltage rise above the  $V_{Sth(ON)}$  threshold.

If the  $V_S$  fall below the  $V_{Sth(ON)} - V_{Sth(HYST)}$  value the power stage is immediately disabled and the FAULT pins are forced low.

Figure 3. UVLO protection management



The device provides a low consumption mode which is set forcing the STBY\RESET input below the  $V_{STBYL}$  threshold.

When the device is in standby status the power stage is disabled (outputs are in high impedance) and the supply to the integrated control circuitry is strongly reduced. When the device leaves the standby status, all the control circuitry is reset at power-up condition.

### 5.2 Logic inputs

The STSPIN830 offers two alternative method to drive the power stage, the proper can be selected setting the status of MODE pin.

If MODE pin is set low (connected to GND) the output of each half bridge is controlled by the respective ENx and INx inputs.

If MODE pin is set high the output of each half bridge is controlled by the respective INxH and INxL inputs.

In both cases the status of the power bridge is also determined by the PWM current limiter as indicated in [Section 5.3 PWM current limiter](#).

**Note:** The MODE pin status must not be changed during device working.

When the EN\FAULT input is forced low the power stage is immediately disabled (all MOSFETs are turned off). The pin is also used as FAULT indication through the integrated open-drain MOSFET as described in paragraph [Section 5.4 Device protections](#) and [Section 5.5 ESD protection strategy](#).

**Table 7. ENx and INx inputs truth table (MODE = 'L')**

MODE	EN\FAULT	ENx	INx	OUTx	'x' Half-bridge condition
0	0	X <sup>(1)</sup>	X <sup>(1)</sup>	High Z <sup>(2)</sup>	Disabled
0	1	0	X <sup>(1)</sup>	High Z <sup>(2)</sup>	Disabled
0	1	1	0	GND	LS on
0	1	1	1	V <sub>S</sub>	HS on

1. X: don't care.
2. High Z: high impedance

**Table 8. INxL and INxH inputs truth table (MODE = 'H')**

MODE	EN\FAULT	INxH	INxL	OUTx	'x' Half-bridge condition
1	0	X <sup>(1)</sup>	X <sup>(1)</sup>	High Z <sup>(2)</sup>	Disabled
1	1	0	0	High Z <sup>(2)</sup>	Disabled
1	1	0	1	GND	LS on
1	1	1	0	V <sub>S</sub>	HS on
1	1	1	1	High Z <sup>(2)</sup>	Disabled (interlocking)

1. X: don't care.

### 5.3 PWM current limiter

The device implements a PWM current limiter.

The load current is sensed through the SNS pin monitoring the voltage drop across an external resistor connected between the source of the low side power MOSFET (SENSE<sub>x</sub> pins) and ground.

The voltage of the sense pin (V<sub>SNS</sub>) is compared to the reference voltage pin (V<sub>REF</sub>).

When V<sub>SNS</sub> > V<sub>REF</sub> the internal comparator is triggered, the OFF time counter is started and all the power outputs are disabled (high impedance) until the end of count of the timer.

During current decays the inputs values are ignored until the system returns to ON condition (decay time expired).

The reference voltage value, V<sub>REF</sub>, has to be selected according the load current target value (peak value) and sense resistors value.

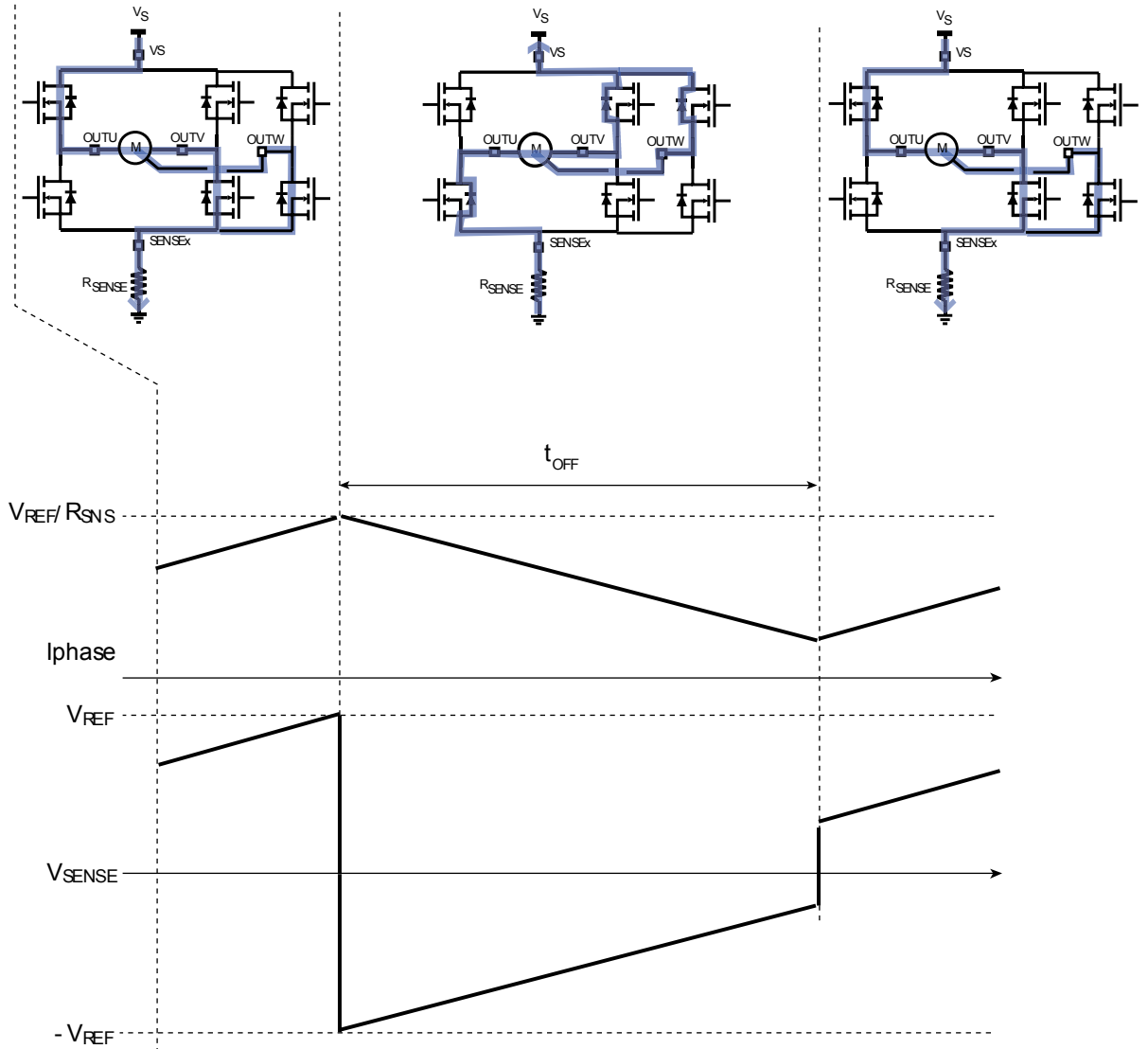
#### Equation 1

$$V_{REF} = R_{SENSE} \times I_{LOAD, peak} \quad (1)$$

The choice of sense resistors value must be take into account two main issues:

- The sensing resistor dissipates energy and provides dangerous negative voltages on the SENSE pins during the current recirculation. For this reason the resistance of this component should be kept low (using multiple resistors in parallel will help obtaining the required power rating with standard resistors).
- The lower is the R<sub>SENSE</sub> value, the higher is the peak current error due to noise on V<sub>REF</sub> pin and to the input offset of the current sense comparator: too small values of R<sub>SENSE</sub> must be avoided.

Figure 4. PWM current limit sequence example



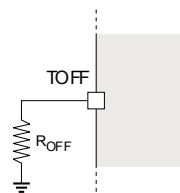
AM040382

Note: When the voltage on the SNS pin exceeds the absolute ratings, fault condition is triggered and the ENFAULT output is forced low.

**TOFF adjustment**

The OFF time is adjusted through an external resistor connected between the TOFF pin and ground as shown in Figure 5. OFF time regulation circuit .

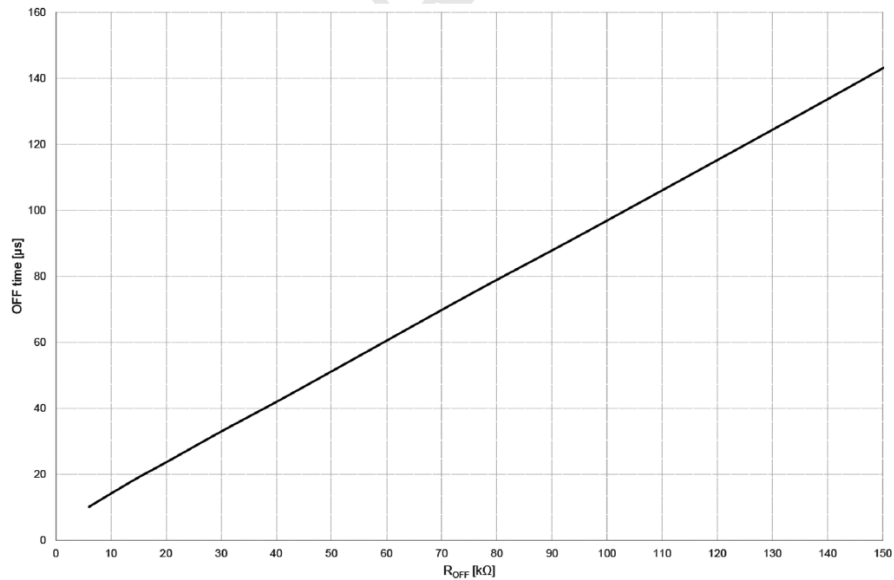
Figure 5. OFF time regulation circuit



AM040383

The relation between the OFF time and the external resistor value is shown in the graph of [Figure 6. OFF time vs ROFF value](#). The value typically ranges from 10  $\mu\text{s}$  to 150  $\mu\text{s}$ . The recommended value for  $R_{\text{OFF}}$  is in the range between 5 k $\Omega$  k $\Omega$

**Figure 6. OFF time vs ROFF value**



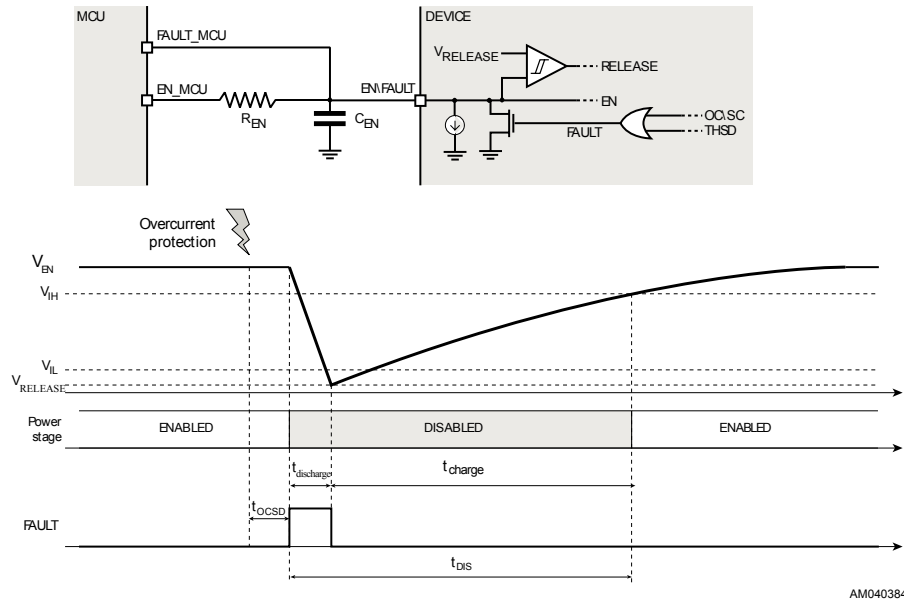
## 5.4 Device protections

### 5.4.1 Overcurrent and short circuit protections

The device embeds a circuitry protecting each power MOSFET against the over load and short circuit conditions (short to ground, short to VS and short between outputs).

When the overcurrent or the short circuit protection is triggered the power stage is disabled and the EN\FAULT input is forced low through the integrated open drain MOSFET discharging the external  $C_{\text{EN}}$  capacitor.

The power stage is kept disabled and the open drain MOSFET is kept ON until the EN\FAULT input falls below the  $V_{\text{RELEASE}}$  threshold, then the  $C_{\text{EN}}$  capacitor is charged through the external  $R_{\text{EN}}$  resistor.

**Figure 7. Overcurrent and short-circuit protections management**


The total disable time after an overcurrent event is set sizing properly the external network connected to EN \FAULT pin (refer to [Figure 8. Disable time versus R<sub>EN</sub> and C<sub>EN</sub> values \(V<sub>DD</sub> = 3.3 V\)](#) ) and it is the sum of the discharging and charging time of the C<sub>EN</sub> capacitor:

**Equation 2**

$$t_{DIS} = t_{discharge} + t_{charge} \quad (2)$$

Considering  $t_{discharge}$  is normally significantly lower than  $t_{charge}$ , its contribution is negligible and the disable time is almost equal to  $t_{charge}$  only:

**Equation 3**

$$t_{DIS} \cong R_{EN} \times C_{EN} \times \ln \frac{(V_{DD} - R_{EN} \times I_{PD}) - V_{RELEASE}}{(V_{DD} - R_{EN} \times I_{PD}) - V_{IH}} \quad (3)$$

Where V<sub>DD</sub> is the pull-up voltage of R<sub>EN</sub> resistor.

The recommended value for R<sub>EN</sub> and C<sub>EN</sub> are respectively 39 kΩ and 10 nF that allow obtaining 200 μs disable time.

Figure 8. Disable time versus REN and CEN values (VDD = 3.3 V)

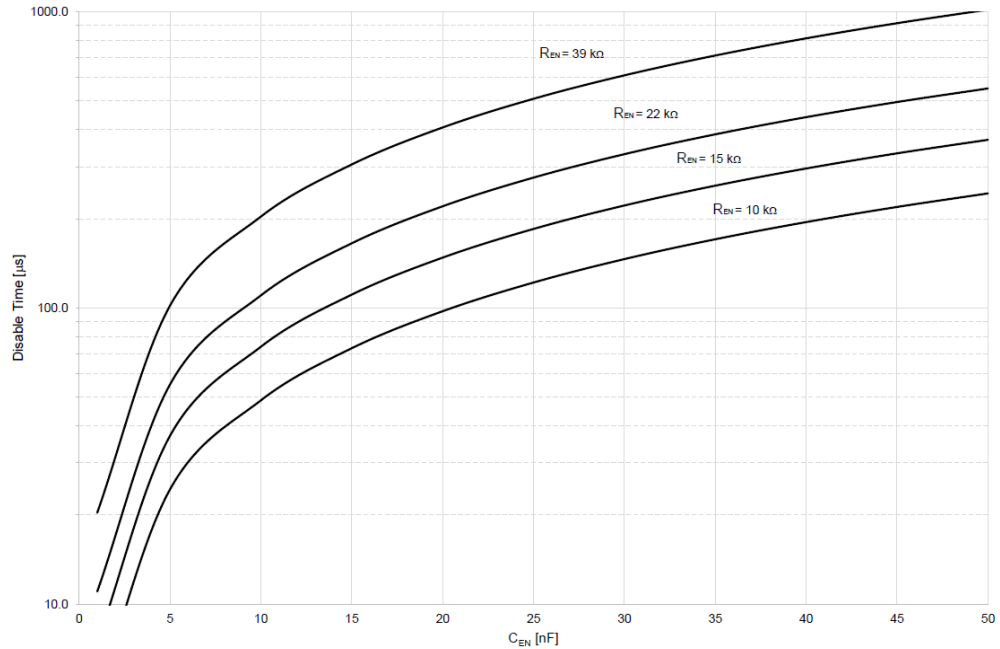
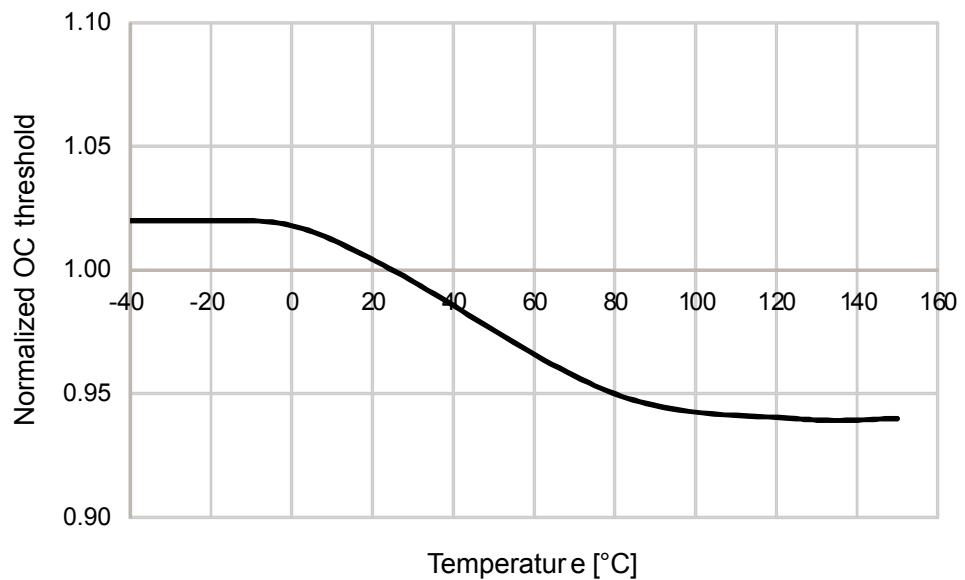


Figure 9. Overcurrent threshold versus temperature (normalized at 25 °C)



AM040385

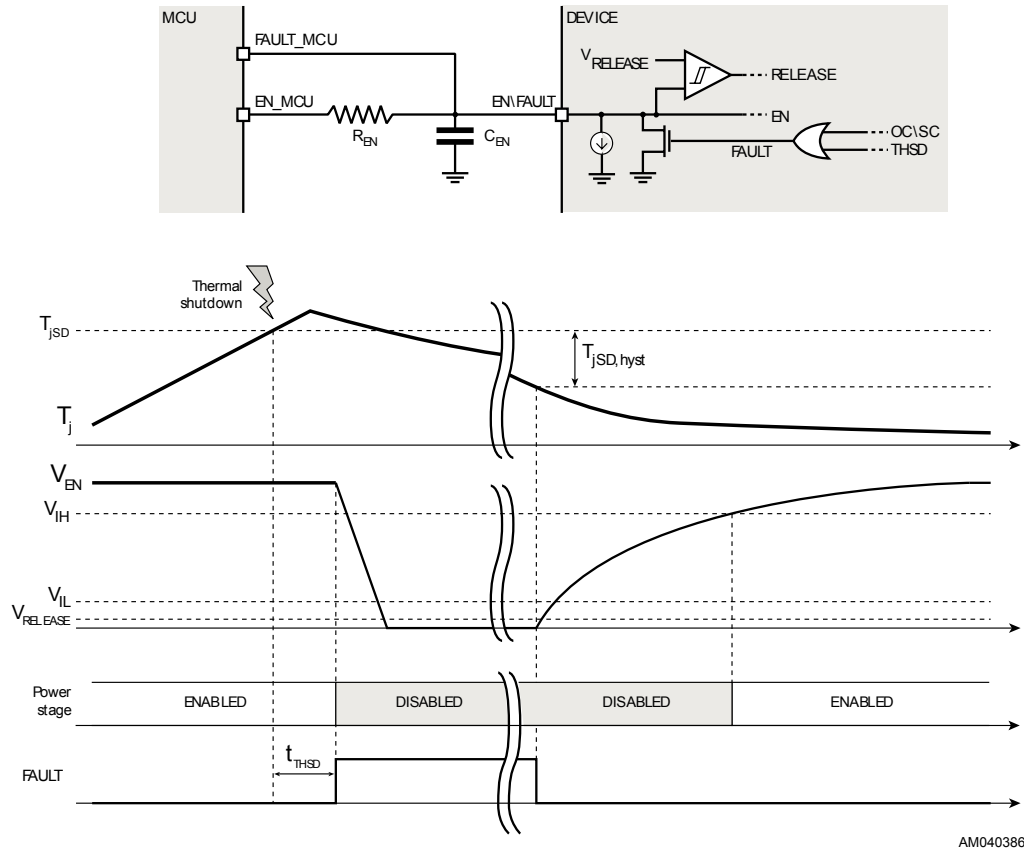
#### 5.4.2 Thermal shutdown

The device embeds a circuitry protecting it from the overtemperature condition.

When the thermal shutdown temperature is reached the power bridges are disabled and the ENFAULT input is forced low through the integrated open drain MOSFET (refer to [Figure 10. Thermal shutdown management](#)).

The protection and the ENFAULT output are released when the IC temperature returns below a safe operating value ( $T_{jSD} - T_{jSD,Hyst}$ ).

Figure 10. Thermal shutdown management



AM040386

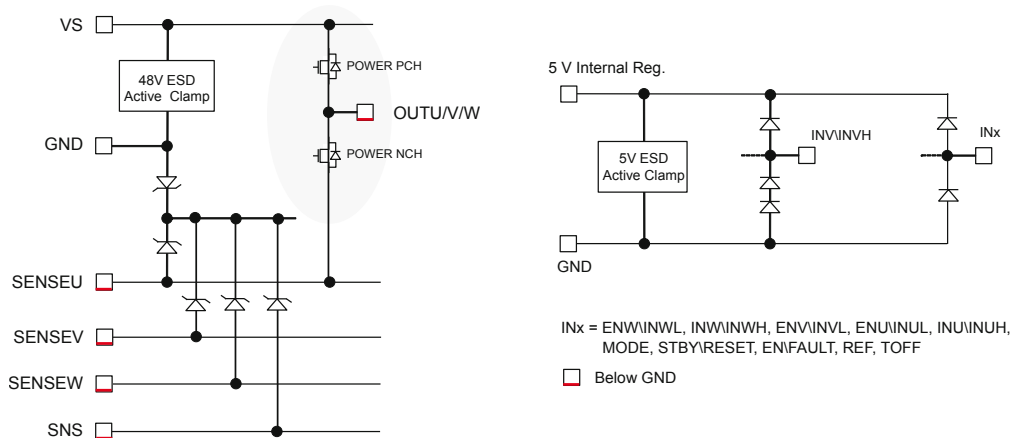
### 5.4.3 Blanking time

The device provides a blanking time  $t_{BLANK}$  after each power MOSFET commutation to prevent false triggering of protections and current limiter.

During blanking time the protections (overcurrent, short circuit, thermal shutdown) and the comparator of the current limiter are inhibit.

## 5.5 ESD protection strategy

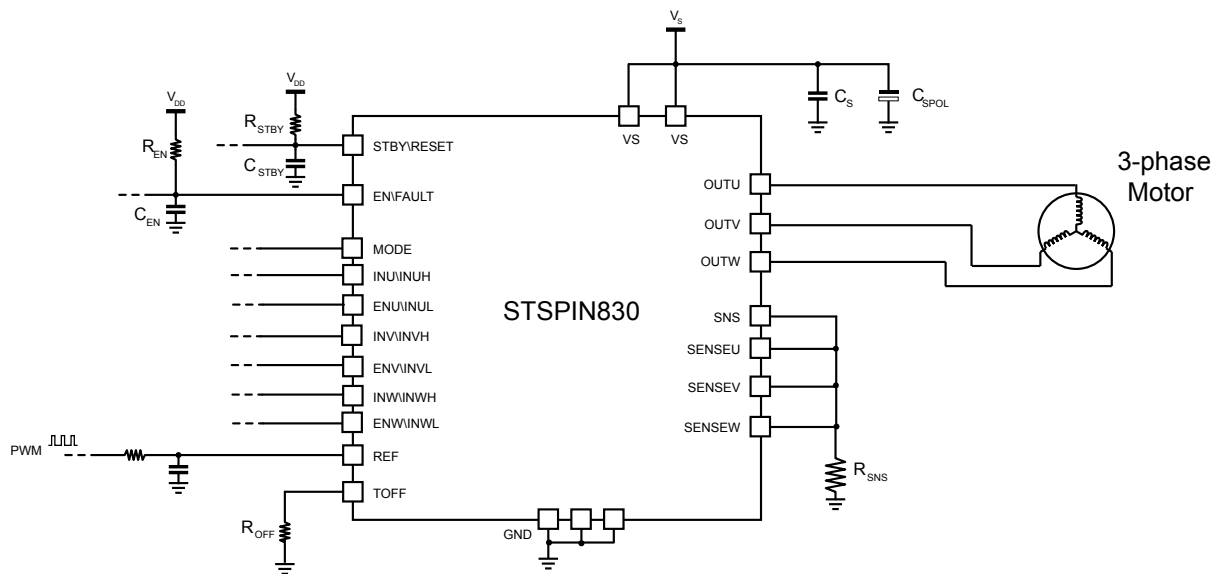
Figure 11. ESD protection strategy



## 6 Typical applications

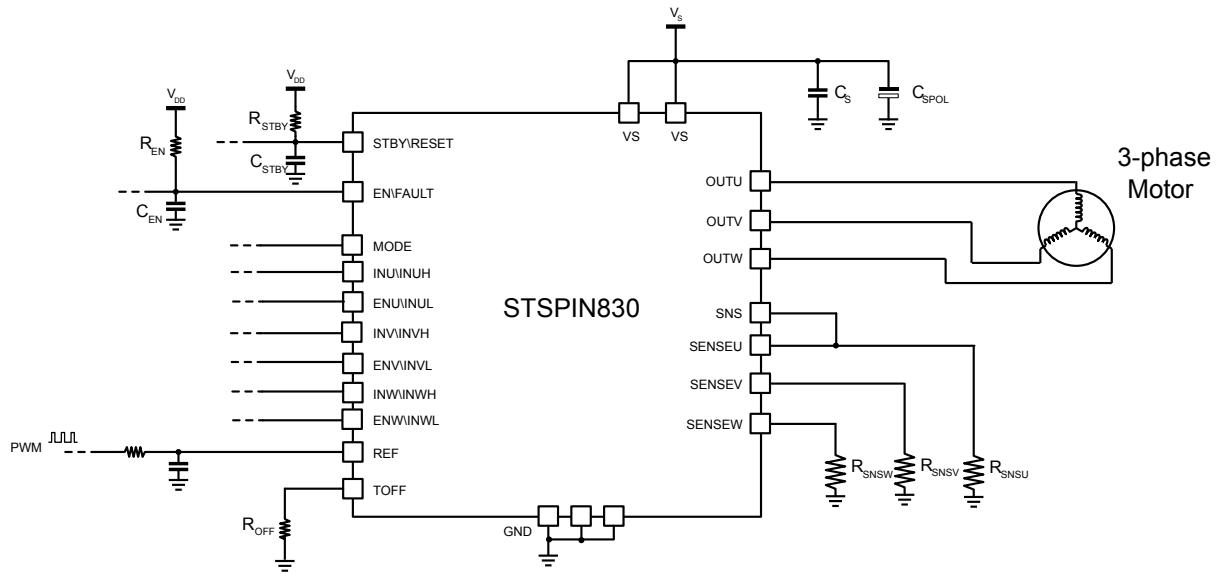
**Table 9. Typical application values**

Name	Value
$C_S$	330 nF
$C_{SPOL}$	33 $\mu$ F
$R_{SNS}$	330 m $\Omega$ / 1W
$C_{EN}$	10 nF
$R_{EN}$	39 k $\Omega$
$C_{STBY}$	1 nF
$R_{STBY}$	18 k $\Omega$
$R_{OFF}$	10 k $\Omega$ ( $T_{OFF} \square 13 \mu$ s)

**Figure 12. Typical application schematic with single shunt**




**Figure 13. Typical application schematic with triple shunt**



## 7 Layout recommendations

The integrates the power stage; in order to improve the thermal dissipation, the exposed pad must be connected to the ground plane on the bottom layer using multiple vias equally spaced. This ground plane acts as a heatsink, for this reason it should be as wide as possible.

The voltage supply VS must be stabilized and filtered with a ceramic bypass capacitor, typically 330nF. It must be placed on the same side and as close as possible to VS pin in order to reject high frequency noise components on the supply. A bulk capacitor could also be required (typically a 33  $\mu$ F). The connection between the power supply connector and the VS pins must be as short as possible using wide traces.

In order to ensure the best ground connection between the and the other components, a GND plane surrounding the device is recommended.

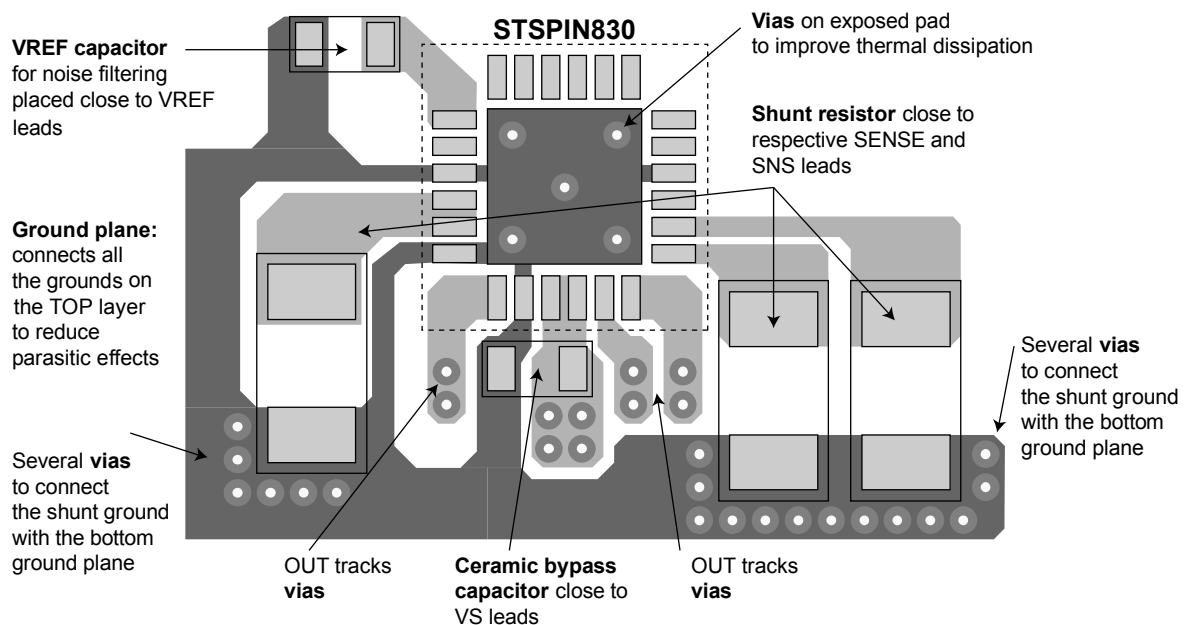
A capacitor between REF pins and ground should be positioned as near as possible to the device in order to filter the noise and stabilize the reference voltage.

Several vias should be positioned as near as possible each sense resistor connecting them to the ground plane on the bottom layer. In this way, both the GND planes provide a path for the current flowing into the power stage.

The path between the ground of the shunt resistors and the ceramic bypass capacitor of the device is critical; for this reason it must be as short as possible minimizing parasitic inductances that can cause voltage spikes on SENSE and OUT pins.

The OUT pins and the VS nets can be routed using the bottom layer, it is recommended to use two vias for output connections.

Figure 14. PCB layout example with triple shunt (top layer)

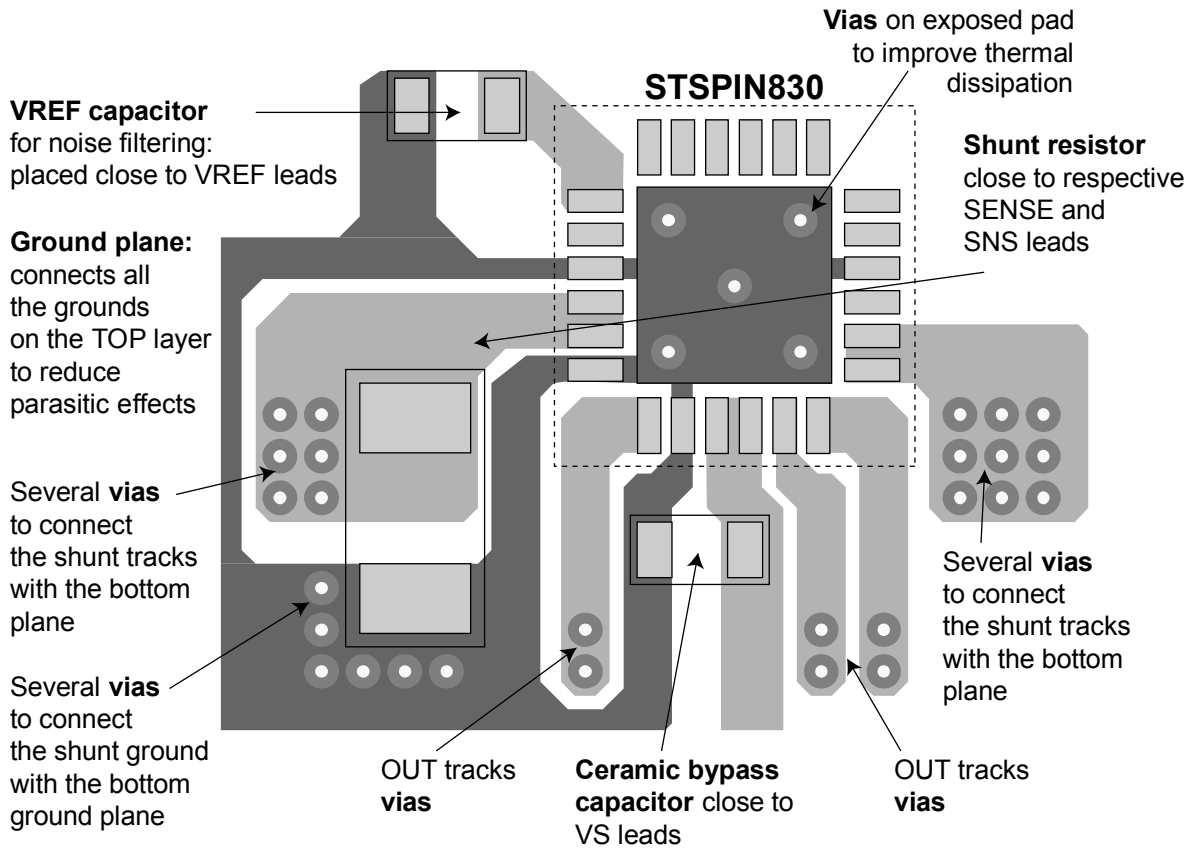


AM040390

In case of single shunt configuration take special care for the SENSE and SNS pins connection.

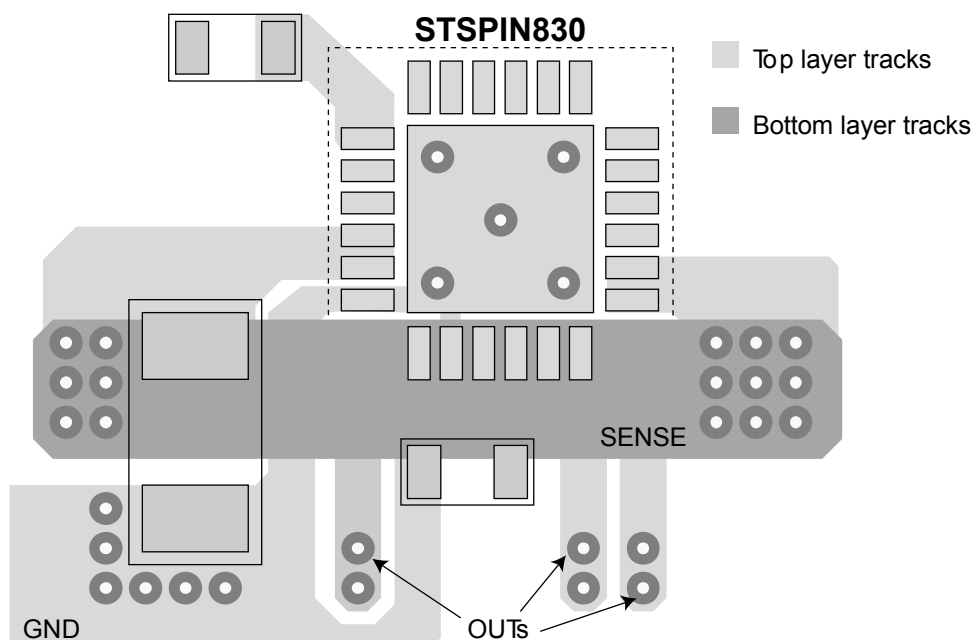
As suggested in the [Figure 15. PCB layout example with single shunt \(top layer\)](#) and [Figure 16. PCB layout example with single shunt \(bottom layer\)](#), the shunt resistor can be placed in the top layer close to SENSEU and SNS pins with a wide copper area and vias. The connection with other sense pins (SENSEV and SENSEW) can be routed in the bottom layer taking care to maximize the track area and add more vias near to the pins.

**Figure 15. PCB layout example with single shunt (top layer)**



AM040391

**Figure 16. PCB layout example with single shunt (bottom layer)**



AM040392

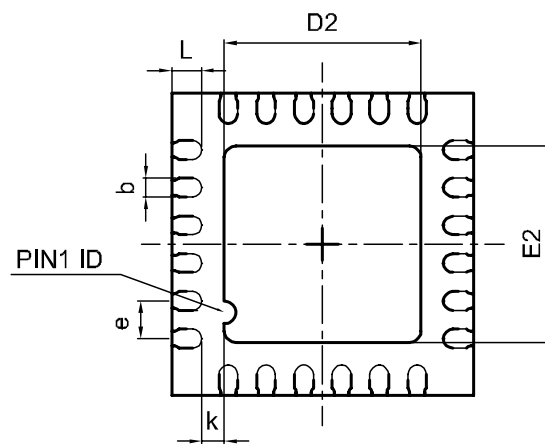
## 8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

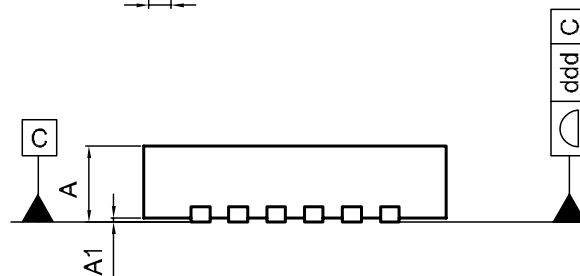
### 8.1 TFQFPN 4x4x1.05 24L package information

Figure 17. TFQFPN 4 x 4 x 1.05 - 24L package outline

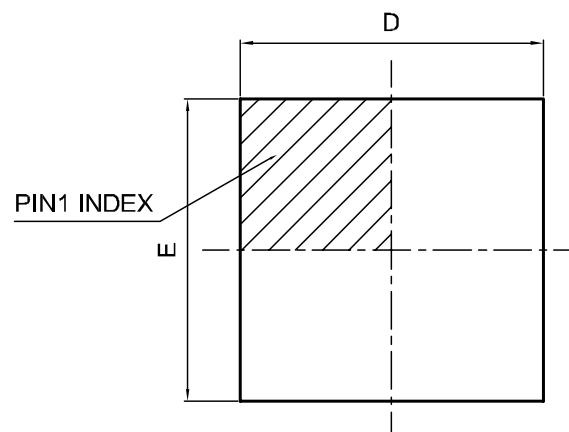
BOTTOM VIEW



SIDE VIEW



TOP VIEW



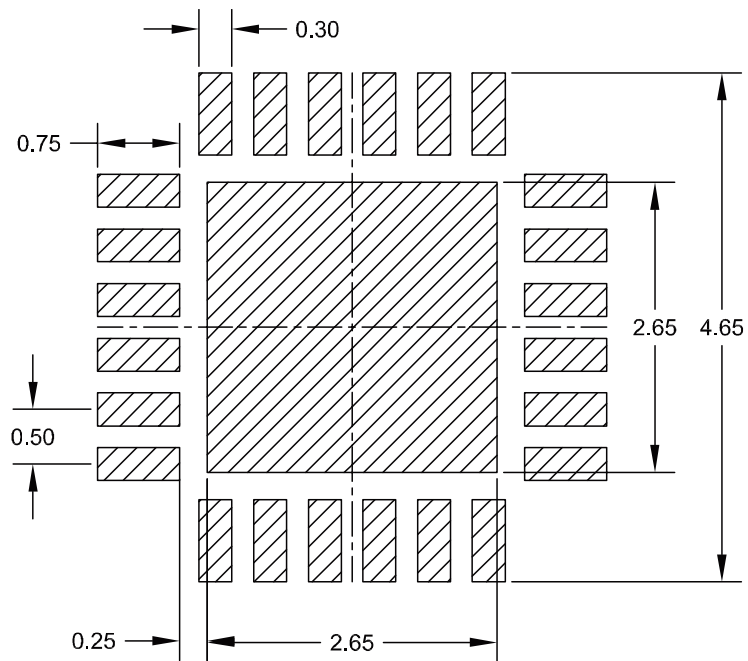
TFQFPN-4x4x1.05-24

Table 10. TFQFPN 4x4x1.05 24L package mechanical data

Symbol	Dimensions (mm)			NOTES
	Min.	Typ.	Max.	
A	0.90	1.00	1.10	
A1	0.00	0.02	0.05	
b	0.20	0.25	0.30	(1)
D	3.90	4.00	4.10	
D2	2.55	2.60	2.65	
E	3.90	4.00	4.10	
E2	2.55	2.60	2.65	
e		0.50		
L	0.35	0.40	0.45	
k		0.30		
ddd		0.05		

Dimension "b" does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum "b" dimension by more than 0.08 mm

Figure 18. TFQFPN 4 x 4 x 1.05 - 24L suggested footprint



TFQFPN 4 x 4 x 1.05 - 24 L

## 9 Ordering information

**Table 11. Ordering information**

Order code	Package	Packing
STSPIN830	TFQFPN 4 x 4 x 1.05 - 24L	Tape and reel

## Revision history

**Table 12. Document revision history**

Date	Version	Changes
18-May-2018	1	Initial release.
02 Aug-2019	2	Some minor text changes inside the document, cover image updated, updated <a href="#">Table 2. Recommended operating conditions</a>

## Contents

<b>1</b>	<b>Block diagram</b> .....	<b>2</b>
<b>2</b>	<b>Electrical data</b> .....	<b>3</b>
2.1	Absolute maximum ratings .....	3
2.2	Recommended operating conditions .....	3
2.3	Thermal data .....	3
2.4	ESD protection ratings .....	4
<b>3</b>	<b>Electrical characteristics</b> .....	<b>5</b>
<b>4</b>	<b>Pin description</b> .....	<b>7</b>
<b>5</b>	<b>Functional description</b> .....	<b>9</b>
5.1	Power supply and standby .....	9
5.2	Logic inputs .....	9
5.3	PWM current limiter .....	10
5.4	Device protections .....	12
5.4.1	Overcurrent and short circuit protections .....	12
5.4.2	Thermal shutdown .....	14
5.4.3	Blanking time .....	15
5.5	ESD protection strategy .....	15
<b>6</b>	<b>Typical applications</b> .....	<b>16</b>
<b>7</b>	<b>Layout recommendations</b> .....	<b>18</b>
<b>8</b>	<b>Package information</b> .....	<b>20</b>
8.1	[Package name] package information .....	20
<b>9</b>	<b>Ordering information</b> .....	<b>22</b>
	<b>Revision history</b> .....	<b>23</b>
	<b>Contents</b> .....	<b>24</b>
	<b>List of tables</b> .....	<b>25</b>
	<b>List of figures</b> .....	<b>26</b>



## List of tables

<b>Table 1.</b>	Absolute maximum ratings . . . . .	3
<b>Table 2.</b>	Recommended operating conditions . . . . .	3
<b>Table 3.</b>	Thermal data . . . . .	3
<b>Table 4.</b>	ESD protection ratings . . . . .	4
<b>Table 5.</b>	Electrical characteristics . . . . .	5
<b>Table 6.</b>	Pin description . . . . .	7
<b>Table 7.</b>	ENx and INx inputs truth table (MODE = 'L') . . . . .	10
<b>Table 8.</b>	INxL and INxH inputs truth table (MODE = 'H') . . . . .	10
<b>Table 9.</b>	Typical application values . . . . .	16
<b>Table 10.</b>	TFQFPN 4x4x1.05 24L package mechanical data . . . . .	21
<b>Table 11.</b>	Ordering information . . . . .	22
<b>Table 12.</b>	Document revision history . . . . .	23

## List of figures

<b>Figure 1.</b>	STSPIN830 block diagram . . . . .	2
<b>Figure 2.</b>	Pin connection (top view) . . . . .	7
<b>Figure 3.</b>	UVLO protection management . . . . .	9
<b>Figure 4.</b>	PWM current limit sequence example . . . . .	11
<b>Figure 5.</b>	OFF time regulation circuit . . . . .	11
<b>Figure 6.</b>	OFF time vs ROFF value . . . . .	12
<b>Figure 7.</b>	Overcurrent and short-circuit protections management . . . . .	13
<b>Figure 8.</b>	Disable time versus REN and CEN values (VDD = 3.3 V). . . . .	14
<b>Figure 9.</b>	Overcurrent threshold versus temperature (normalized at 25 °C). . . . .	14
<b>Figure 10.</b>	Thermal shutdown management . . . . .	15
<b>Figure 11.</b>	ESD protection strategy . . . . .	15
<b>Figure 12.</b>	Typical application schematic with single shunt . . . . .	16
<b>Figure 13.</b>	Typical application schematic with triple shunt . . . . .	17
<b>Figure 14.</b>	PCB layout example with triple shunt (top layer) . . . . .	18
<b>Figure 15.</b>	PCB layout example with single shunt (top layer) . . . . .	19
<b>Figure 16.</b>	PCB layout example with single shunt (bottom layer) . . . . .	19
<b>Figure 17.</b>	TFQFPN 4 x 4 x 1.05 - 24L package outline . . . . .	20
<b>Figure 18.</b>	TFQFPN 4 x 4 x 1.05 - 24L suggested footprint . . . . .	21

**IMPORTANT NOTICE – PLEASE READ CAREFULLY**

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, please refer to [www.st.com/trademarks](http://www.st.com/trademarks). All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2019 STMicroelectronics – All rights reserved