

N-Channel Reduced Q_g , Fast Switching MOSFET

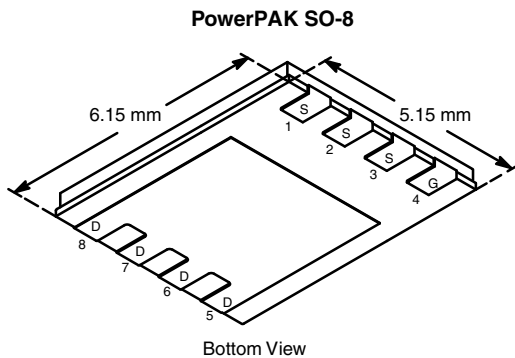
| PRODUCT SUMMARY | | |
|-----------------|-----------------------------|-----------|
| V_{DS} (V) | $R_{DS(on)}$ (Ω) | I_D (A) |
| 30 | 0.00975 at $V_{GS} = 10$ V | 15 |
| | 0.01375 at $V_{GS} = 4.5$ V | 13 |

FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- Extremely Low Q_{gd} for Low Switching Losses
- TrenchFET[®] Power MOSFET
- New Low Thermal Resistance PowerPAK[®] Package with Low 1.07 mm Profile
- 100 % R_g Tested
- 100 % UIS Tested
- Complaint to RoHS Directive 2002/95/EC



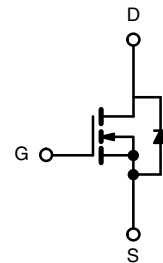
Available
RoHS*
COMPLIANT
HALOGEN FREE
Available



Ordering Information: Si7392DP-T1-E3 (Lead (Pb)-free)
Si7392DP-T1-GE3 (Lead (Pb)-free and Halogen-free)

APPLICATIONS

- High-Side DC/DC Conversion
 - Notebook
 - Server



N-Channel MOSFET

| ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted) | | | | | |
|---|----------------|---------------|--------------|------|----|
| Parameter | Symbol | 10 s | Steady State | Unit | |
| Drain-Source Voltage | V_{DS} | 30 | | V | |
| Gate-Source Voltage | V_{GS} | ± 20 | | | |
| Continuous Drain Current ($T_J = 150$ °C) ^a | I_D | $T_A = 25$ °C | 15 | 9 | A |
| | | $T_A = 70$ °C | 12 | 7 | |
| Pulsed Drain Current | I_{DM} | ± 50 | | | |
| Continuous Source Current (Diode Conduction) ^a | I_S | 4.1 | 1.5 | | |
| Avalanche Current | I_{AS} | L = 0.1 mH | 30 | | mJ |
| Single-Pulse Avalanche Energy | | | E_{AS} | 45 | |
| Maximum Power Dissipation ^a | P_D | $T_A = 25$ °C | 5 | 1.8 | W |
| | | $T_A = 70$ °C | 3.2 | 1.1 | |
| Operating Junction and Storage Temperature Range | T_J, T_{stg} | - 55 to 150 | | °C | |
| Soldering Recommendations (Peak Temperature) ^{b, c} | | 260 | | | |

| THERMAL RESISTANCE RATINGS | | | | | |
|---|------------|---------------|---------|------|------|
| Parameter | Symbol | Typical | Maximum | Unit | |
| Maximum Junction-to-Ambient (MOSFET) ^a | R_{thJA} | $t \leq 10$ s | 20 | 25 | °C/W |
| | | Steady State | 53 | 70 | |
| Maximum Junction-to-Case (Drain) | R_{thJC} | 3.5 | 4.5 | | |

Notes:

a. Surface mounted on 1" x 1" FR4 board.

b. See solder profile (www.vishay.com/ppg?73257). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

c. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.

* Pb containing terminations are not RoHS compliant, exemptions may apply.

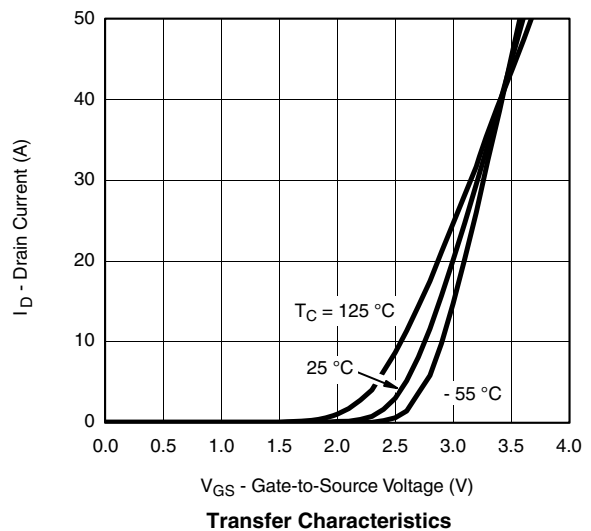
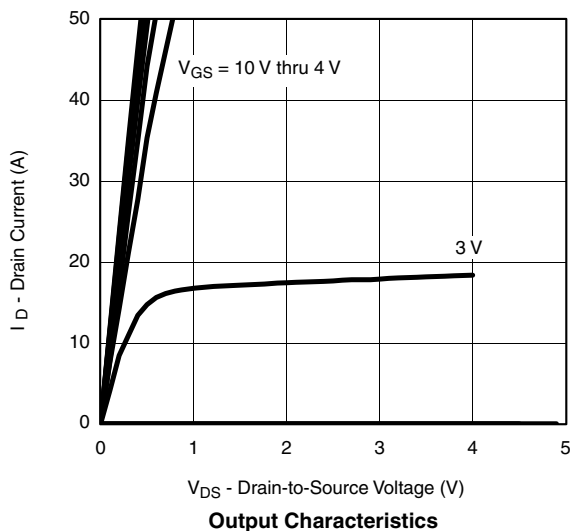
| MOSFET SPECIFICATIONS (T _J = 25 °C, unless otherwise noted) | | | | | | |
|--|---------------------|--|------|-------|---------|------|
| Parameter | Symbol | Test Conditions | Min. | Typ. | Max. | Unit |
| Static | | | | | | |
| Gate Threshold Voltage | V _{GS(th)} | V _{DS} = V _{GS} , I _D = 250 μA | 1.0 | | 3.0 | V |
| Gate-Body Leakage | I _{GSS} | V _{DS} = 0 V, V _{GS} = ± 20 V | | | ± 100 | nA |
| Zero Gate Voltage Drain Current | I _{DSS} | V _{DS} = 30 V, V _{GS} = 0 V | | | 1 | μA |
| | | V _{DS} = 30 V, V _{GS} = 0 V, T _J = 70 °C | | | 5 | |
| On-State Drain Current ^a | I _{D(on)} | V _{DS} ≥ 5 V, V _{GS} = 10 V | 40 | | | A |
| Drain-Source On-State Resistance ^a | R _{DS(on)} | V _{GS} = 10 V, I _D = 15 A | | 0.008 | 0.00975 | Ω |
| | | V _{GS} = 4.5 V, I _D = 13 A | | 0.011 | 0.01375 | |
| Forward Transconductance ^a | g _{fs} | V _{DS} = 15 V, I _D = 15 A | | 40 | | S |
| Diode Forward Voltage ^a | V _{SD} | I _S = 4.1 A, V _{GS} = 0 V | | 0.75 | 1.1 | V |
| Dynamic^b | | | | | | |
| Total Gate Charge | Q _g | V _{DS} = 15 V, V _{GS} = 4.5 V, I _D = 15 A | | 10 | 15 | nC |
| Gate-Source Charge | Q _{gs} | | | 3.5 | | |
| Gate-Drain Charge | Q _{gd} | | | 2.6 | | |
| Gate Resistance | R _g | | | 1.6 | 2.7 | Ω |
| Turn-On Delay Time | t _{d(on)} | V _{DD} = 15 V, R _L = 15 Ω I _D ≅ 1 A, V _{GEN} = 10 V, R _g = 6 Ω | | 15 | 25 | ns |
| Rise Time | t _r | | | 7 | 15 | |
| Turn-Off Delay Time | t _{d(off)} | | | 46 | 70 | |
| Fall Time | t _f | | | 9 | 17 | |
| Source-Drain Reverse Recovery Time | t _{rr} | I _F = 2.7 A, di/dt = 100 A/μs | | 30 | 60 | |

Notes:

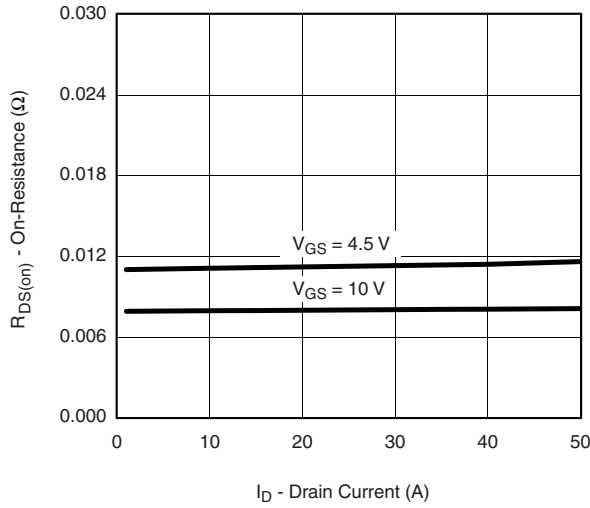
- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

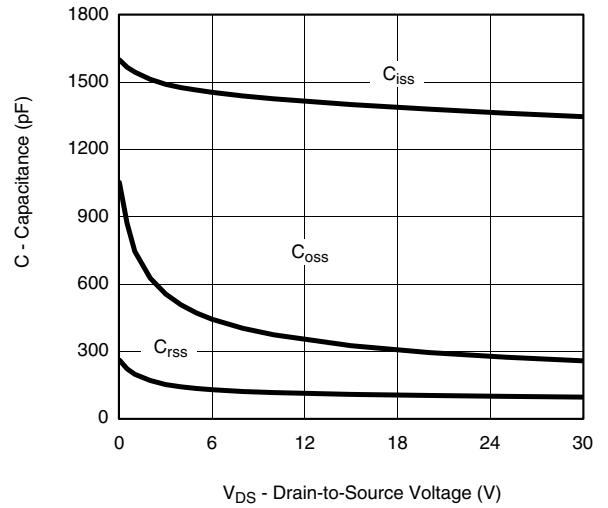
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



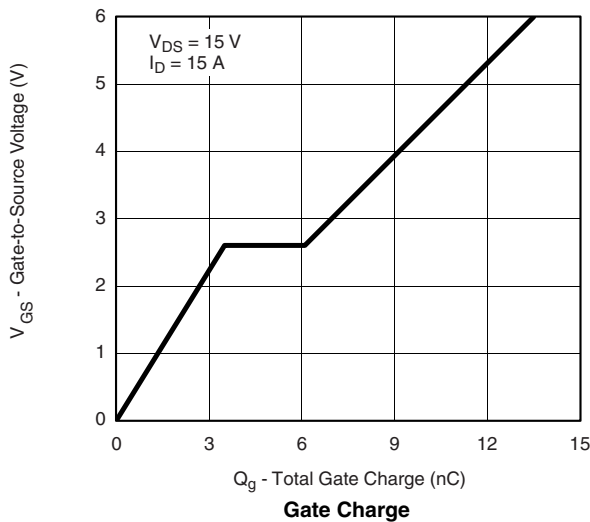
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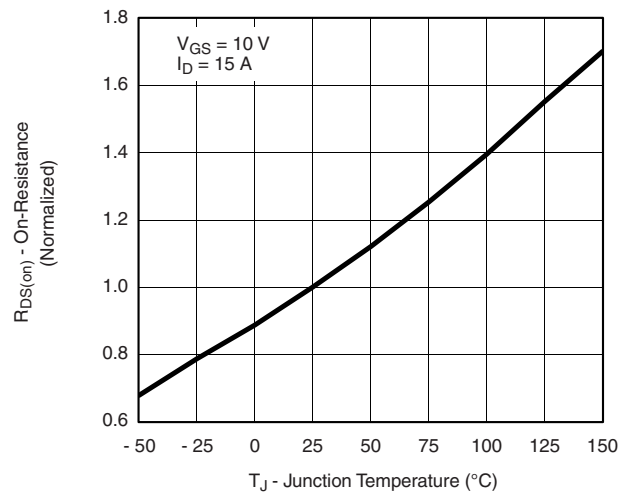
On-Resistance vs. Drain Current



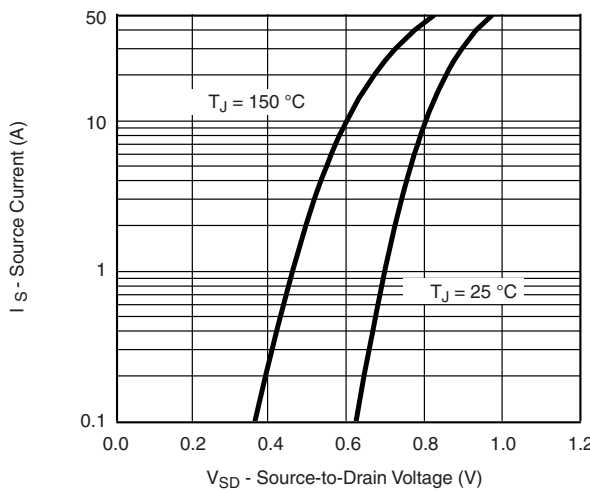
Capacitance



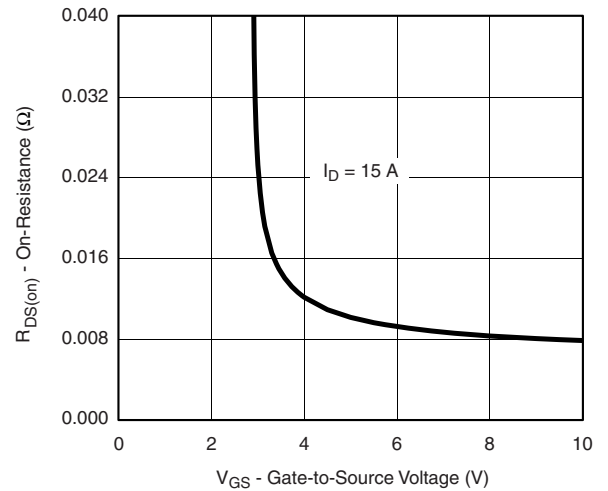
Gate Charge



On-Resistance vs. Junction Temperature

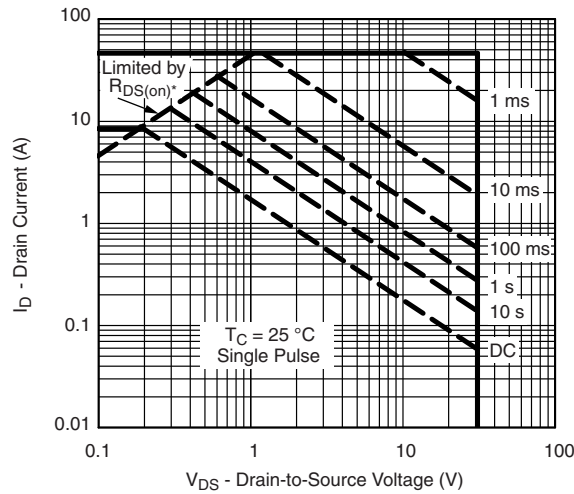
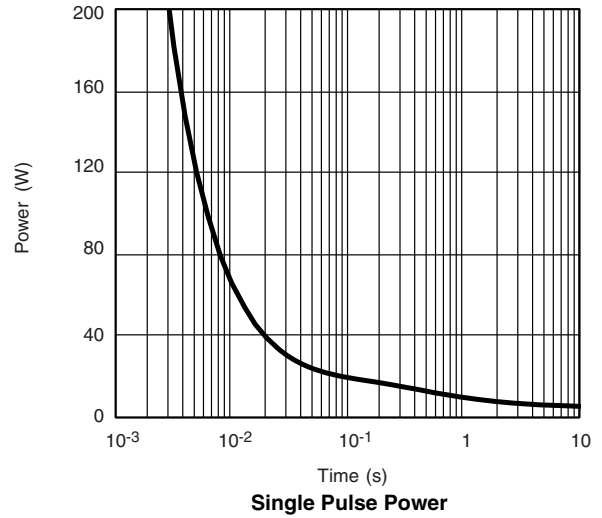
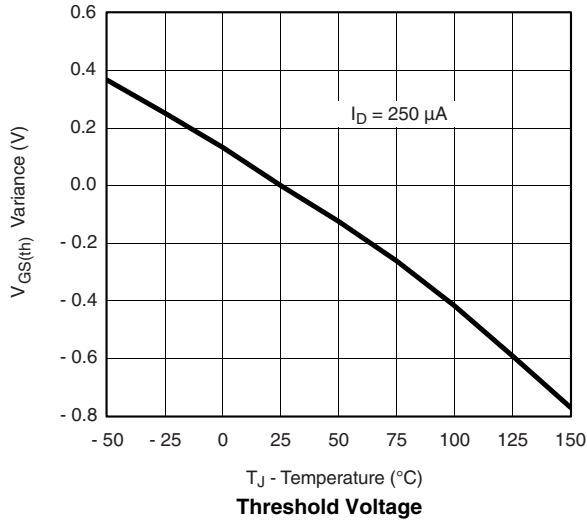


Source-Drain Diode Forward Voltage

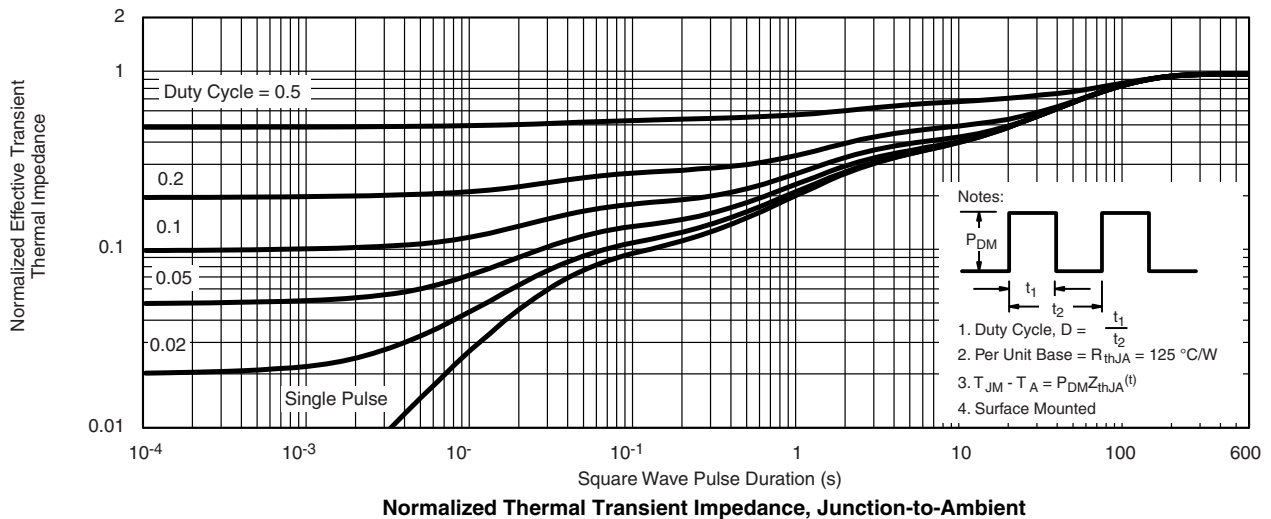


On-Resistance vs. Gate-to-Source Voltage

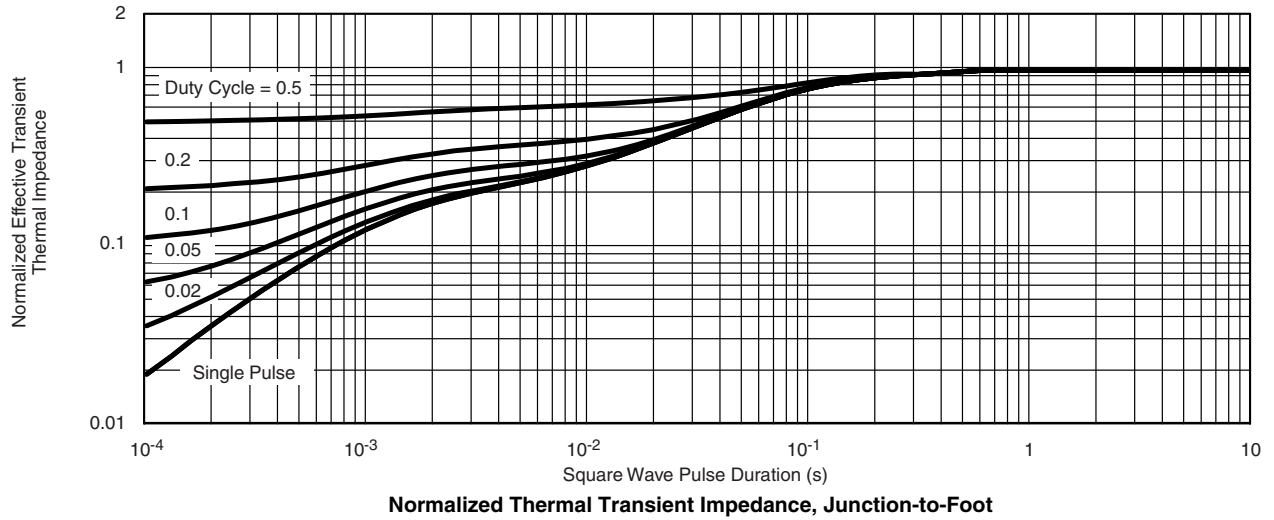
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



* $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



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