Assembling eGaN® FETs

eGaN FETs enable a new state-of-the-art in power conversion efficiency. One of the contributors to this new performance benchmark is that these FETs are in a chipscale Land Grid Array (LGA) package. This package format reduces board space, stray inductance, and parasitic resistance.

In this application note we discuss how to reliably mount these LGA packages on to a printed circuit board (PCB). Due to eGaN FET's small size and pitch, greater care is needed during the assembly process than for larger, less efficient form factors.

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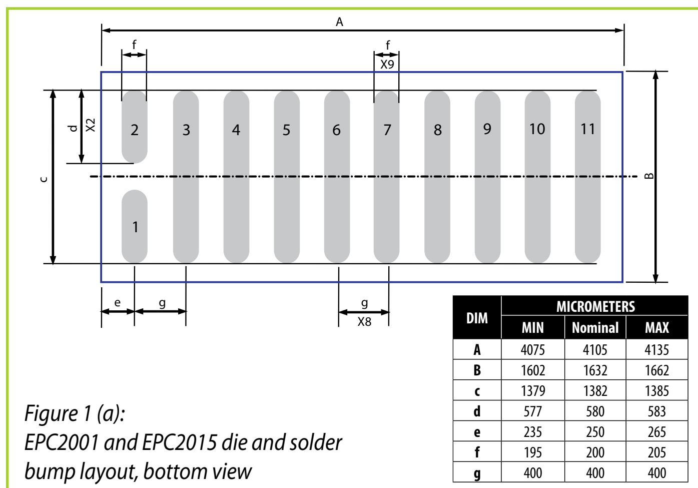
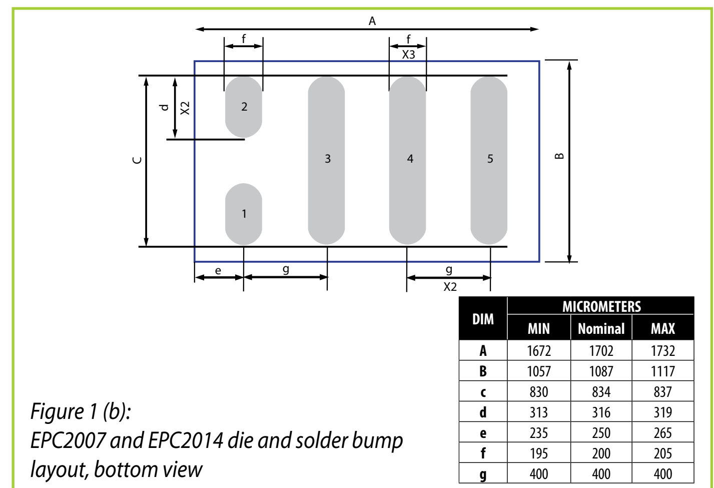
eGaN® FET Configurations

eGaN FETs are available in four different layout configurations (Figure 1). As of September 2011, all devices are lead free and halogen free. The RoHS compliant LGA package uses a Sn/Ag/Cu solder with a composition of 95.5% Sn, 4% Ag, and 0.5% Cu. Bump height is 100 µm +/- 20 µm.



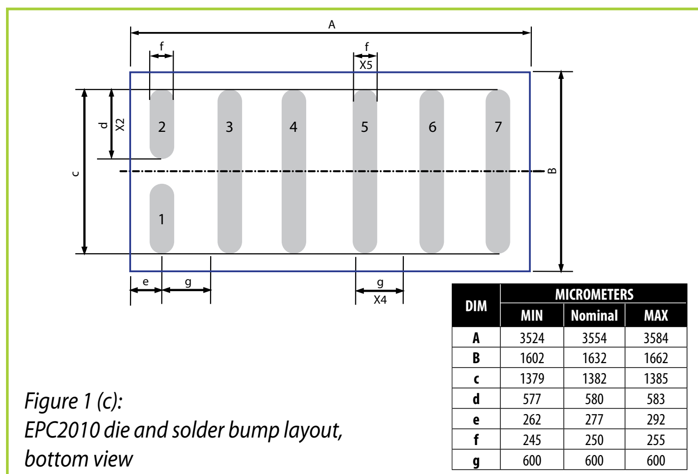
DIM	MICROMETERS		
	MIN	Nominal	MAX
A	4075	4105	4135
B	1602	1632	1662
c	1379	1382	1385
d	577	580	583
e	235	250	265
f	195	200	205
g	400	400	400

Figure 1 (a): EPC2001 and EPC2015 die and solder bump layout, bottom view



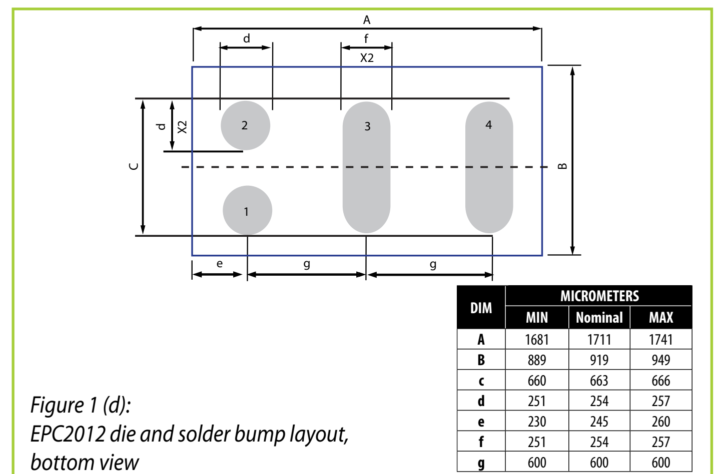
DIM	MICROMETERS		
	MIN	Nominal	MAX
A	1672	1702	1732
B	1057	1087	1117
c	830	834	837
d	313	316	319
e	235	250	265
f	195	200	205
g	400	400	400

Figure 1 (b): EPC2007 and EPC2014 die and solder bump layout, bottom view



DIM	MICROMETERS		
	MIN	Nominal	MAX
A	3524	3554	3584
B	1602	1632	1662
c	1379	1382	1385
d	577	580	583
e	262	277	292
f	245	250	255
g	600	600	600

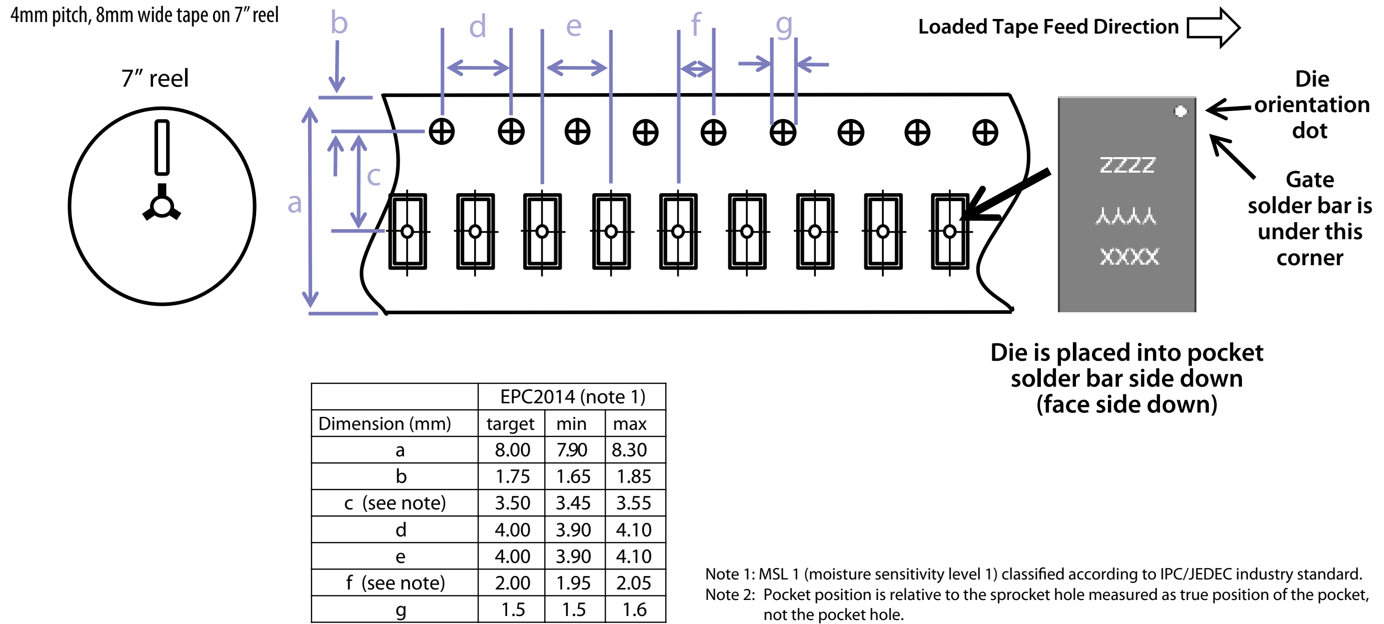
Figure 1 (c): EPC2010 die and solder bump layout, bottom view



DIM	MICROMETERS		
	MIN	Nominal	MAX
A	1681	1711	1741
B	889	919	949
c	660	663	666
d	251	254	257
e	230	245	260
f	251	254	257
g	600	600	600

Figure 1 (d): EPC2012 die and solder bump layout, bottom view

All lead free products are moisture sensitivity level 1 (MSL1 260°C), the highest commercial semiconductor level, and are delivered in tape and reel for efficient, low cost assembly as shown in Figure 2.



Dimension (mm)	EPC2014 (note 1) target	min	max
a	8.00	7.90	8.30
b	1.75	1.65	1.85
c (see note)	3.50	3.45	3.55
d	4.00	3.90	4.10
e	4.00	3.90	4.10
f (see note)	2.00	1.95	2.05
g	1.5	1.5	1.6

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.
Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

Figure 2: Tape and Reel Configuration

EGAN® FET ASSEMBLY DESIGN GUIDE

Land Pattern Design

Figure 3 shows the recommended land pattern design for each of the four eGaN FET layout configurations listed in Table 1. A Solder-mask-defined (SMD) land pattern is preferred as it provides a more accurate pattern registration than NSMD (non-solder-mask-defined) land pattern. The SMD land pattern is required due to the fine pitch configuration and to aid in preventing die tilt. The SMD land patterns are derived by bringing in the solder mask from each side of the solder bar by 10 µm. For products with 200 µm wide solder bars, the solder mask defined land pad width will be 180 µm wide. For products with 250 µm wide solder bars, the solder mask defined land pad width will be 230 µm wide.

Table 1

Part Number	Package (mm)	Lead Free	V_{DS} (V)	V_{GS} (V)	$R_{DS(ON)}$ (mΩ)	Q_G (nC)	Q_{GS} (nC)	Q_{GD} (nC)	V_{TH} (V)	Q_{RR} (nC)	I_D (A)
EPC2014	LGA 1.7x1.1	Yes	40	6	16	2.8	0.67	0.48	1.4	0	10
EPC2015	LGA 4.1x1.6	Yes	40	6	4	10.5	3.0	2.2	1.4	0	33
EPC2007	LGA 1.7x1.1	Yes	100	6	30	2.1	0.5	0.6	1.4	0	6
EPC2001	LGA 4.1x1.6	Yes	100	6	7	8.0	2.3	2.2	1.4	0	25
EPC2012	LGA 1.7x0.9	Yes	200	6	100	1.5	0.33	0.57	1.4	0	3
EPC2010	LGA 3.6x1.6	Yes	200	6	25	5.0	1.3	1.7	1.4	0	12

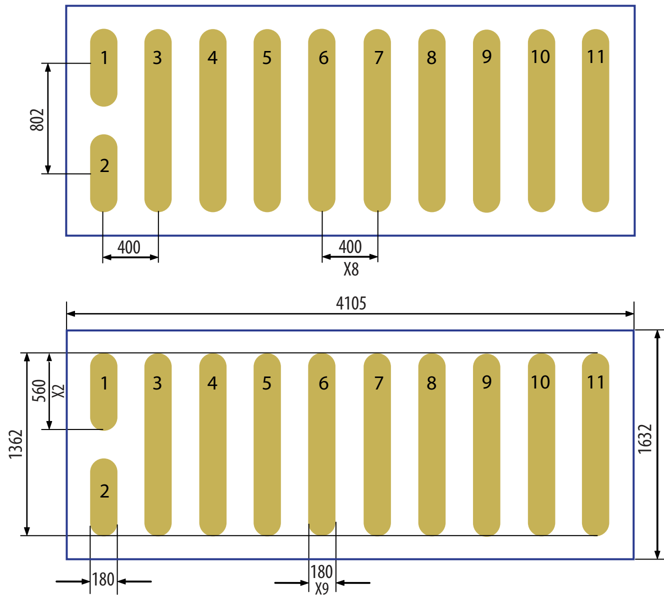


Figure 3 (a):
Recommended land pattern for EPC2001 and EPC2015 (dimensions in microns)

Land Pattern is Solder Mask Defined. Solder mask is 10µm smaller per side than the bump.

Pad no. 1 is Gate
Pads no. 3, 5, 7, 9, 11 are Drain
Pads no. 4, 6, 8, 10 are Source
Pad no. 2 is Substrate

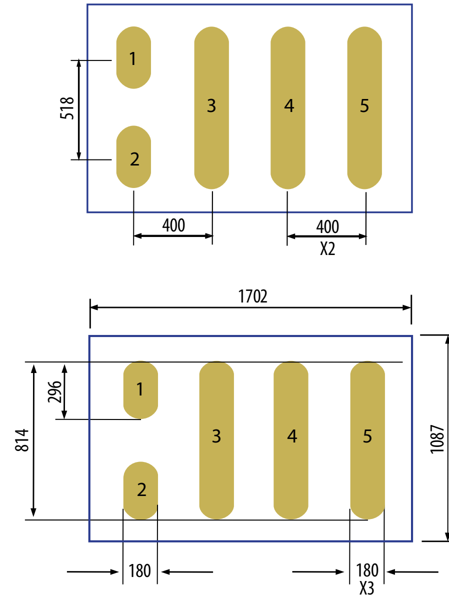


Figure 3 (b):
Recommended land pattern for EPC2007 and EPC2014 (dimensions in microns)

Land Pattern is Solder Mask Defined. Solder mask is 10µm smaller per side than the bump.

Pad no. 1 is Gate
Pads no. 3 and 5 are Drain
Pads no. 4 is Source
Pad no. 2 is Substrate

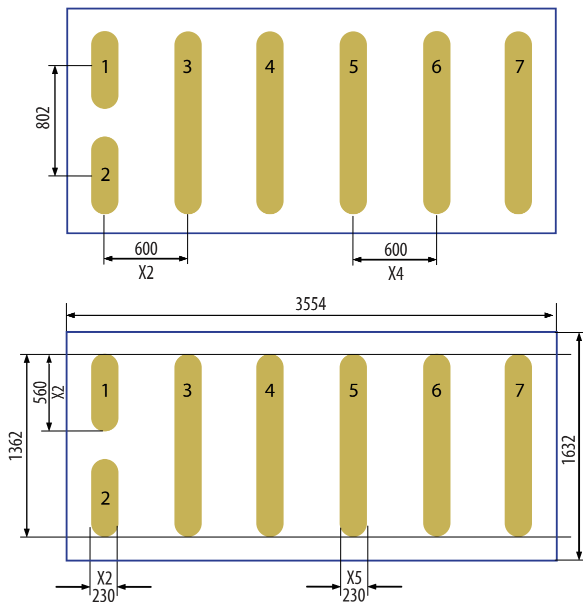


Figure 3 (c):
Recommended land pattern for EPC2010 (dimensions in microns)

Land Pattern is Solder Mask Defined. Solder mask is 10µm smaller per side than the bump.

Pad no. 1 is Gate
Pads no. 3, 5 and 7 are Drain
Pads no. 4 and 6 are Source
Pad no. 2 is Substrate

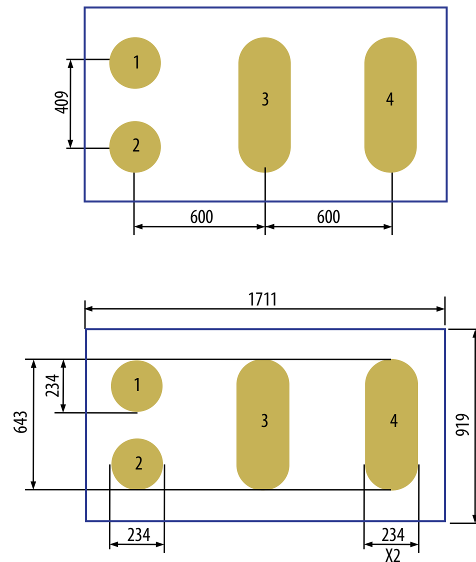


Figure 3 (d):
Recommended land pattern for EPC2012 (dimensions in microns)

Land Pattern is Solder Mask Defined. Solder mask is 10µm smaller per side than the bump.

Pad no. 1 is Gate
Pads no. 3 is Drain
Pads no. 4 is Source
Pad no. 2 is Substrate

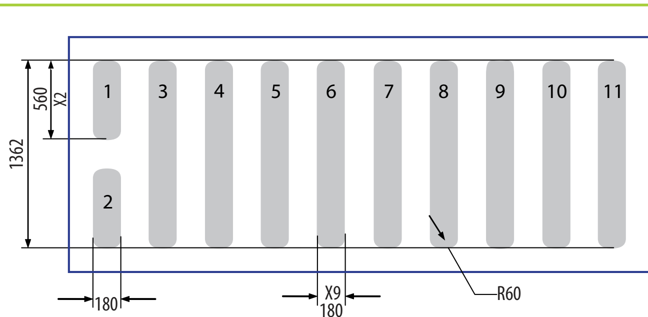


Figure 4 (a):
Recommended Stencil Aperture Design for EPC2001 and EPC2015 (units in µm)

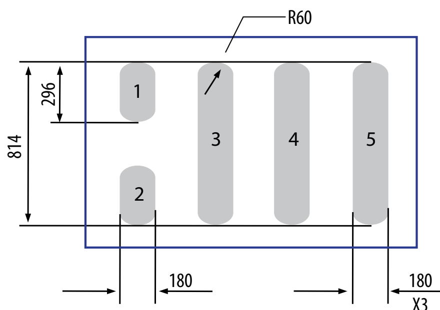


Figure 4 (b):
Recommended Stencil Aperture Design for EPC2007 and EPC2014 (units in µm)

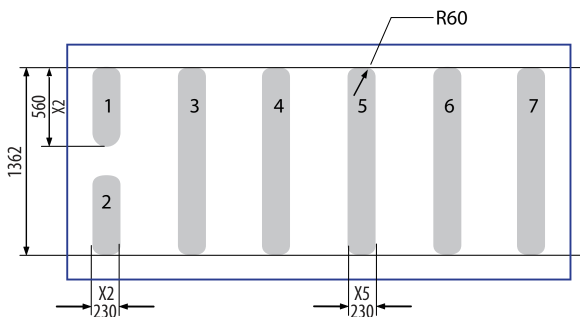


Figure 4 (c):
Recommended Stencil Aperture Design for EPC2010 (units in µm)

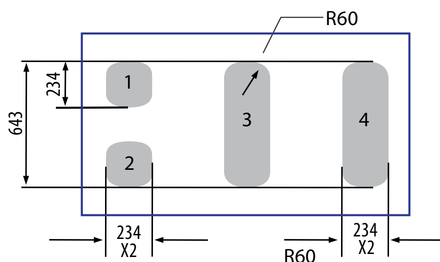


Figure 4 (d):
Recommended Stencil Aperture Design for EPC2012 (units in µm)

Surface Finish

The commonly used pad-surface finishes are as follows:

- NiAu (electroless nickel immersion gold);
- OSP (organic solderability preservative);
- HASL (hot-air surface leveling);
- Immersion Ag (silver).

Die Pad Top Copper Layer

A 2 ounce top layer Cu and through PCB vias just outside of the die area are recommended. Vias should not be placed under the solder bars unless they are micro vias and completely filled with copper. Vias with holes located directly under the source, gate, or drain solder bars will cause wide variation in the die stand-off distance to the PCB. Variation in stand-off distance could (1) affect the user's ability to thoroughly clean between the FET and the PCB, (2) add to die tilt variation, and (3) reduce the transistor's temperature cycling performance.

Stencil Design

The recommended stencil aperture designs are shown in Figure 4 and schematic illustrations of the device in relation to the various layers is shown in Figures 5 and 7.

The rectangular shaped stencil apertures are the same length and width dimensions as the land pads. The corners of the apertures are rounded with a radius of 60 µm. The recommended stencil foil thickness is 100 µm.

Solder Paste and Solder Paste Printing

Typically SAC305 solder, or the higher-cost SAC405 is used with a particle size of Type 3 or Type 4. The solder paste typically contains around 88.5% metal loading. Solder pastes with a no-clean flux are recommended. It is also recommended to clean the no clean flux.

As examples, EPC has used the following solder systems during reliability testing: AIM Solder NC257-2 SAC305 Lead Free No Clean Solder Paste and SMIC Senju Metal Industry Co. Eco Solder M705-GRN360 K-V-Series. The reflow profiles for these two systems are shown in Figure 6. It should be noted that the vendor recommended reflow guidelines for the particular solder being used should be followed, not necessarily the reflow profiles for a different solder that EPC used.

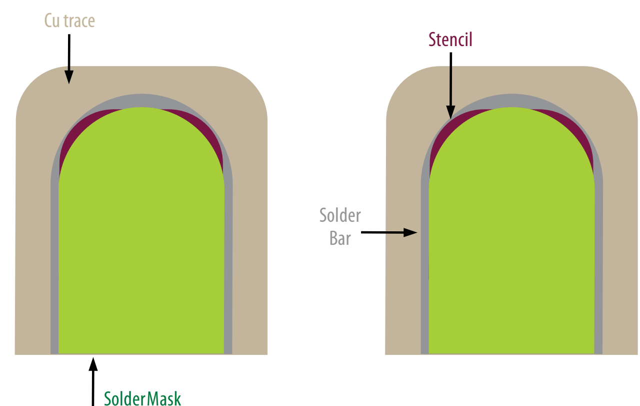
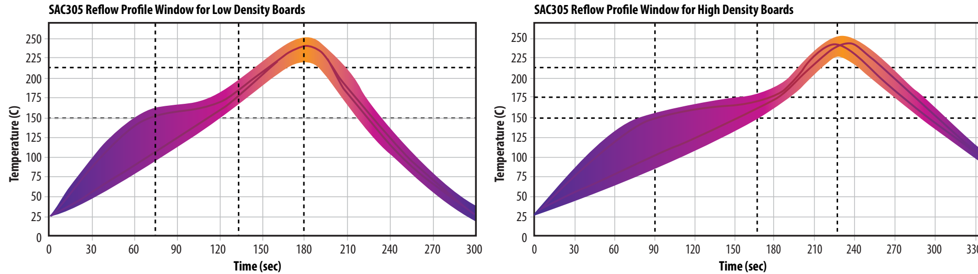


Figure 5: Top view showing the relationship between the solder bar, solder stencil, and top copper trace.

Reflow Profile

Two unique profile families are depicted below; both can be used in ramp-spike or ramp-soak-spike applications, and they each have similar reflow temperatures. The two profiles differ in where they reach their respective peak temperatures, as well as the time above liquidus (TAL). The shorter profile of the two would apply to smaller assemblies, where as the longer profile would apply to larger assemblies, such as backplanes or high-density boards. The shaded area defines the process window. Oven efficiency, board size/mass, component type and density all influence the final profile for a given assembly. These profiles are starting points, and processing boards with thermal-couples attached is recommended to optimize the process.



Rate Of Rise 2°C / Sec Max	Ramp To 150°C (302°F)	Progress Through 150°C-175°C (302°F-347°F)	To Peak Temp 230°C-245°C (445°F-474°F)	Time Above 217°C (425°F)	Cooldown ≤ 4 °C / Sec	Profile Length Ambient To Peak
Short Profiles	≤ 75 Sec	30-60 Sec	45-75 Sec	30-60 Sec	45± 15 Sec	2.75-3.5 Min
Long Profiles	≤ 90 Sec	60-90 Sec	45-75 Sec	60-90 Sec	45± 15 Sec	4.5-5.0 Min

- THE RECOMMENDED REFLOW PROFILE FOR NC257-2 IS PROVIDED AS A GUIDELINE. OPTIMAL PROFILE MAY DIFFER DUE TO OVEN TYPE, ASSEMBLY, LAYOUT, OR OTHER PROCESS VARIABLES. CONTACT AIM TECNICAL SUPPORT IF YOU REQUIRE ADDITIONAL PROFILING ASSISTANCE.
- THE REFLOW PROFILE FOR THE SnAgCu PASTES USING A VAPOR PHASE REFLOW OVEN: PEAK TEMPERATURE RANGE IS 230°C – 245°C.

Figure 6 (a): Reflow profile from AIM Solder NC257-2 SAC305 Lead Free No Clean Solder Paste 12/10 Rev15; http://www.aimsolder.com

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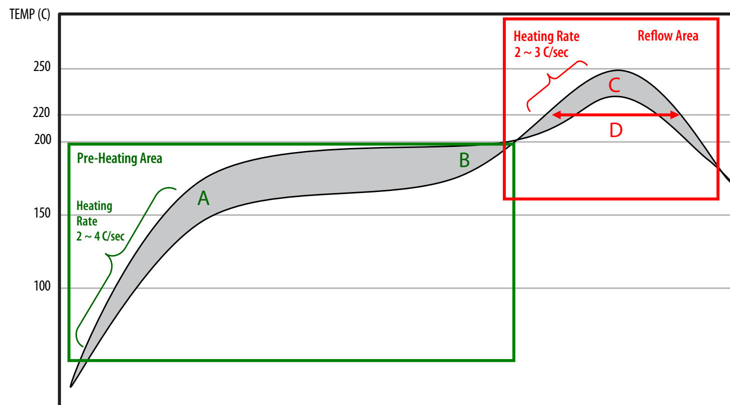
M705-GRN360-K-V Recommended Reflow Temperature Profile

Senju's recommended reflow temperature profile for M705-GRN360-K-V is shown below. On the PCB, a difference of temperature occurs according to differences in heat capacity of parts on the assembled PCB. However, it is ideal that all soldering points on the PCB reach the following recommended zones and times.

In addition, soldering characteristics may vary depending on reflow oven specifics, PCB mounting, and loading components. Performing a check evaluation is recommended.



Recommendation Value at Each Point

A: soak start:	150 ～ 180°C	C: Peak temp.:	230 ～ 250°C
B: soak end:	170 ～ 200°C	D: time above 220°C (solidus line)	30 ～ 60sec
A — B: soak time:	90 ±30sec		

Our recommended equipment for reflow:
SAI-3808 (Air convection type)
SNR-725 (For Nitrogen)

Figure 6 (b): Reflow profile from SMIC Senju Metal Industry Co. Eco Solder M705-GRN360 K-V-Series specification sheet TC-P40-3 4F May 2004 "Spec M705-GRN360-K2V.pdf' ; http://www.senju-m.co.jp/en/product/ecosolder

Die Placement

Misalignment of bumps on the die to the land pads on the PCB by 50 µm or less is recommended, but misalignment up to 100 µm during placement of the die on the PCB is tolerable because the surface tension of the molten solder will self-align the die to the land pads.

It is advisable not to correct a placement offset. This can smear the paste underneath, and can lead to bridging and solder balling.

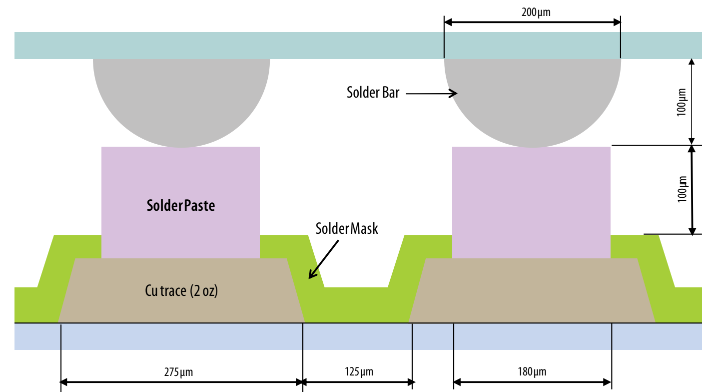


Figure 7: Schematic cross-sectional view of a die placed on a PCB with a stencil-printed solder paste.

Quick-Start Lab Assembly

eGaN FET users can generally apply standard surface mount techniques to successfully attach the FETs onto standard PCBs. However, design engineers working in a lab environment may wish to mount devices quickly and reliably.

EPC's eGaN® FETs can be mounted directly onto PC boards without added solder by using a tacky flux to hold the part in place while reflowing the solder. An example of an acceptable Lead Free (PbF) process uses Kester TSF6502 no-rinse flux. The reflow profile used by EPC to assemble product is shown in Figure 8 compared with the manufacturer's recommended profile. Please note that this recommended profile that has been used on the EPC PbF parts shows a peak temperature of 232C.

EPC has developed a Quick Reference Procedure Guide both for Die Attach and Die Removal. These documents can be found at: http://epc-co.com/epc/DesignSupportbr/Applications/AssemblyBasics.aspx

Note : Kester recommends the use of TSF-6592LV for PbF processes. This flux is reflow-able with peak temperatures up to 270C. (http://www.kester.com ; See Products/ChipAttachFlux/TackyFluxes TSF6502 and TSF-6592-LV)

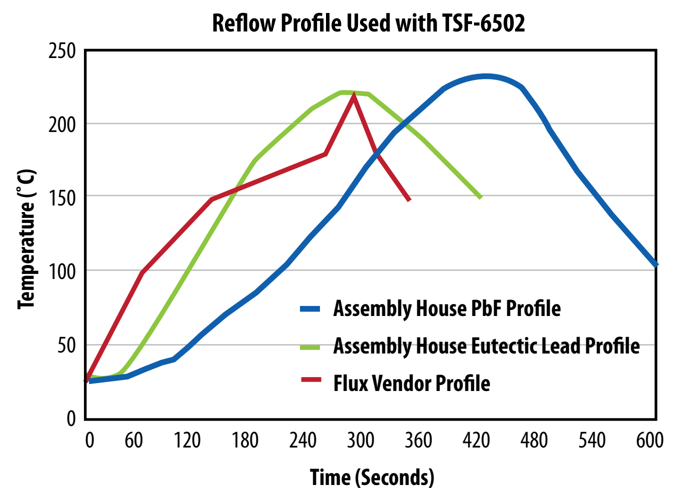


Figure 8: Reflow profile for Kester TSF6502 overlaid with assembly house profiles

Die Storage Requirements

EPC's GaN transistors are packed in vacuum sealed antistatic bags and have demonstrated Moisture Sensitivity Level 1(MSL1) capability. As a result, no special care needs to be taken to protect the devices once the vacuum sealed bags are opened.

Heatsinking

eGaN FETs are able to conduct significantly higher current than similarly-sized power MOSFETs. In general, the lower on-resistance and lower temperature coefficient of that on-resistance [1] make additional heatsinking unnecessary. If, however, even greater power density is desired, heatsinks can be attached directly to the back of the GaN device as per Figure 9 provided the heatsink is electrically connected to the source of the die below, or isolated from the die with thermally conducting insulator. To avoid mechanically damaging the devices it is very important to make certain the mount down process minimizes die tilt, and it is recommended that a thermal pad be used between the device and the heatsink such as 3M thermally conductive interface pads [2], Dow Corning thermal interface pads and films [3], or Bergquist Gap Pads[4].

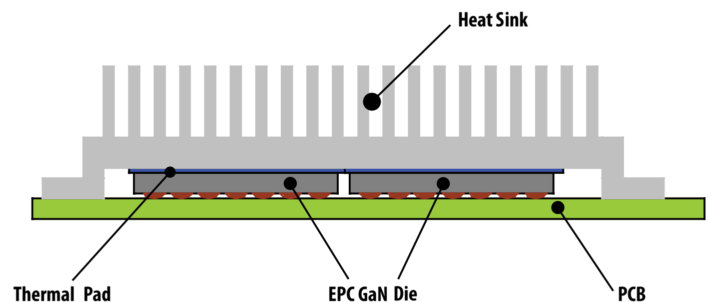


Figure 9: eGaN FETs mounted on a PCB with heatsink directly attached

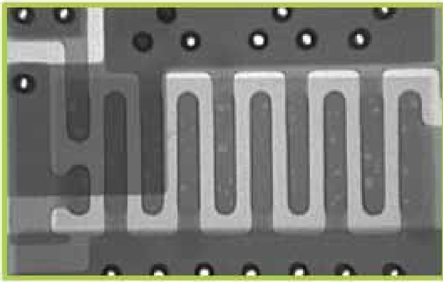


Figure 10: X-Ray of eGaN FET after tacky flux process

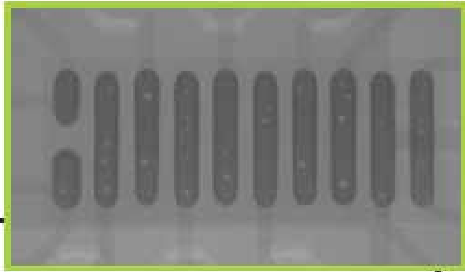


Figure 11: X-Ray of eGaN FET after solder stencil proces

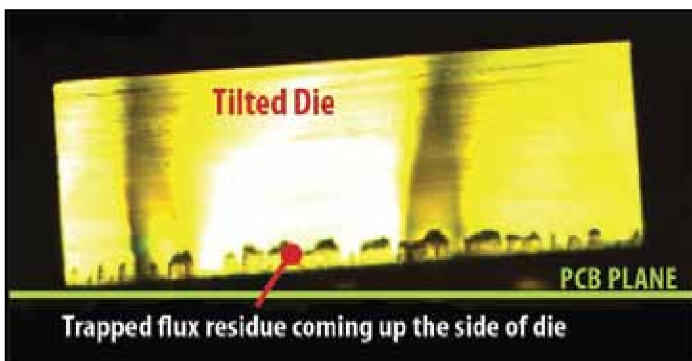


Figure 12: Side view of an eGaN FET with severe die tilt after soldering

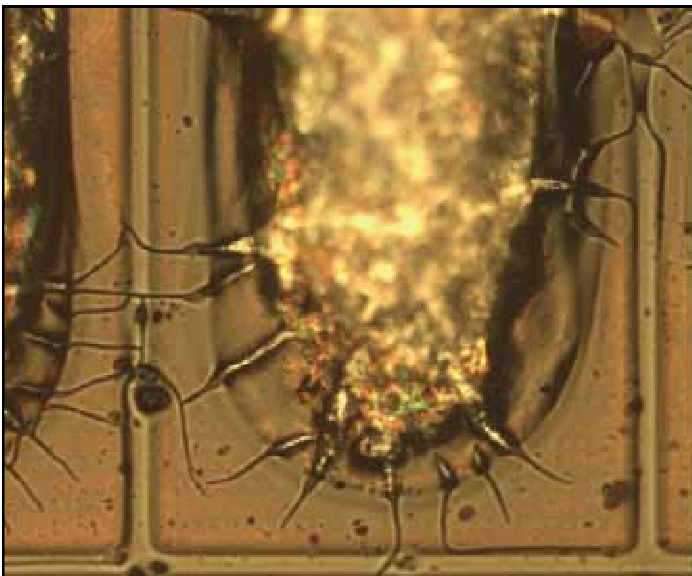


Figure 13: eGaN FET showing dendrite formation after exposure to residual flux

Inspection

eGaN FETs are mechanically robust and have demonstrated high yield in volume assembly. Damage, however, can still occur if several standard precautions are not taken to ensure adequate solder reflow, reduce excessive die tilt, and avoid residual uncured solder flux.

Adequate solder reflow

Even though eGaN FETs have been designed such that the reflowed solder is visible to the unaided eye, as with all chip scale packaging the best way to determine if devices are properly reflowed is by taking X-ray images. Figures 10 and 11 show X-ray images of parts assembled with tacky flux (no added solder) and with a solder stencil process. It was found that the solder stencil process typically yields less voiding, but both processes can be used to produce a reliable product.

Die Tilt and Dendrites

During product testing and assembly process development, several parts were observed to be tilted after reflow using a solder stencil process (Figure 12). The main causes of die tilt were found to be; (1) uneven thickness of solder paste, (2) excessive vibration during reflow, (3) non-optimized temperature profile and (4) oversized solder mask and / or oversized solder stencil.

If the assembly process uses a solder with a flux that requires rinsing, die tilt can obstruct the flow of the rinse and cause flux to be trapped under the die. This residual flux can cause rapid formation of dendrites (Figure 13) which will cause early device failure. For this reason, using a no rinse solder flux with low ionic content and then rinsing the no rinse flux is recommended.

If there is no die underfill and the assembly process uses flux to attach components to the PCB after die attach reflow, the flux must be fully cured prior to applying any bias to the device. Dendrites such as those shown in Figure 13 can be formed in just a few seconds if the die is biased in the presence of uncured flux. Flux cure can generally be achieved by heating the PCB to 150°C for 30 min, or 125°C for 60 min.

Summary

GaN FETs give the power conversion designer a whole new spectrum of capabilities unachievable with silicon-based power MOSFETs. The intrinsic low conduction losses and high frequency capability are complimented by the ability of eGaN FETs to be assembled with chipscale packaging. The assembly technology required is not significantly more demanding than the technology already in place for high-density SO packages.

REFERENCES

[1] Alex Lidow, "Is it the End of the Road for Silicon?", http://epc-co.com/epc/documents/product-training/Appnote_Si_endofroad.pdf

[2] 3M pads : http://solutions.3m.com/wps/portal/3M/en_WW/electronics/home/productsandservices/products/TapesAdhesives/ThermalInterface/

[3] Dow Corning Pads: http://www.dowcorning.com/content/etronics/etronicspadsfilm/

[4] Bergquist Pads: http://www.bergquistcompany.com/thermal_materials/gap_pad/pdfs/gap-pad-vo-soft/PDS_GP_VOS_12.08_E.pdf